Heat Balanced Bolometer with Sigma-Delta Interface

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***Abstract*—This paper presents a single-loop 2nd order sigma-delta interface circuit for a bolometer operating in closed-loop mode. Switched capacitor circuitry is developed to implement the sigma-delta structure. The sigma-delta modulator acts both as digital readout circuit and as a mean of heat feedback. The design approach of the sigma-delta structure and the feedback shaping is explained. The circuit is designed for a realization in AMS CMOS 0.35µm technology.**

Keywords-bolometer; sigma-delta modulator; electrical substitution; frequency sensor.

I. INTRODUCTION

Uncooled resistive bolometers are part of the thermal infrared detector's category. In 2010, uncooled resistive bolometers represented 95% of the market of infrared imaging system [1]. Their operating principle is based on the measurement of temperature variations due to the incident optical power. In parallel to research work trying to improve the sensitivity of the bolometers through material or geometry optimization, other research work has focused on the development of feedback techniques to operate the bolometers in closed-loop mode as constant temperature bolometric detectors [2, 3]. All the proposed techniques are based on the Electrical Substitution principle that assumes that optical power can be substituted by electrically produced power. For integration and simplicity reasons, heat feedback is produced by Joule effect, considering that heat electrically produced can be used to equivalently stimulate the sensing resistor of the bolometer. This assumption is the basis of the Electrical Substitution (ES) principle also called Electric Equivalence principle [3, 4]. The advantages of closed-loop operation are numerous, including improvement of bandwidth and reduction of spatial noise. In 2009, a new configuration has been proposed for the closed-loop operation of resistive bolometers [5]. The so-called Capacitively Coupled Electrical Substitution (CCES) configuration exhibits the advantages of previous configurations without their limitations in terms of additional material required or stability issues. Proofs of principle of the CCES configuration have been demonstrated through successive analogous and digital implementations with discrete components [5, 6]. Digital implementation, besides the implicit digital measurement output, exhibit extra performance compared to analogous implementation because of linearization of the system [4, 5]. Recently, smart-functions using a digital implementation of the CCES configuration with a microcontroller have been experimentally demonstrated [7].

In this work, we aim at integrating the electronic circuitry of the CCES configuration for closed-loop operation of resistive bolometers and for smart-functions implementation. With a view toward integration of lines or matrixes of pixels, digital solution using a sigma-delta core is preferred to solution using a microcontroller. Consequently, for the first time to our knowledge, an integrated sigma-delta interface for a bolometer is developed. The sigma-delta modulation is attractive because it provides a digital output, linearizes the heat feedback path and can be easily implemented in high-density CMOS technology. Such device will inherit the advantages and performance of the previous discrete realizations and will be the first step toward fully integrated smart infrared imagers.

The paper is organized as follows. The second section describes the principle of the digital closed-loop operation of resistive bolometers. The third section presents the design of the sigma-delta interface associated with the bolometer. Finally, the result section exhibits simulation results that illustrate the expected behavior and performance.

II. DESCRIPTION OF THE SYSTEM

The system is a heat balanced bolometer using heat feedback through electrical substitution means. It is composed of a resistive bolometer, its readout electronics, and a sigma-delta modulator with a feedback shaping block for the implementation of the CCES configuration.

A. *Uncooled resistive bolometers*

Resistive bolometers are composed of a sensing resistor on a surface thermally insulated from the substrate by suspension legs, as illustrated in Fig. 1.

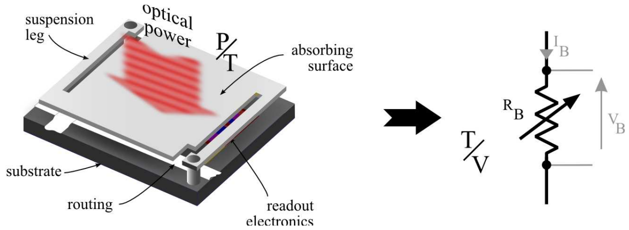

Figure 1. Top view of a bolometer pixel and equivalent electrical model

The operating principle is the following: the optical infrared (IR) power absorbed onto the surface of the bolometer rises the temperature of the sensing resistor (P/T conversion). If the sensing resistor (R_B) is current biased (I_B), then the voltage across the resistor (V_B) measures the temperature variations (T/V conversion). The material of the sensing resistor is chosen for its high Temperature Coefficient of Resistance (TCR).

The responsivity of a bolometer characterizes the variations of the output voltage signal (V_B) depending on the infrared input optical power (P_{opt}) [8]. It is expressed by

$$R(s)[V/W] = \frac{V_B(s)}{P_{opt}(s)} = \frac{\alpha \eta I_B R_B}{G_{eff}(1 + s\tau_{eff})} \quad (1)$$

where α is the TCR of the sensing resistor, η is the absorption coefficient of the absorbing surface, G_{eff} and τ_{eff} are the effective thermal conductance and the effective thermal constant respectively [8]. τ_{eff} depends on the heat capacity C_{th} of the bolometer as follows: $\tau_{eff}=C_{th}/G_{eff}$. The equation (1) indicates that the more the bolometer is thermally insulated, *i.e.* G_{eff} small, the higher the responsivity is. However, the more the bolometer is thermally insulated, the higher the time constant is, *i.e.* the slower the bolometer is. This is the traditional tradeoff between responsitivity and time constant of resistive bolometers. Usually, the thermal conductance is designed to match the time constants required for imaging applications and therefore the responsivity is not optimized. Such tradeoff can be released by operation in closed-loop mode.

B. Closed loop operation of uncooled resistive bolometers

Like for every sensor and generally speaking system, closed-loop configuration has advantages over open-loop configuration, including reduced time response and linearization. Closed-loop operation of resistive bolometers enables other interesting characteristics such as operation around a user defined operating point and simple selection of the measurement range. In the case of matrixes of bolometer pixels, since the output response in closed-loop is quite independent from the nominal resistance value of the sensing resistor, the spatial noise due to process discrepancies is intrinsically cancelled.

Closed-loop operation requires heat feedback since the incoming signal is power. Fig. 2 illustrates the closed-loop configuration of a resistive bolometer. The system is controlled in temperature to a dynamic set point defined by a bias voltage V_{Bias}. G is the gain of the conditioning electronics and V_T the amplified voltage. The absorbed incoming optical power, ηP_{opt}, is considered as a perturbation compensated by the Joule power P_J. The closed-loop system maintains the temperature of the bolometer constant by keeping the total amount of power constant. The total power corresponds to the Joule power initially applied prior to exposure to optical power to elevate the temperature

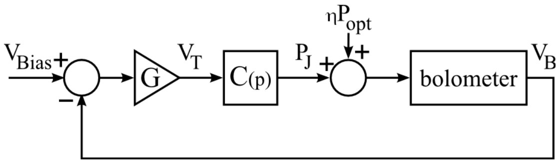

Figure 2. Schematic of electrical substitution feedback loop

of the bolometer. This initial power sets the static thermal working point. A controller C(p) is inserted in the loop to adjust the performance of the closed-loop system (bandwidth, robustness, noise rejection, …). As usually R(s).G is large, a simple controller C(p)=1 can be used in a first try.

Bolometers operating in closed-loop mode have been developed either with analog or digital feedback implementations. Digital implementation is interesting in that the feedback path is linearized in a simple way if pulsed modulated signals are used [4, 5] and in that the output signal is directly digital. The digital pulsed signals can be modulated in width (PWM, pulsed width modulation) or in density (sigma-delta modulation). The major drawback of previously proposed digital implementation [6] is the need for a microcontroller with an ADC for the digital feedback path. We propose here to use a sigma-delta modulator both for the digital conversion and the feedback signal generation. This approach is somehow comparable to that of micro-accelerometers operating in closed-loop mode with sigma-delta modulators. In the case of lines or matrixes of bolometer pixels, this approach should lead to a solution better suited for integration.

The schematic of the sigma-delta feedback loop for the bolometer is illustrated in Fig. 3, with a controller C(p)=1.

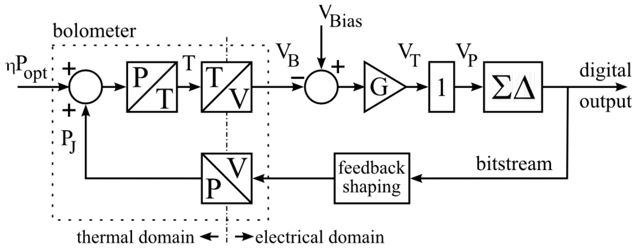

Figure 3. Schematic of sigma-delta feedback loop for the bolometer

The output bitstream corresponding to the measurement at the output of the sigma-delta modulator would have to be treated by digital filters and decimators to get the output signal with the format resolution allowed by the oversampling rate.

The feedback shaping is here to implement the capacitively coupled electrical substitution (CCES) that enables easy setting of the system. In the case of the CCES implementation, the pulsed modulated signal is shifted to high frequencies by modulation with a carrier and then capacitively coupled onto the sensing resistor of the bolometer. The objective is to dissociate the electrical and thermal working points according to a frequency basis. It uses a high frequency modulated signal for the heat feedback voltage applied to the sensing resistor. This implementation can be applied to any kind of uncooled resistive bolometer.

The sigma-delta interface for heat balanced bolometer using CCES configuration requires two main functional blocks:

(1) a sigma-delta modulator,
(2) a feedback shaping block.

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III. DESIGN OF THE CIRCUIT

The design is for AMS 0.35 µm CMOS technology.

A. *Sigma-Delta (ΣΔ) modulator*

For stability, linearity and resolution reasons, a single-loop, single-bit, 2nd order sigma delta architecture was chosen for the sigma-delta modulator [9]. The resulting architecture is illustrated in Fig. 4. It is composed of two integrators with gain a and b respectively -0.5 and -2.0, of a comparator and of a 1-bit digital-to-analog converter. Compared to classical architectures, here an extra input on the first integrator is used to add a component to the signal. The role of this input is to set the static thermal working point, *i.e.* the Joule power applied in absence of optical signal. The oversampling ratio (OSR) is 256 to ensure at least the 98 dB signal-to-noise ratio required for a 16-bit resolution according to [9]

$$\mathrm{SNR_{dB}} = 10\log\left[\frac{3\pi}{2}\left(2^B-1\right)^2\left(2n+1\right)\left(\frac{OSR}{\pi}\right)^{2n+1}\right] \quad (2)$$

where B is the number of bits of the quantizer, n is the order of the modulator.

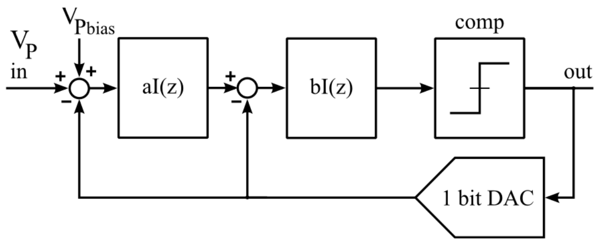


Figure 4. Block diagram of the 2nd order single loop 1-bit ΣΔ modulator

For integration reasons, switched capacitor circuitry was chosen leading to the classical fully-differential structure illustrated in Fig. 5. The sigma-delta modulator is clocked at 5 MHz for an input bandwidth of 10 kHz. Non-overlapping two-phase clock signals with delayed outputs are used and double sampling correlation is implemented to reduce the flicker noise contribution of the OTA [10]. The capacitors are 500fF minimum to ensure a kT/C noise small enough compared to the quantization noise.

The integrators are built around folded-cascode OTA with gain above 60 dB to ensure the chosen resolution [11]. Folded-cascode OTA with switched-capacitor common mode feedback circuitry was chosen for stability reasons and for its high gain-bandwidth product, here over 100 MHz.

The common mode voltages of the first integrator, V_{cm1+} and V_{cm1-}, are used to set the static thermal working point; they correspond to the V_{Pbias} signal of Fig. 4. These inputs can also be used as built-in stimuli useful for self-test, self-calibration or self-identification as illustrated in [12], *i.e.* useful to upgrade the bolometer into a smart-bolometer. The common mode voltage of the second integrator, V_{cm2}, is unique and is set at half the supply voltage.

B. *Feedback shaping block*

The role of the feedback shaping block is to translate to high frequency the pulse-density modulated bitstream of the sigma-delta modulator output. The feedback shaping block involves a Voltage Controlled Oscillator (VCO), a mixer and a programmable attenuator as illustrated in Fig. 6.

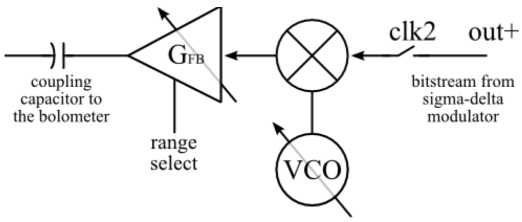


Figure 6. Feedback shaping

The VCO is a chain of inverters forming a ring topology whose frequency can be tuned between 70 MHz and 800 MHz. The mixer consists in a transmission gate controlled by the pulse-density modulated bitstream signal from the sigma-delta modulator. The programmable attenuator is a ladder of cascaded transmission gates with different ON resistances. The selected gain, G_{FB}, defines the measurement range of the closed-loop system. An 8-bit selection word allows changing the measurement range over more than two orders of magnitude. The feedback is only applied during the integration phase (clk2) not to disturb the sampling phase.

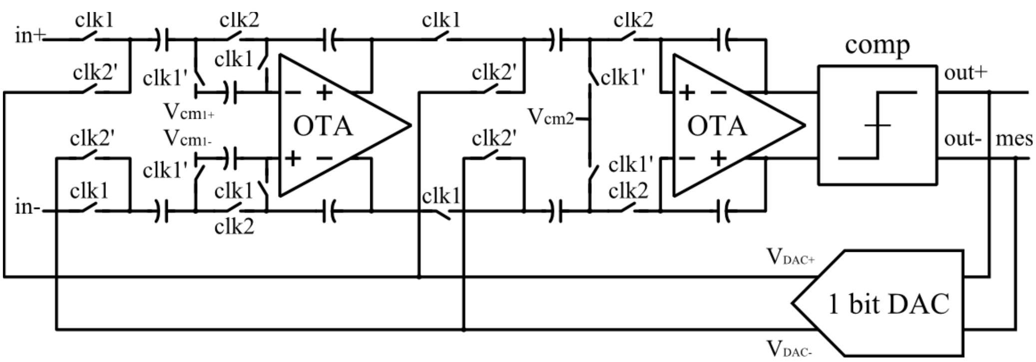


Figure 5. Schematic of the 2nd order sigma-delta modulator

IV. SIMULATION RESULTS, EXPECTED PERFORMANCE

Simulations performed to verify that the design fulfills the requirements are time consuming, therefore, once the performance validated, the blocks are modeled to carry out top-level simulations. The top-level simulations of the complete system are performed using Simulink®.

C. *Sigma-Delta simulation*

The electrical simulation results confirm the expected performances of the 2nd order sigma-delta modulator. The density of the pulses of the bitstream varies linearly according to the input signal (Fig. 7).

Since the voltage to power conversion (V/P) is linear with this type of modulation, the feedback path is entirely linear.

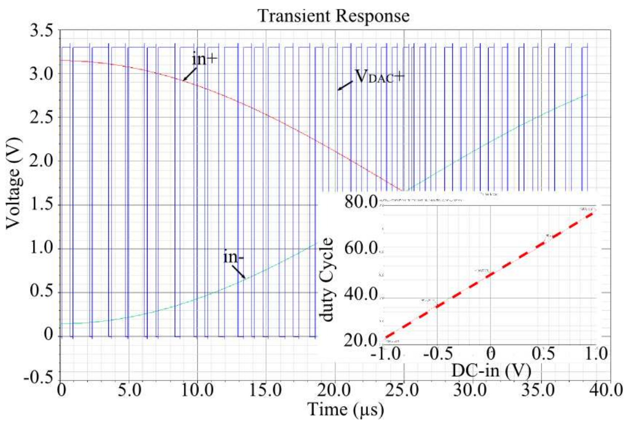
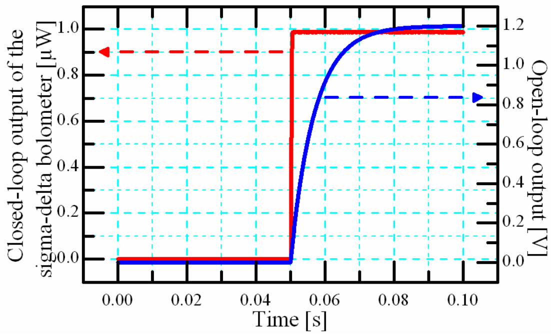


Figure 7. Transient simulation of the sigma-delta modulator. Inset, duty cycle versus DC input from transient simulations

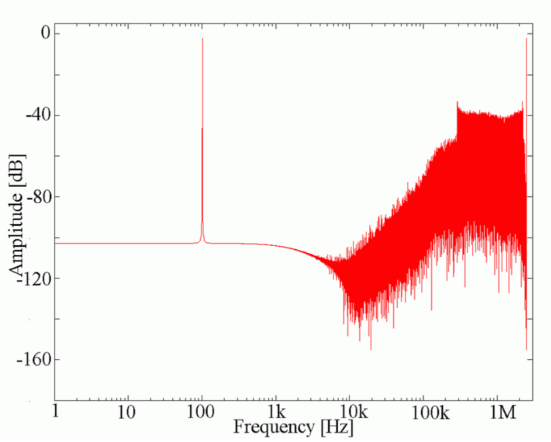
D. *Complete system*

The top-level simulations illustrate the expected behavior of the system and its expected noise performance. The models developed in [13] are used for the integrators of the sigma-delta modulator and for the noise considerations. Typical characteristics taken from [14] are used for the bolometer (7 ms time constant and 5×10^{-8} W/K thermal conductance). Fig. 8(a) illustrates the step response of both the bolometer in open-loop (output V_T) and in closed-loop mode when the bolometer is heat-balanced with the sigma-delta interface directly looped (output corresponding to the bitstream after filtering). The input step is 1 µW. The closed-loop operation is interesting in that the output is directly proportional to the incoming power and the time response is much faster, *i.e.* response time (5% final value) below 1 ms.

Fig. 8(b) illustrates the expected performances in terms of noise taking into account the noise sources of sigma-delta interface (quantization noise, kT/C noise, clock jitter noise, and OTA noise). The noise floor is 100 dB below the 50 µW reference signal, this means that the sigma-delta interface does not negatively impact the noise performance of the system, *i.e.* the noise performance will still be limited by the noise of the bolometer.



(a)



(b)

Figure 8. (a) Step response of the bolometer in open-loop and in closed-lopp when heat balanced with the sigma-delta interface. (b) Expected noise performance of the sigma-delta interface, with a 50 µW input reference signal at 100 Hz

IV. CONCLUSION AND FUTURE WORK

In this paper, the design of a sigma-delta interface for a heat balanced bolometer is presented. This interface enables an integrated implementation of the capacitively coupled electrical substitution configuration for uncooled resistive bolometers. By enclosing the bolometer in a one-bit feedback loop, simultaneous heat feedback and analog-to-digital conversion is achieved. The feedback path enables built-in stimulus to be applied and the resulting device is a pulsed digital output infrared detector part of so-called frequency sensors, with configuration capabilities upgrading it into a smart bolometer. Future work will involve the characterization and test of the realized prototypes and next development will focus on the integration of lines and matrixes of pixels.

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