A Low-Voltage Folded-Cascode OP Amplifier with a Dynamic Switching Bias Circuit

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***Abstract*—Wideband filters employing Operational Amplifiers (OP Amps) are required in sensing devices such as video cameras for environment sensing. A high-speed low-voltage Folded-Cascode (FC) OP Amp with a Dynamic Switching Bias (DSB) circuit capable of processing video signals, which enables low power consumption, high gain with wide bandwidths, and a wide dynamic range, was proposed. Through simulations, it was shown that the OP Amp with the reduced 3-V power supply is able to operate at a 14.3 MHz dynamic switching rate, allowing processing video signals, and a dissipated power of 57 % compared to that in the conventional 5-V power DSBFC OP Amp while keeping a 0.6 V wide output dynamic range. The response of the 2nd-order switched capacitor Low-Pass Filter (LPF) tested as its application was near the theoretical frequency response within frequencies below 5 MHz. The power dissipation of this LPF was also reduced to 56.8 % of that in the switched capacitor LPF with the conventional 5-V power DSBFC OP Amp.**

Keywords-CMOS; operational amplifier; dynamic switching; switched capacitor circuit; filter.

I. INTRODUCTION

Wideband filters are essential for signal processing in video electronic appliances. Specifically, a wideband Low-Pass Filter (LPF) is needed in sensing devices such as a CCD (Charge-Coupled Device) camera with a monitor handling a wide bandwidth video signal of over 2 MHz. The CMOS (Complementary MOS) Switched Capacitor (SC) techniques suitable for realizing analog signal processing ICs (Integrated Circuits), have promising use in video signal bandwidth circuits. It has been demonstrated that SC techniques using CMOS Operational Amplifiers (OP Amps) are useful for implementing analog functions such as filters [1]-[4]. Although CMOS OP Amps are suitable for such filter ICs, the use of several OP Amps results in large power consumption. Especially, the power consumption of OP Amps in high speed operation becomes large because they have wideband properties. There is a possibility that this causes unstable operation.

Until now, several approaches have been considered to decrease the power consumption of OP Amps, including the development of ICs that work at low power supply voltages [5][6]. In the two-stage Folded-Cascode (FC) OP Amp operating at the low power of 1 V [6], resistive biasing and capacitive level shifter are required to increase the output voltage swing. The requirement of four resistors for the resistive biasing makes it difficult to realize as an IC. A clocked current bias scheme for FC OP Amps suitable for achieving a wide dynamic range has typically been proposed to decrease the power consumption of the OP Amp [7][8]. Since the circuit requires complicated four-phase bias-current control pulses and biasing circuits, it is not suitable for the high speed operation and results in a large layout area.

Recently, the author proposed an FC CMOS OP Amp with a Dynamic Switching Bias circuit (DSBFC OP Amp), of simple configuration, to provide low power consumption while maintaining high speed switching operation suitable for processing video signals [9]. This OP Amp operating at the 5-V power supply voltage is not necessarily enough for use in low-voltage signal processing applications under the progress of miniaturization of equipment. That is, the development of OP Amps with a still lower power supply voltage is expected to decrease their power dissipation.

In this paper, a Low-Voltage (LV) DSBFC OP Amp with the 3-V power supply voltage is proposed, which enables low power consumption and is suitable for achieving wide bandwidths and realizing as an IC. The point of view in design for architecture and operation of the LV DSBFC OP Amp is discussed in Section Ⅱ. Simulation results for performance of the LV DSBFC OP Amp are shown in Section Ⅲ. As an application example of this OP Amp, its practicability for a 2nd-order SC Butterworth LPF is also evaluated in Section Ⅳ. Finally, conclusions of this work are summarized in Section Ⅴ.

II. LOW-VOLTAGE DSB OP AMP CONFIGURATION

Figure 1 shows a configuration of an LV DSBFC OP Amp, in which the power supply voltages (±1.5 V) were reduced to 60 % of the previous ones (±2.5 V). The DSB method is also used for implementing low power consumption. When the power supply voltage is simply reduced, their gains are restrained and bandwidth becomes low. So, in the newly developed circuit, each FET (Field Effect Transistor) size of the LV DSBFC OP Amp was optimized to achieve high-speed switching operation of 14.3 MHz. This OP Amp has a DSB circuit suitable for low power dissipation and an FC OP Amp to achieve a wide dynamic range even in low power supply voltages. The DSB

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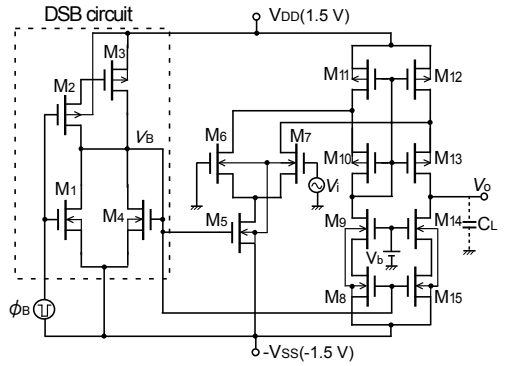

Figure 1. Configuration of the low-voltage DSBFC OP Amp.

TABLE Ⅰ. LOW-VOLTAGE DSBFC OP AMP DESIGNED VALUES.

FET	W/L (μm/μm)	FET	W/L (μm/μm)
M_1	15/2.5	M_6, M_7	2000/2.5
M_2	30/2.5	M_8, M_{15}	92/2.5
M_3	50/4	M_9, M_{14}	1055/2.5
M_4	44/6	M_{10}, M_{13}	2000/2.5
M_5	187/2.5	M_{11}, M_{12}	390/2.5

circuit consists of a bias circuit of M_1-M_4. The FC OP Amp consists of a current mirror of M_{10}-M_{13} and current sources of M_8, M_9, M_{14}, and M_{15}. The current sources M_5, M_8, and M_{15} of the FC OP Amp are controlled by switching a bias voltage V_B of the DSB circuit dynamically from V_B* to -1.5 V to reduce the power consumption still more. Table Ⅰ shows its designed values. A minimum channel length of p-MOS FETs and n-MOS FETs is 2.5 µm. In order to achieve almost the same transconductance g_m as that in the conventional 5-V power DSBFC OP Amp, a channel width W of M_{11} and M_{12} and that of M_{10} and M_{13}, in p-MOS current mirror circuits, were increased by nearly fourfold and twofold, respectively. Each W of n-MOS current sources M_9, M_{14}, M_8, and M_{15} was increased by nearly one and a half. The bias voltage of V_B* at the on state of the FC OP Amp was adjusted to nearly 0 V (larger than the conventional one) to decrease W of the current source M_5 maintaining a high switching speed of the DSB circuit. W of M_1-M_3 was increased by over twofold. W of M_4 was adjusted to an optimum value. The bias voltage Vb of the current source consisting of M_9 and M_{14} was set at 0.15 V.

In the DSB circuit, when an external control pulse ϕ_B driving an inverting switching circuit of M_1-M_4 is -1.5 V, the OP Amp turns on by setting V_B at an appropriate level of nearly 0 V by enabling M_3 and M_4 to operate in the saturation region, and operates normally as an operational amplifier. Conversely, when ϕ_B becomes 1.5 V, the OP Amp turns off by setting V_B at nearly -1.5 V, enabling M_1 to operate in a low impedance and M_3 in a high impedance. This high impedance status of M_3 occurs because the gate of M_3 is set at a potential determined by the capacitive coupling between gate and source of M_2 and between gate and drain of M_3 at the transition of ϕ_B to 1.5 V. Therefore, the OP Amp does not dissipate power at all during this off period, which brings about low power consumption.

TABLE Ⅱ. TYPICAL PERFORMANCES FOR THE LOW-VOLTAGE 3-V POWER AND CONVENTIONAL 5-V POWER DSBFC OP AMPS. C_L=1 PF.

Performance parameters	3V power DSBFC OP Amp - this work	5V power DSBFC OP Amp
Power supply voltages	±1.5 V	±2.5 V
Switching frequency *fs*	14.3 MHz	14.3 MHz
Open loop gain Ao	47.1 dB	51 dB
Phase margin θ	32.8 degrees	34.2 degrees
Unity gain frequency *fu*	603.7 MHz	709 MHz
Slew rate SR (C_L=10 pF)	131 V/µs	140 V/µs
Settling time ts	10 ns	12 ns
Distortion THD (*fin* =10 kHz, *Vo* =0.6 Vp-p)	0.73%	0.40%
Power dissipation (C_L=5 pF) in 50 % switching duty ratio	9.3 mW	16.3 mW

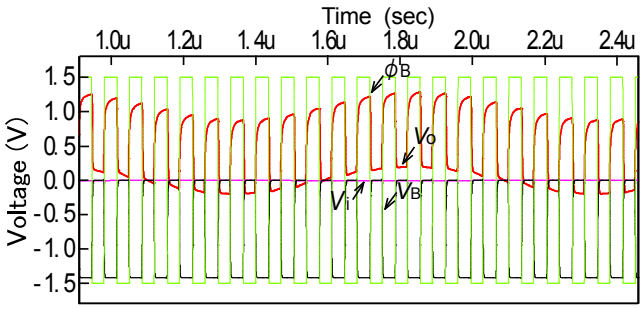

Figure 2. Simulation waveforms of the low-voltage DSBFC OP Amp. Input signal frequency f_{in}=1 MHz, V_{in}=1 mV, *fs*=14.3 MHz, C_L=2 pF.

Ⅲ. SIMULATION RESULTS

The LV DSBFC OP Amp performance was tested through SPICE simulations. The power supply voltages V_{DD} and Vss are 1.5 V. Typical performances compared with those of the conventional DSBFC OP Amp with a power supply of 5 V are shown in Table Ⅱ. The values of parameters of open loop gain, phase margin, unity gain frequency, slew rate, and settling time are almost the same as those in the conventional 5-V power DSBFC OP Amp. As the inherent static nonlinearity of the LV DSBFC OP Amp, the total harmonic distortion THD for the 10 kHz input signal, enabling 0.6 Vp-p to output, was 0.73 %, which is a little large compared to the conventional one. However, this is less than 1 %.

The LV DSBFC OP Amp operated in a dynamic switching mode with a Duty Ratio (DR) of 50 % and a switching frequency, *fs*, of 14.3 MHz as shown in Figure 2. The output sine wave voltage for the input signal of 1 mV was nearly equal to that in the static operation mode of this OP Amp. Like this, the distortion by the dynamic operation seems to be hardly seen. In the dynamic switching operation mode of 50 % duty ratio, the power dissipation was 9.3 mW, which is 66 % of that observed in the static operation mode as shown in Figure 3. This is also 57 % of that of the conventional 5-V power DSBFC OP Amp. This shows this OP Amp's extremely low power consumption characteristics due to the reduced effect of power supply voltages (60 % of that in the

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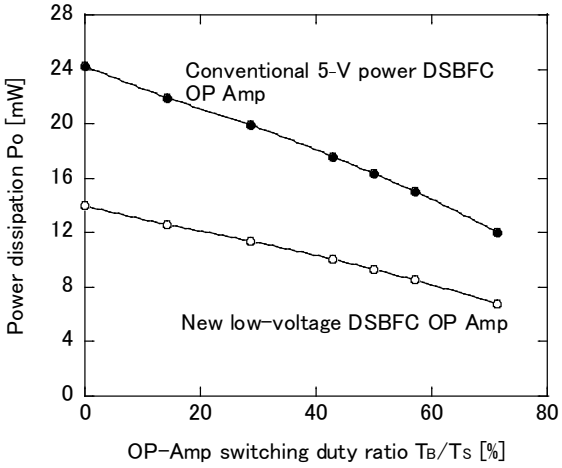

Figure 3. Power dissipation vs. OP-Amp switching duty ratio in the DSB mode. fs=14.3 MHz, C_L=5 pF.

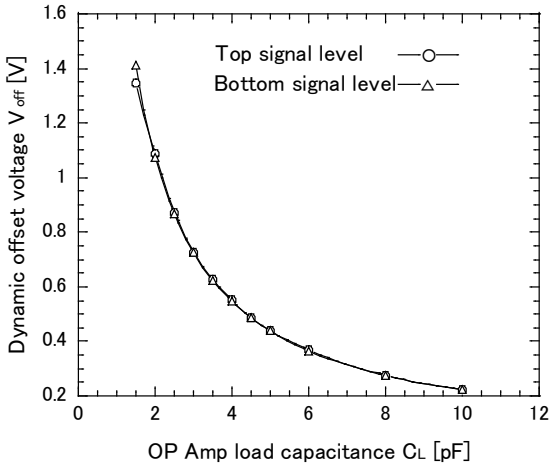

Figure 4. Dynamic offset voltage vs. OP Amp load capacitance in the LV DSBFC OP Amp. f_{in}=0.5 MHz, V_{in}=1 mV.

conventional 5-V power DSBFC OP Amp) and dynamic switching operation.

The LV DSBFC OP Amp switches dynamically to the off state. At this time, though p-MOSFETs M11 and M12 remain the on-state, MOSFETs M6, M7, M9, M10, M13, and M14 change to the on-state weakly. The output terminal of *Vo* of the OP Amp is set at a voltage depending on the load capacitance through the capacitive coupling between the drain and the gate of the MOSFET M13. So, a large output swing in *Vo* occurs at the off-state transition. A dynamic offset voltage Voff (defined as the difference of the on-state and the off-state output voltages) at the off-state transition of the OP Amp vs. load capacitance C_L was tested (Figure 4). In small load capacitances less than 1.5 pF, top and bottom signal levels of the dynamic off swing do not match. This causes distortion at an output signal of the OP Amp. Therefore, we can see that the load capacitance C_L over 2 pF is desirable for its operation.

Ⅳ. APPLICATION TO SC LPF

To demonstrate the practicability of the above low-voltage DSBFC OP Amp, the feasibility of its application in a 2nd-order SC IIR (Infinite Impulse Response) LPF with the Butterworth frequency characteristic was tested. When a sampling frequency fs=14.3 MHz (equal to four times of NTSC (National Television System Committee) color sub-carrier frequency 3.58 MHz) and a cutoff frequency fc=2 MHz, respectively, were chosen for this LPF, the discrete-time transfer function is given by [10]

$$H(z) = -\frac{0.1174(1+z^{-1})^2}{1-0.8252z^{-1}+0.2946z^{-2}}. \quad (1)$$

The circuit configuration and operation waveforms realizing this transfer function are shown in Figures 5 and 6, respectively [10]. This filter consists of a sample-hold circuit with a holding capacitor C_1 and a CMOS sampling switch controlled by ϕ_{SH}, CMOS switches ϕ_1, ϕ_2 for charge transfer, capacitors A-E, G, and I, and two LV DSBFC OP Amps (OP Amps 1 and 2). The sampling switch was designed to a channel width / channel length W/L=105/2.5 (μm/μm) for each of p-MOSFET and n-MOSFET. Other CMOS switches were designed to 75/2.5 (μm/μm). CMOS switches are turned on and off by non-overlapping two-phase clock pulses ϕ_1, ϕ_2, swinging from -1.5 V to 1.5 V. These sampling and CMOS switches were designed to have a balanced structure with each equal L and W of p-MOS and n-MOS FETs to delete a feed-through phenomenon. This phenomenon is easy to be caused by a capacitive coupling between gate and output terminals.

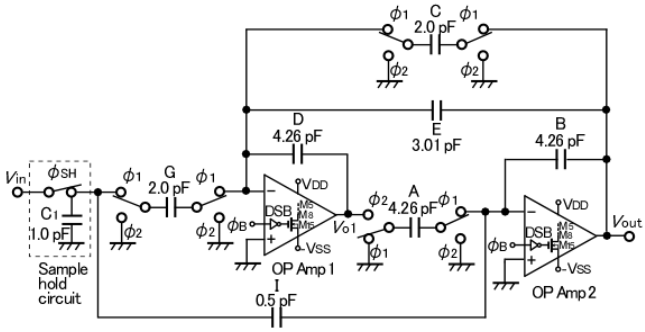

Figure 5. Configuration of the 2nd-order SC LPF.

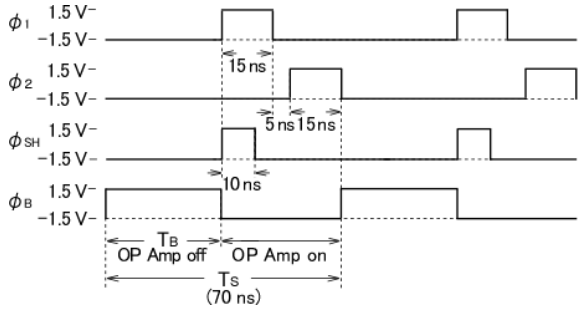

Figure 6. Operation waveforms of the 2nd-order SC LPF.

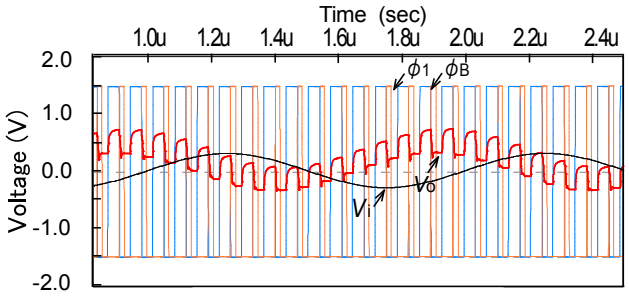

Figure 7. Simulation waveforms for the 2nd-order SC LPF. V_{in}=0.3 V_0-p, f_{in}=1 MHz, C_L=4 pF.

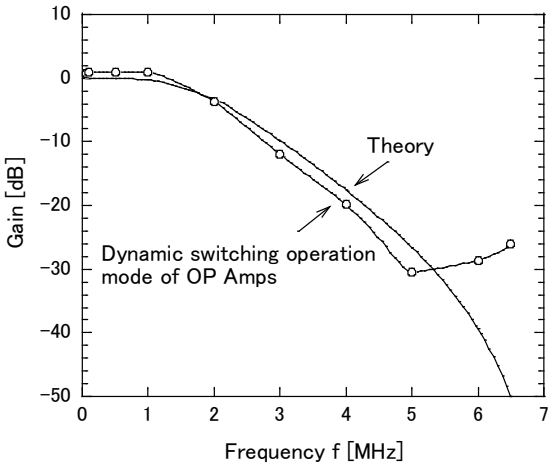

Figure 8. Frequency response of the SC LPF in the DSB mode of the OP Amp. T_B=35 ns.

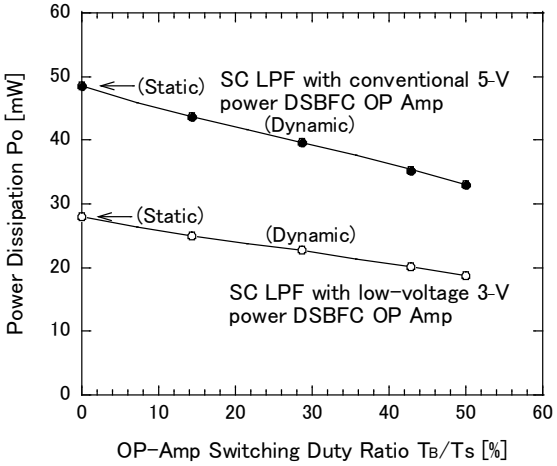

Figure 9. Power dissipation vs. OP Amp switching duty ratio in the 2nd-order SC LPF. f_{in}=1 MHz.

Major CMOS process parameters are given as a gate insulating film thickness t_{ox}=50 nm, a p-MOSFET threshold voltage V_{TP}=-0.6 V, and an n-MOSFET threshold voltage V_{Tn}=0.6 V.

Operation waveforms for an input signal of 1 MHz with an amplitude of 0.3 V and an output load of 4 pF are shown in Figure 7. In the dynamic switching operation, an output load of the LV DSBFC OP Amp increases to nearly 5 pF including internal capacitances of the SC LPF. For the pass-band frequency signal (≦2MHz), almost the same signal as the input one was obtained. The frequency response of the SC LPF in the dynamic switching operation of the LV DSBFC OP Amp is shown in Figure 8. The frequency response was near the theoretical one from 100 kHz to near 5 MHz. In the high frequency range over 6 MHz, it deteriorated due to a sampling phase effect. The gain below -26 dB was obtained at over 6 MHz within a stop-band. Though this stop-band gain is not enough, it is expected to be improved by making the roll-off steeper through the increase of filter order.

Power dissipation vs. OP Amp switching duty ratio in the 2nd-order SC LPF is shown in Figure 9. The power dissipation of the SC LPF itself decreased in proportion to the off period T_B of the OP Amp. In the dynamic switching operation mode of T_B=35 ns (DR=50 %), the power dissipation of the SC LPF (18.7 mW) was reduced to 66.8 % as compared to that in the static operation of the OP Amps (28.0 mW). Thus, the dynamic switching operation of the LV DSBFC OP Amp is useful for reducing the power dissipation of the SC LPF. This power dissipation was 56.8 % compared to that in the SC LPF using the conventional 5-V power DSBFC OP Amp (32.9 mW). This low power characteristic was realized by the low power supply voltages and dynamic switching operation.

V. Conclusions and Future Work

A high-speed low-voltage Folded-Cascode (FC) OP Amp with a Dynamic Switching Bias (DSB) circuit capable of processing video signals, which enables low power consumption, high gain with wide bandwidths, and a wide dynamic range, was proposed. Through simulations, it was shown that the OP Amp with the reduced 3-V power supply is able to operate at a 14.3 MHz dynamic switching rate, allowing processing video signals, and a dissipated power of 57 % compared to that in the conventional 5-V power DSBFC OP Amp while keeping a 0.6 V wide output dynamic range. The response of the 2nd-order Switched Capacitor Low-Pass Filter (SC LPF) tested as its application was near the theoretical frequency response within frequencies below 5 MHz. The power dissipation of this LPF was also reduced to 56.8 % of that in the SC LPF with the conventional 5-V power DSBFC OP Amp.

Thus, it was confirmed that the 3-V power DSBFC OP Amp is useful for high speed operation, low power consumption, and greatly reducing the power dissipation of the SC LPF. This circuit should be useful for the realization of low-power wide-band signal processing ICs. It is also noteworthy that the performance is expected to be improved still more by employing MOSFETs with a minimum shorter channel length than 2.5 μm used in this work.

As the future work, the study on the increase of the filter order remains, because the frequency response will be improved to a practical level by increasing this one. However, there might be a limitation in the filter order, because two OP Amps per one order LPF must be used and so power dissipation will increase in proportion to the filter order.

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