Integrated Sensor System for Signal Conditioning, Digitization and Interfacing for Terahertz Bolometric Camera

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***Abstract*—This work is about designing an integrated system to capture, partially process and digitalize data from a terahertz bolometric antenna array. Different techniques for achieving the required operation are presented, including a low noise amplifier with a custom lateral bipolar p-n-p structure as input stage and other strategies to reject noise, and integration of analogue signal processing into Analogue-to-Digital Converter (ADC). The results of the bipolar structure characterization are presented in great detail, demonstrating the feasibility of using them in an amplifier.**

Keywords-lateral bipolar transistor; low-noise amplifier; terahertz bolometric camera; custom CMOS structure.

I. INTRODUCTION

The one-dimensional terahertz camera uses a pulsed 50% duty cycle source of electromagnetic waves with frequency between 0.08 and 1 THz and in-house designed and manufactured bolometers, precisely designed resistors bonded to THz micro antennas, that are sensitive to these frequencies [1][2]. The camera is designed for industrial applications where high image rate is required. Typically, objects are flying past the camera at speeds up to 20 m/s and need to be imaged with precision in the range of millimetres, requiring sample rates in the range of 20 kS/s [3].

Due to the nature of bolometers, sensor value acquisition must be synchronised with the terahertz source duty cycle to correctly detect peak-to-peak values (between source being on and off). The effective pixel value is the difference between these two acquired values.

The currently used system uses an Application-Specific Integrated Circuit (ASIC) with custom designed Low-Noise Amplifiers (LNA), Successive Approximation Register (SAR) ADCs for early digitalization and Field-Programmable Gate Array (FPGA) unit for processing and interfacing. Early digitalization is a trend in the sensor industry but, with the ever-increasing number of pixels, the data rates and processing power requirements are becoming too high and too expensive. It currently takes 8 16-bit ADC conversions per one pulse of terahertz source, which are then averaged and subtracted to get one sample value for one pixel. With several hundred sensors at 20 kS/s, it becomes a costly challenge for the FPGA interface.

Designing a single chip sensor interface as for regular complementary metal–oxide–semiconductor (CMOS) camera sensors is not feasible; pixels are a couple of millimetres apart, stretched over wide areas and we can only interface a few pixels with one chip. Therefore, distributed processing is required, to minimise the amount of data that goes to the interface unit.

Section 2 of this work describes the proposed updates of the system; Section 3 demonstrates some preliminary results of system simulations and test structures measurements and Section 4 summarizes the findings.

II. UPDATED SYSTEM DETAILS

The novel proposed system joins an improved LNA, a circuit for analogue processing of the amplified signal and an integrated capacitive SAR ADC on a single ASIC. The camera would be composed of several ASICs which would be interfaced through a simplified central system with a microprocessor or FPGA (Fig. 1).

The LNA is improved by introducing a bipolar input stage, as it is not a victim to 1/f shot noise and helps in reducing the white noise level. Unlike for CMOS transistors, noise is not dependent on the bipolar transistor size. Therefore, the new LNA is expected to utilize a fraction of the silicon area used by the existing LNA. Designing a bipolar stage is, however, a challenge of its own as a regular bipolar transistor cannot be fabricated in the preferred 0.35 µm CMOS technology due to layer availability, or has the collector permanently connected to the substrate, making it useless. Fortunately, there is an option to create a lateral p-n-p structure which has two collectors, one (horizontal) still permanently connected to substrate and the other (lateral) available for active load connection (Fig. 2). Initial Spice simulation model parameters for the structure have been borrowed from a similar CMOS technology of a different

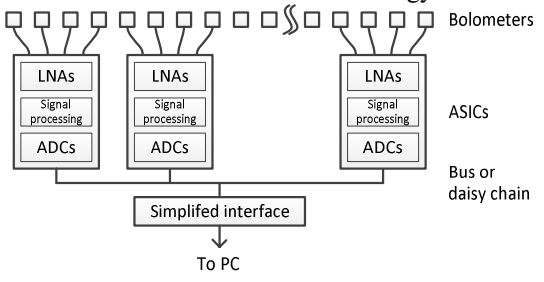

Figure 1. Proposed system

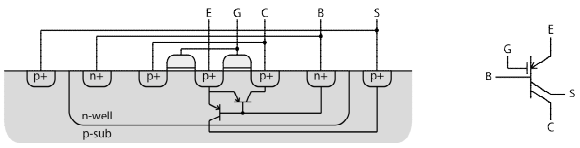

Figure 2. Lateral p-n-p structure

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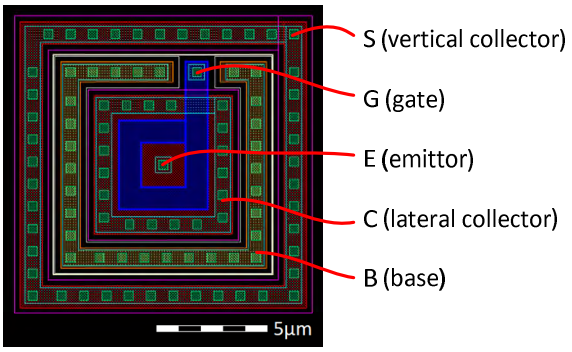

Figure 3. Layout diagram for lateral p-n-p structure

semiconductor foundry and will be later updated to better match the results of the test structures (Fig. 3) to be then used in simulations of LNA.

The analogue signal processing circuit is partially integrated into ADC and allows it to directly digitize peak-to-peak values of the amplified signal from the bolometers. A SAR ADC usually samples signal and reference simultaneously in its capacitors, while here it is set to sample the bottom peak as reference in the first half of the period and the top peak as signal in the second half. The rest of the processing circuit is a configurable low-pass filter, used to minimise noise with lowest impact on signal, so that we can avoid oversampling and possibly lower requirements for the number of bits.

III. Results and Discussion

Testing of lateral p-n-p test structures showed promising results compared to the existing Spice model (Fig. 4). We tried two slightly different layouts of which one (Q1) appears to be more stable over V_{BC} voltage with beta factor around half of expected value, while the second (Q2) shows much better beta factors at higher currents, but varies a lot with V_{BC}. In an amplifier, a number of transistors would be connected in parallel, allowing utilisation of higher beta factors at lower currents through single transistors. The grey area in Fig. 4 marks the planned single-transistor collector current – it would be a compromise between total collector current, silicon area and highest beta. The samples still require more detailed characterisation, but designing a third layout that is between these two seems as a reasonable idea to get a better compromise.

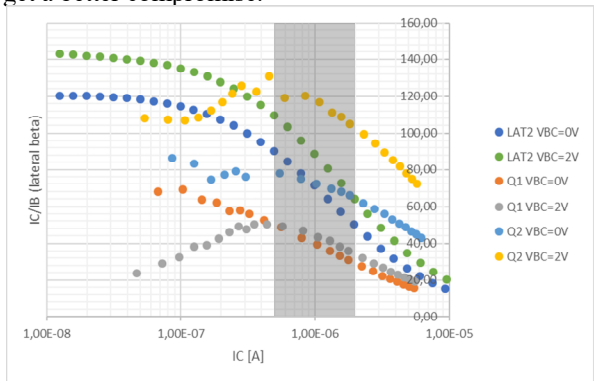

Figure 4. Measurement results for beta of lateral transistor

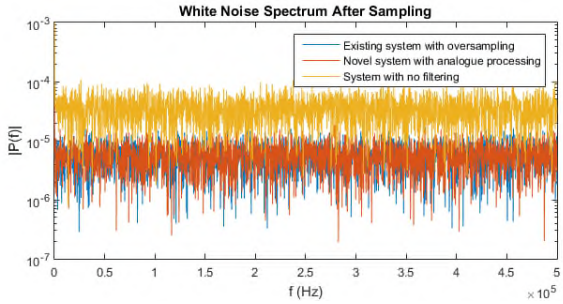

Figure 5. Noise comparison of systems with digital and analogue signal processing, and with no filtering

Noise results are incomplete at this point, but we are expecting white noise with level inversely proportional to the collector current.

Simulink simulations of analogue processing show noise levels comparable to digital with oversampling. The correct settings of analogue low-pass filter are required. By varying the filter edge frequency, we could either let more noise pass through, lower the signal, or even introduce pixel retention noise. When the filter is set correctly, the noise rejection in our proposed system is very similar to the digital system, when we compare them to a system with no filtering, as seen in Fig. 5.

Our findings suggest that we will need to trim these filters to adapt them to the desired sample rate and possibly compensate for the process spread of integrated components (resistors, capacitors).

IV. Conclusion

With this work, we have demonstrated that the novel system with analogue processing is feasible and would significantly reduce hardware cost of the terahertz camera. This is done by more means: integrating ADCs on chip, reducing the amount of digital data, optimizing data connections to the interface and replacing powerful FPGA with a simpler interface.

At the same time, we have shown that the performance of the system will not be compromised but rather improved with better noise characteristics of the new LNA.

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