High-precision Time Synchronization Digital Sensing Platform Enabling Connection of a Camera Sensor

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Abstract - **The authors are conducting research and development of different types of sensor systems for the maintenance of civil infrastructures, such as aging bridges and highways, and buildings. Highly accurate time information is added to measurement data, and a set of sensing data that ensures time synchronization is acquired and used for multimodal analysis of risk. In research so far, as a first step, a sensor device was developed that uses a digital high-precision accelerometer to perform highly-accurate time-synchronized sensing of civil infrastructure, such as bridges and highways, and buildings. A vibration table test was performed on the new sensor device, and its time synchronization performance was verified by comparing the measurement results with multiple sensor devices and a servo-type accelerometer. In this paper, a different type of digital sensing platform has been developed that allows a camera sensor to be connected in addition to a digital accelerometer. By adding a unified time stamp synchronized with the absolute time to data from the digital accelerometer and the image from the camera sensor when data is acquired, the vibration and the image can be measured synchronously. First, a Chip-Scale Atomic Clock (CSAC), which is an ultra-high-precision clock, is mounted on the sensor device, and a mechanism is implemented whereby a time stamp is added to the outputs of the digital accelerometer and the camera sensor with timekeeping precision. Since the timekeeping precision of the CSAC is too high, a delay occurs when a time stamp is added by the CPU of the sensor device. Therefore, a Field-Programmable Gate Array (FPGA) dedicated to adding time stamps is prepared. In this paper, the results of a performance verification experiment on a camera sensor mounted on the platform, are described.**

Keywords-Time Synchronization; Chip Scale Atomic Clock; Earthquake Observation; Structural Health Monitoring; Micro Electro Mechanical Systems; Camera Sensor

I. INTRODUCTION

As civil infrastructure, such as bridges and highways, and buildings deteriorate over time, it has become important to automate inspections for maintenance of these structures. In addition, since there are many disasters, such as earthquakes and typhoons in Japan, it is necessary to detect damage to structures immediately after a disaster, and to estimate the damage situation. Data collection and analysis by sensor groups is effective for automating the detection of such abnormalities, but to analyze data sets measured by multiple sensors and evaluate structural safety, time synchronization between sensors is required.

The authors applied wireless sensor network technology to develop sensors for seismic observation and structural health monitoring, and demonstrated their performance in skyscrapers [1][2]. In this system, time synchronization was achieved by sending and receiving wireless packets between sensors [1]. However, it is impossible to target multiple buildings, long structures, such as bridges, and wide-area urban spaces with wireless sensor network technology. On the other hand, if sensors installed in various places can autonomously retain accurate time information, this problem can be resolved. The method of using GPS signals is effective outdoors, but it cannot be used inside buildings, underground, under bridges, or in tunnels, etc.

Therefore, the author developed a sensor device that autonomously retains accurate time information using a Chip-Scale Atomic Clock (CSAC) [3]-[5], which is an ultra-high-precision clock [6]-[8]. In order to apply the developed sensor device to earthquake observation, a logic was implemented that detects the occurrence of an earthquake and saves data on earthquake events, and its function was verified in a vibration table experiment [9]. The developed sensor device was also installed in an actual building and on an actual bridge, and used for seismic observation and evaluation of structural health [10]. However, as the developed sensor device had an analog MEMS accelerometer, it was difficult to measure minute vibrations accurately, and there was a risk of noise being mixed with the analog signal. The risk of noise was therefore eliminated by making the accelerometer mounted on the sensor device a digital type. In this paper, a different type of digital sensor platform is further developed wherein a camera sensor can be connected to the sensor device. The details of the digital sensing platform and a mechanism whereby ultra-high-accuracy time information is added to sensor data by the CSAC, are described. The results of experiments performed to verify the time synchronization performance of the camera sensor are also reported.

In this paper, Section II shows the existing time synchronization methods and describes their problems and achievement of the development of digital sensing platform proposed in this research. Section III describes the configuration of digital sensing platform and the development of the actual sensor device. Further, Section IV describes the performance verification experiments on the time

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synchronization of developed camera sensor device, and it is confirmed that time synchronization among the developed digital sensor devices with camera is achieved.

II. STATE OF THE ART

A time synchronization function is indispensable for sensor devices used to monitor structural health and make seismic observations of civil infrastructure, such as bridges and highways, and buildings. This is because time series analysis using phase information cannot be performed unless a data set is obtained in which time synchronization is achieved. Regarding time synchronization of sensing, many studies have already been performed, such as the use of GNSS signals from artificial satellites and the Network Time Protocol (NTP) for time synchronization on the Internet [11]. There are also studies where time synchronization is achieved by utilizing the characteristic of wireless sensor networks that propagation delay is small. For example, time synchronization protocols, such as Reference Broadcast Synchronization (RBS), Timing-sync Protocol for Sensor Networks (TPSN), and Flooding Time Synchronization Protocol (FTSP) are being studied [12]-[16].

However, although time synchronization using wireless technology is highly convenient, wireless communication may not always be possible. Particularly, if wireless communication is interrupted during an earthquake, it will not be possible to perform sensing where time synchronization is guaranteed. A technology that realizes highly accurate time synchronization in a room includes IEEE1588 Precision Time Protocol (PTP). PTP uses an Ethernet cable in a general Local Area Network (LAN) as a transmission line, and achieves accurate synchronization within one microsecond using time packets. However, it has many problems. For example, it is difficult to achieve stable synchronization accuracy due to packet delay fluctuation and packet loss due to congestion in the LAN. Moreover, since the delay is corrected by packet switching, the PTP devices that can be connected to the master device are limited, and it cannot be deployed in a Wide Area Network (WAN) environment where the delay amount varies drastically.

To obtain a set of sensor data that guarantees long-term, stable time synchronization even when GPS signals are not available, wireless transmission/reception is unstable, and wired network connection is not possible, it would be ideal if different sensors autonomously retain accurate time information. If accurate time information could be added to the data measured by each sensor, a sensor data set that guarantees time synchronization would be obtained. It was therefore decided to develop a sensing system that autonomously retains accurate time information by employing a CSAC [4]-[6], which is a clock with high timekeeping accuracy. The CSAC is a clock that achieves ultra-high-accuracy time measurement to several tens of picoseconds (5 x 10^{-11} seconds), while having an ultra-small external shape that can be mounted on a board. Development began in 2001 with the support of the US Defense Advanced Research Projects Agency (DARPA), and consumer products were launched in 2011.

Applications include measures against GPS positioning interference by jamming signals, high-precision positioning by installing on smartphones, etc., and high-level assessment of disaster situations, and further price reduction is expected as it becomes more widespread. CSAC has a small error of about 4 to 8 orders of magnitude less than that of timekeeping by a crystal oscillator, and time synchronization by NTP or GPS signals. If this CSAC is installed in each sensor device and a mechanism is implemented that gives a highly accurate time stamp to sampling of the data to be measured, sensor data sets that guarantee time synchronization can be collected even if GPS signals cannot be used, wireless transmission/reception is unstable, and wired network connection is unavailable. In development so far, the sensor device had a MEMS accelerometer, and the system configuration allowed for any analog sensor to be connected via an external input interface.

However, as the accuracy of the analog MEMS accelerometer is not high, noise might still be mixed with the analog signal, and it was desired to be able to connect a camera sensor, which is a type of digital sensor, it was decided to develop a new platform with full digital sensing. Specifically, a technology was developed to mount a digital accelerometer on the sensor device to enable high-precision acceleration measurement without the risk of noise contamination, connect a camera sensor, and assign accurate time stamps by CSAC to both digital outputs. Data sets obtained by the sensor device described in this paper, where time synchronization is guaranteed, can be used to analyze the structural health of civil infrastructure and buildings, and understand seismic phenomena.

III. DIGITAL SENSING PLATFORM AND CIRCUIT CONFIGURATION

An ordinary sensor device consists of a CPU, a sensor, a memory and a network interface, and a crystal oscillator is used for the CPU. If a CSAC is mounted on such a sensor device to correct the time information of the CPU and perform measurement, a delay will occur because the timing accuracy of the CSAC is too high. Therefore, in order to directly add time information by the CSAC to the measurement data of the sensor in terms of hardware, a mechanism utilizing a Field-Programmable Gate Array (FPGA), which is a dedicated integrated circuit, was contrived. As a result, the CPU of the sensor device is not overloaded, and it became possible to save measurement data to which time information is added by the FPGA in a memory, and to collect the data via a network. Moreover, since the FPGA is programmable, it can not only handle CSAC time information, but also incorporate logic, for example to detect abnormalities, etc., using the measurement data. In this paper, a mechanism is developed whereby accurate time stamps by the CSAC are added to the outputs of the digital accelerometer and camera sensor.

3.1 System Configuration

As shown in Figure 1, the sensor device in this research consists of an oscillator board that synchronizes GPS Time (GPST) with the CSAC and supplies a stable reference signal, a sensor board on which a digital accelerometer and external analog sensor input interface are mounted, a signal processing

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board on which a CPU and FPGA are mounted, and a camera that captures images. A high-precision 10 MHz reference clock and one Pulses Per Second (PPS) signal are supplied by the oscillator board, and a time stamp and trigger signal for acquiring data are generated by the FPGA. The sensor board is provided with the digital accelerometer and external analog sensor input interface. Any analog sensor can be connected to the external analog sensor input interface.

The digital accelerometer outputs data according to the trigger signal via a Universal Asynchronous Receiver/Transmitter (UART). The data of the sensor connected to the external analog sensor input interface is converted by an A/D converter according to the trigger signal, and output as a 16-bit serial value. The camera sensor can release the shutter according to the trigger signal, and outputs it as an RGB value. The data thus acquired is saved in a connected storage (SSD). The sensor device is operated via a wired LAN, Wi-Fi, or USB.

3.2 Oscillator board

The configuration and external appearance of the oscillator board are shown in Figures 2 and 3. The oscillator board has a function to synchronize the CSAC with 1 PPS output by the GPS module or 1 PPS input from outside. When time synchronization is required between multiple sensor devices, all the sensor devices are designated as "master", or one sensor device is designated as a "master" and the other sensor devices are designated as "slave". When the sensor device is a master, GPS and the CSAC are synchronized by receiving GPS signals, and inputting 1 PPS obtained from the GPS module to the CSAC. When the sensor device is a slave, the master and slave are synchronized by inputting 1 PPS output by the master. In addition, commands for setting the CSAC synchronization cycle or resetting the phase value, as well as signal selection commands, are executed by the signal processing board through the connector. The 10MHz and 1 PPS output by this board are clock sources for this system.

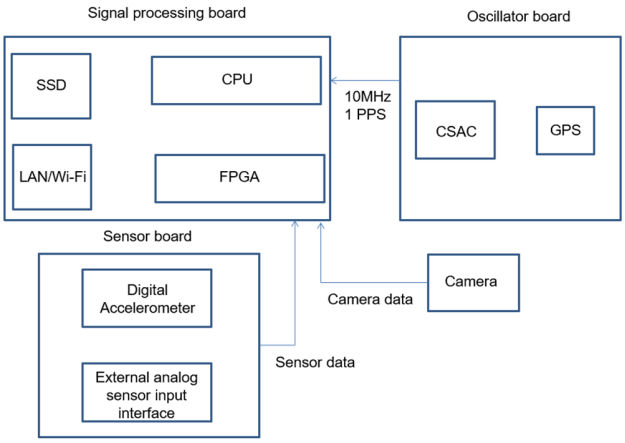

Figure 1. System configuration.

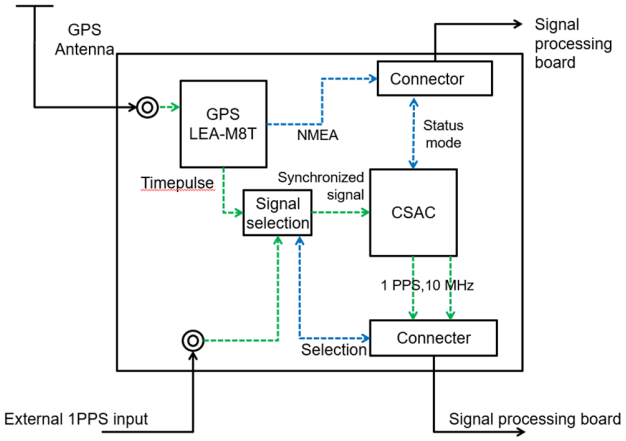

Figure 2. Oscillator board configuration.

Figure 3. External appearance of the oscillator board.

3.3 Sensor board

The configuration and external appearance of the sensor board are shown in Figures 4 and 5. The sensor board is provided with a digital accelerometer and an external analog sensor input interface. The data obtained by the digital accelerometer can be sampled at the timing of the trigger. For the external analog sensor input interface, three channels are provided assuming that a servo-type analog accelerometer is connected for comparison with the digital accelerometer. Depending on the measurement purpose, any analog sensor can be connected in addition to an analog accelerometer.

The signal input from the external analog sensor interface is converted by the A/D converter to output as a 16-bit serial value. Note that the signal is split into two paths, and one of them is amplified 64 times. Therefore, even with an A/D converter having a resolution of 16 bits, a resolution equivalent to 22 bits can be obtained. The data obtained by the digital accelerometer is output by the UART, and the data obtained by the sensor connected to the external analog sensor input interface is output by a Serial Peripheral Interface (SPI), both to the signal processing board.

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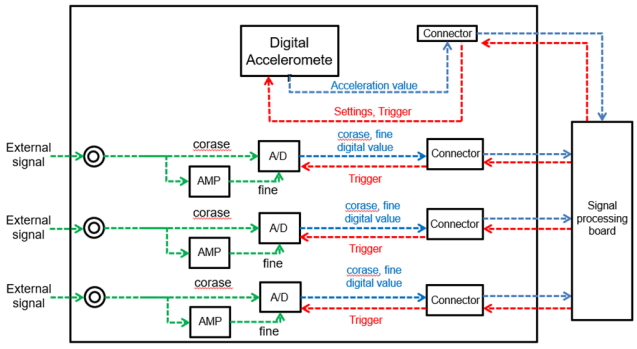

Figure 4. Sensor board configuration.

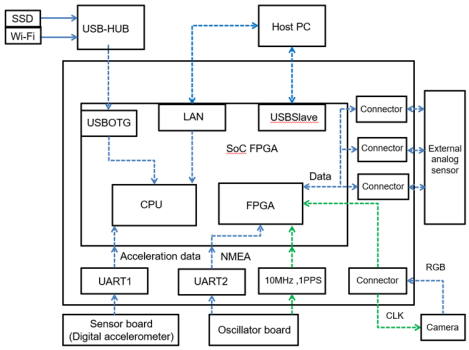

Figure 6. Signal processing board configuration.

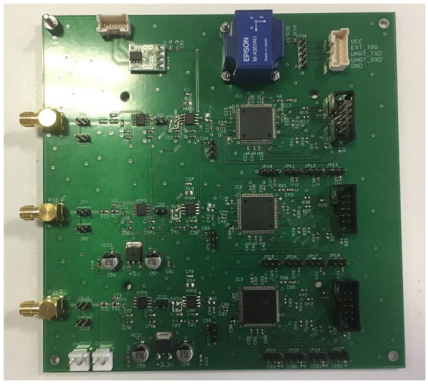

Figure 5. Sensor board.

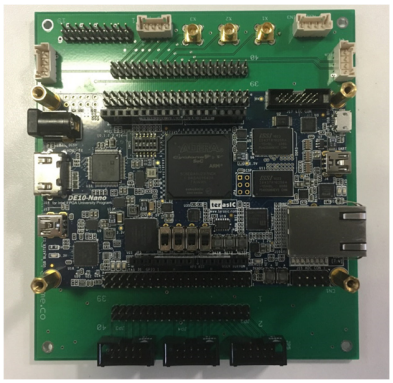

Figure 7. Signal processing board.

3.4 Signal processing board

The configuration and external appearance of the signal processing board are shown in Figures 6 and 7. The FPGA shown in Table 1 is mounted on the signal processing board. As shown in Table 1, Ubuntu is installed as the OS of the CPU and Cyclone V is installed in the FPGA, enabling the use of 1 GB of SDRAM. Also installed is a USB On-The-Go (USB OTG), and it is possible to be connected to an SSD and a Wi-Fi antenna which are extension devices. The Samba function can be used to acquire and browse built-in data via a LAN, and Secure Shell (SSH) allows to perform operations, such as settings and starting measurement. In addition, since it has a USB slave function, it can be operated via USB even when a LAN cannot be used. In addition to the above functions, the CPU mainly performs time setting, sorting of acquired data, format conversion, and filing. The FPGA adjusts the internal RTC (real-time clock), and generates the trigger signal based on the clock obtained from the oscillator. It also constitutes a data acquisition block for the various sensors and camera.

3.5 Digital accelerometer

The external appearance and specifications of the digital accelerometer mounted on the sensor board are shown in Figure 8 and Table 2, respectively. The on-board digital MEMS has a built-in 3-axis crystal accelerometer with high precision and stable performance manufactured by finely processing a crystalline material with superior precision and stability. As shown in Table 2, high-resolution vibration measurement with low noise and low power, is possible.

TABLE I. SPECIFICATIONS OF MAIN FPGA AND DE10-NANO(CPU)

Model	DE10-NANO
OS	Ubuntu 16.04.6 LTS (GNU/Linux 4.5.0-00185-g3bb556b armv7l)
CPU	800MHz Dual-core ARM Cortex-A9
Memory	1GB DDR3 SDRAM
LAN	1 Gigabit Ethernet PHY with RJ45 connector
USB	USBOTG×1, USBUART×1
UART	UART×2
FPGA	CYCLONE V
FPGAROM	EPCS64
Storage	16GB (MicroSD)

Figure 8. Digital Accelerometer.

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TABLE II. SPECIFICATIONS OF DIGITAL ACCELEROMETER

Model	EPSON M-A351AS
Range	±5 G
Noise Density	0.5 μG/√Hz (Average)
Resolution	0.06 μG/LSB
Bandwidth	100 Hz (selectable)
Output Range	1000 sps (selectable)
Digital Serial Interface	SPI
Outside Dimensions (mm)	24 × 24 × 18
Weight	12 grams
Operating Temperature	-20 ℃ to +85 ℃
Power Consumption	3.3 V, 66 mW
Output Mode Selection	Acceleration, Tilt Angle, or Tilt Angle Speed

3.6 Camera sensor

The external appearance and specifications of the camera sensor are shown in Figure 9 and Table 3, respectively.

Figure 9. Camera sensor.

TABLE III. SPECIFICATIONS OF CAMERA SENSOR

Model	OmniVision OV5642
Active Array Size	2592 x 1944
Power Supply	core: 1.5VDC±5%, analog: 2.6-3.0 V, I/O: 1.7-3.0 V
Temperature Range	operating: -30 ℃ to +70 ℃ stable image: 0 ℃ to +50 ℃
Output Formats (8-bit)	YUV(422/420)/YCbCr422, RGB565/555/444, CCIR656, 8-bit compression data, 8/10-bit raw RGB data
Lenz Size	1/4”
Input Clock Frequency	6-27 MHz
Shutter	rolling shutter
Maximum Image Transfer Rate	5 megapixel (2592x1944): 15 fps 1080p (1920x1080): 30 fps 720p (1280x720):60fps VGA (640x480): 60 fps QVGA (320x240): 120 fps
Scan mode	progressive
Maximum Exposure Interval	1968 x t_{ROW}
Pixel Size	1.4 μm x 1.4 μm
Image Area	3673.6 μm x 2738.4 μm

OmniVision OV5642, which is a CMOS camera module, is used as the camera sensor. It is compact, has low power consumption, supports digital data (YUV422) output, performs very well in poorly lite environments, and can acquire images at the timing of a trigger by inputting an external trigger.

IV. PERFORMANCE VERIFICATION EXPERIMENT ON THE TIME SYNCHRONIZATION FUNCTION OF CAMERA SENSOR

A performance verification experiment was carried out on the time synchronization function of the camera sensor. The experimental system configuration is shown in Figure 10. The trigger signal generated by the signal processing board is transmitted to the camera sensor and the FPGA of the LED control simultaneously. Since the shutter of the camera sensor and the lighting of the LEDs are synchronized, if the image can be acquired when the LEDs light up, it is considered that the image acquired is synchronized with the trigger. The FPGA for LED control shown in Figure 11 is configured to control the lighting of the LEDs at the clock timing of the trigger signal. As shown in Figure 12, 5×5 matrix LEDs light up one by one from upper left to lower right according to the rise of the trigger signal. As shown in Figure 13, the matrix LEDs are photographed with the camera sensor fixed.

Figure 14 shows the result of imaging by the camera sensor. Time elapses from the upper left to the lower right. Since the LEDs in the image light up one by one, images can be acquired according to the signal input to the FPGA for LED control. In the images, the LEDs light up two at a time, and it can be seen that the camera sensor has a certain delay with respect to the trigger. As shown in Fig. 14, it was verified that images could be continuously acquired in synchronization with the trigger.

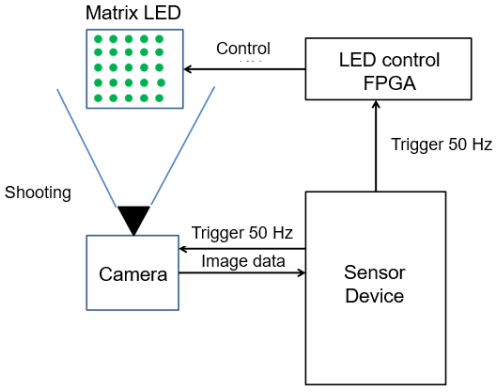

Figure 10. Camera data measurement system.

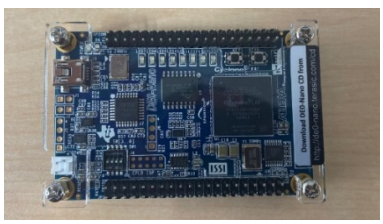

Figure 11. FPGA for LED control.

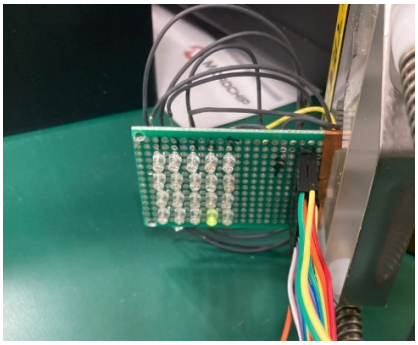

Figure 12. Matrix LEDs.

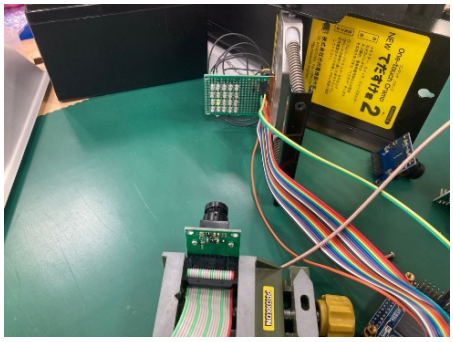

Figure 13. Imaging arrangement.

Figure 14. Continuous images from the experimental result.

The performance verification experiment on the time synchronization of developed camera sensor device was carried out as shown above. It is confirmed that time synchronization among the developed digital sensor devices with camera is achieved. The development of this digital sensing platform has enabled time-synchronized measurements between digital accelerometers, camera sensors, and many types of external input analog sensors, as well as multimodal analysis between measurement data.

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V. CONCLUSION

In this paper, research and development relating to a digital sensing platform that autonomously retains highly accurate time information by applying a CSAC, was reported. First, a system based on a digital sensor and autonomous time synchronization by a CSAC was described, in which the development of a mechanism and a sensor device that add ultra-high-accuracy time information to sensor data using the CSAC were explained in detail. A function was added to assign the same time stamp as that of the output of the built-in digital accelerometer, to the output of the camera sensor.

The results of an experiment carried out to verify the time synchronization performance of the camera sensor were also reported. In the future, the author plan to apply this new, different type of digital sensing platform to actual structures to acquire acceleration and video data that retain accurate time information. One possible problem is that although the timing accuracy of the CSAC is high, aging will occur in the long term, so it may be necessary to consider how to operate the sensing system according to the purpose and object of measurement. Further, as CSAC are currently expensive, it is hoped that they will be used more extensively in many fields.

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