A Novel Multiple Valued Logic OHRNS Adder Circuit for Modulo (r^n-1)

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***Abstract*— Residue number system is a carry free and non-weighted number system. This system is appropriate for applications that require fast arithmetic computation. Residue Number System is defined by a moduli set. Selecting the moduli set is an important issue in this number system. Each number in this system is represented by its remainders in moduli set, so it introduces smaller numbers than conventional systems, which results in fast calculation and low power consumption. Multi Valued Logic increases the dynamic range by using same positions rather than binary logic. One Hot Residue Number System is a method, which reduces the delay of arithmetic computations such as addition and multiplication to just one transistor delay. In this paper, a new adder circuit is introduced for modulo (r^n-1) by combining One Hot Residue Number system and Multi Valued Logic, which has significant improvement in terms of number of applied transistors and power consumption in comparison to the ordinary One Hot Residue Number System with Multi Valued Logic.**

Keywords-Residue Number System;One-hot; Multiple Valued Logic; Low Power Circuits; VLSI.

I. INTRODUCTION

Some applications such as digital signal processing require fast computation with low power consumption. Residue Number System (RNS) satisfies these requirements by presenting a weighted number into smaller numbers with carry-free property, which results in parallel arithmetic operation [1][3]. One of the most efficient methods to achieve parallelism in arithmetic computation in VLSI digital systems is applying RNS. VLSI digital systems can be designed with smaller chip area, lower power consumption and more speed using RNS rather than conventional numeric systems.

Each RNS is based on moduli set, which consists of a set of relatively prime integers.

One of the most applied modulo in moduli sets is (a^b-1). Some well-known moduli sets which use this modulo are $\{r^a-1, r^b, r^c+1\}$, $\{2^{2n-1}, 2^{2n+1}-1, 2^{2n+1}+1\}$ $\{2^n-1, 2^n, 2^{n+1}-1\}$, $\{2^n-1, 2^n, 2^n+1\}$, etc.

In this paper, an adder circuit for modulo (r^n-1) is proposed, which has high speed and low power consumption. One Hot RNS (OHRNS) is a method that has lowest delay for addition and multiplication operations in RNS moduli. Since applying OHRNS is normally associated with using of Multi Valued Logic (MVL) and large number of transistors, so the VLSI circuit design based on OHRNS requires high power consumption and large area. The designed circuit in this paper decreases the number of transistors, which decreases power consumption, area and delay-power product (DP-product) significantly in OHRNS for (r^n-1) modulo adder.

The rest of this paper is organized as follow: Section II describes the necessary background. The proposed circuit is discussed in Section III. Sections IV and V contain the performance evaluation and conclusion respectively.

II. BACKGROUND

A. Residue Number System(RNS)

Residue Number System is specified by moduli set like $(m_1, m_2, ..., m_n)$ in which all the moduli are positive integers. If all the modulus be relatively pair wise prime the system will have the largest possible dynamic range which equals [α , α +M) in which α is an integer and M is:

$$M = \prod_{i=1}^{n} m_i \tag{1}$$

An integer X is represented in the Residue Number System by an n-tuple $(x_1, x_2, ..., x_n)$ where x_i a non negative integer is satisfied by:

$$x_i = X \bmod m_i \tag{2}$$

In RNS, arithmetic computations such as Addition, subtraction and multiplication for two given integer numbers X and Y, which are represented by $(x_1, x_2, ..., x_n)$ and $(y_1, y_2, ..., y_n)$ in moduli set $\{m_1, m_2, ..., m_n\}$, are as follow:

Assume $Z = X \circ Y$ and $Z = (z_1, z_2, ..., z_n)$ where $\circ$ operand is one of the noticed operations. For $1 \le i \le n$:

$$z_i = (x_i \circ y_i) \bmod m_i \tag{3}$$

z_i s can be calculated in parallel without any dependency between them, which leads to high speed computations in RNS. To convert a residue number $(x_1, x_2, ..., x_n)$ into its binary representation *X*, the Chinese Remainder Theorem is widely used. In CRT, the binary number *X* is computed by:

$$X = \left| \sum_{i=1}^{n} N_i \left| N_i^{-1} \right|_{m_i} x_i \right|_M \tag{4}$$

where $N_i = \frac{M}{m_i}$ and $\left|N_i^{-1}\right|_{m_i}$ is the multiplicative inverse of $\left|N_i\right|_{m_i}$ [1].

$$\begin{array}{cccc} a_{n-1} & a_{n-2} & .... & a_0 \\ \downarrow & \downarrow & .... & \downarrow \\ r^{n-1} & r^{n-2} & .... & r^0 \end{array}$$

Figure 1. Digits of a number in MVL

B. Multi Valued Logic

Another important feature of RNS is an alternative named multiple valued logic (MVL) that despite of binary system which is limited to just two possible logic states, the number of discrete signal values or logic states extends beyond two. Using MVL can result in more effective usage of silicon resource and circuit interconnections [2]. Therefore, by defining r levels for MVL each position has one of the $(0,1,....,r-1)$ levels. The value of each position in r-level MVL is r^i, where *i* indicates each position. For a given number $A(a_{n-1}.....a_0)$ the values of its digits are as shown in Fig. 1.

Since by using high radix in MVL much more information can be stored in each location in compare with binary logic, so speed of arithmetic computations is increased in this logic that has advantages of reduction of chip area, interconnections and increasing of chip performance.

C. One Hot RNS(OHRNS)

Power consumption is one of the most important factors, which is considered in designing the VLSI circuit. Many techniques have been proposed to decrease the power consumption. In many cases decreasing the power consumption results in reduced circuit performance, Therefore designers have focused on circuit design considering a more important factor is called Delay-Power product (DP product).

In one-hot, remainders of each modulo m_i $(0,1,...,m_i-1)$ are represented by a separated line as shown in Fig. 2, where in each moment just one line that is equal to x_i, a remainder of m_i modulo, is active and others are inactive. By changing the input value, the amount of two lines changes at maximum level. Therefore the wasting of power is at minimum level.

OHRNS makes this ability to do arithmetic computations such as addition, subtraction and multiplication rapidly and based on barrel shifters. OHRNS structure can be represented by a state machine.

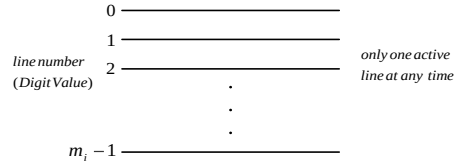

Figure 2. One- Hot representation for remainder of a modulo

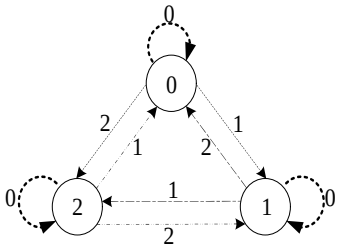

Figure 3. Representation of OHRNS as a state machine

For example for addition in OHRNS there are two operands, which one of them can be considered as the current state of machine and second operand is a shifter that shifts the first operand to the correct output as the final result. As an example, OHRNS state machine for addition in modulo 3 is illustrated in Fig. 3.

Structure of a computational OHRNS for each operation in modulo m_i has been shown in Fig. 4. It has two series of inputs, which are actually two required operands for addition operation. One of them is applied as a shifter and another as a data that must be shifted. In this architecture, transistors play the role of a shifter. More details about this structure have been introduced in [9]. Since modulo (r^n-1) is widely used in moduli sets in RNS, an adder for this modulo based on OHRNS has been designed.

According to above expressions and considering the details of this structure in [9], for adding two numbers in modulo (r^n-1), the required transistors are equal to (r^n-1)^2. However, the delay of this circuit is equal to just one transistor delay. In next section, a method is proposed, which decreases the number of applied transistors considerably. Furthermore, our proposed circuit handles the problem of previous work about OHRNS in which the circuit may encounter the fault and incorrect output due to the using of same unit for producing the addition result and carry-out digit.

III. MVL OHRNS ADDER FOR MODULO (r^n-1)

In this paper, an OHRNS–based adder circuit is proposed for modulo (r^n-1), which has significant improvement in terms of hardware cost and power consumption. Furthermore, its DP is considerably lower in comparison to the previous circuits. Assume that *A* and *B* are two numbers in modulo (r^n-1). Their values are totally in defined below span:

$$\begin{aligned} A &= (a_{n-1}.....a_2a_1a_0), \quad 0 \le A < r^n-1 \\ B &= (b_{n-1}.....b_2b_1b_0), \quad 0 \le B < r^n-1 \end{aligned} \tag{5}$$

where a_i and b_i have the values of:

$$0 \le a_i < r$$

$$0 \le b_i < r$$

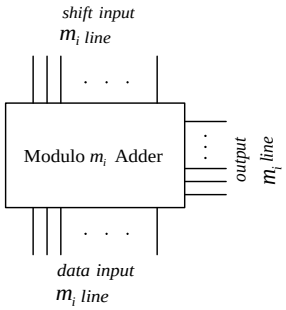

Figure 4. Block diagram of an OHRNS adder

In proposed modulo (r^n-1) adder, number *A* which has *n* digits is represented as two parts. The first part represents first *n/2* digits, which is considered as low significant part and another as high significant part such that:

$$A = (a_{n-1}a_{n-2}.....a_2a_1a_0)_r \rightarrow A = (A_1A_0)_r$$

where:

$$A_0 = \begin{cases} (a_{n/2}a_{(n/2)-1}.....a_1a_0)_r & \text{if } n \text{ is even} \\ (a_{\lfloor n/2 \rfloor}a_{\lfloor (n/2) \rfloor -1}.....a_1a_0)_r & \text{if } n \text{ is odd} \end{cases}$$
$$A_1 = \begin{cases} (a_na_{n-1}.....a_{n/2}) & \text{if } n \text{ is even} \\ (a_na_{n-1}a.....a_{\lfloor n/2 \rfloor +1}) & \text{if } n \text{ is odd} \end{cases} \quad (6)$$

In these equations both A_1 and A_0 are numbers in radixes R_0 and R_1, which are equal to:

$$R_0, R_1 = r^{n/2} \quad \text{if } n \text{ is even}$$
$$R_0 = r^{\lfloor n/2 \rfloor}, R_1 = r^{\lfloor n/2 \rfloor -1} \quad \text{if } n \text{ is odd} \quad (7)$$

In the same way for number *B* we have:

$$B = (b_{n-1}b_{n-2}.....b_2b_1b_0)_r \rightarrow B = (B_1B_0)_r$$

B_1 and B_0 are defined as well as A_1 and A_0. In new definition *A* and *B* have two low and high significant parts. Therefore, to add numbers in modulo (r^n-1) the adding method in conventional systems is used in which for adding two n-digits numbers all digits with same position are added together from least significant position to most significant position and the carry is added with the digits in next position. But the carry digit, which is obtained from adding most significant digits, must be added to the resulted number. So, to add *A* and *B* numbers the operation is performed as shown in fig. 5, where *C* is the result of adding *A* and *B* in modulo (r^n-1). The proposed circuit for (r^n-1) modulo adder is implemented by an OHRNS structure as shown in Fig. 6.

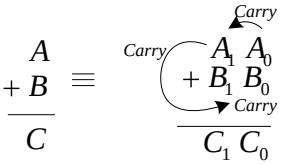

Figure 5. Adding two numbers in modulo $(r^n - 1)$

According to Fig. 6, addition operation once requires carry propagation from low significant part to high significant part and in next step from high significant part to low significant part. The carry in each step is obtained by one Hot for carry unit, which has a structure same to the One Hot adder unit. In spite of previous papers about OHRNS that each One Hot transistor is connected to two outputs, one for carry and another for the result of addition, we do not apply such method because coupling all output results together makes this problem that when value of an output is equal to one, the value of carry digit will be one even if its previous value is zero and it means an incorrect result. Therefore, to avoid such problem a separated One Hot unit is used to produce carry digits.

In this implementation for adding each part of two numbers as well as Fig. 5 a One Hot adder and a One Hot for carry units are used. Since the carry digit is equal to one or zero so, two lines of transistors are used to add it to the next part as shown in fig. 6.a. But as it can be observed in fig. 6.b for obtaining C_1 no One-Hot for carry unit is used because in modulo (r^n-1) the carry digit is just added once to the resulted number. So, it is ignored in the last part of the circuit.

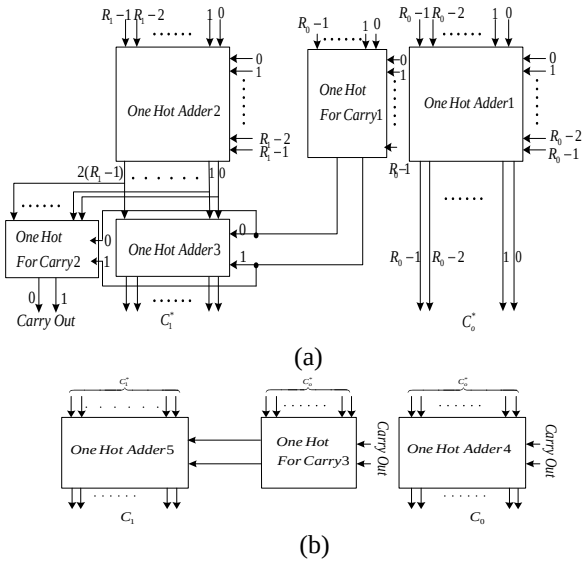

Figure 6. Block diagram of OHRNS adder in modulo $(r^n - 1)$

TABLE I. PERFORMANCE EVALUATION

	Hardware		Delay
Conventional OHRNS adder for modulo (r^n-1)	$(r^n-1)^2$ **Transistor**s		1 Transistor delay
Proposed OHRNS adder for this modulo	***Even n***	***Odd n***	4 Transistors delay
	$\left((r^{n/2})^2\times 3\right)+\left((r^{n/2}\times 2)\times 5\right)$	$\left((r^{(n+1)/2})^2\times 2\right)+(r^{(n-1)/2})^2+\left(6\times(r^{(n-1)/2})\right)+\left(4\times(r^{(n+1)/2})\right)$	

For example assume r and n are 3 and 4 respectively. For modulo (r^n-1) the value is:

$$(r^n-1)=(3^4-1)=80$$

To represent each number such as A in this modulo, four digits are required and it can be written as:

$$A=(a_3a_2a_1a_0)_m=(A_1,A_0)_r$$

$$A\in\{0,1,2,...,79\}\ and\ a_i\in\{0,1,2\},\ i=0,1,2,3$$

$$(A_1)_{R_1}=(a_3a_2)_{R_1},\ R_1=3^2\ and\ (A_2)_{R_0}=(a_1a_0)_{R_0},\ R_0=3^2$$

To make a comparison between conventional OHRNS and proposed method, the number of applied transistors is calculated for r=3 and different values for n. The results have been illustrated in Fig. 7 and Fig. 8. According to the results a significant reduction in applied transistors can be observed by using this method for modulo (r^n-1). The delay of this circuit is just equal to the delay of four transistors.

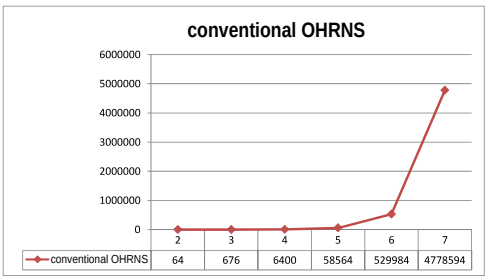

Figure 7.The number of applied transistors in ordinary OHRNS

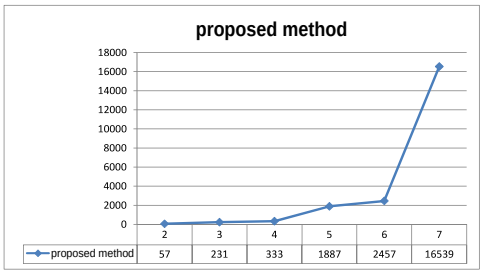

Figure 8.The number of applied transistors using proposed method

V. PERFORMANCE EVALUATION

In this section, the proposed OHRNS adder is compared with conventional OHRNS adder in terms of propagation delay and number of used transistors. In ordinary OHRNS for adding two numbers in a given modulo m, the required transistors are equal to m^2. In proposed method the numbers are divided into two parts that each one is calculated separately by using the One Hot adder unit. In previous work this unit was responsible for producing carry digits too. It should be taken into account that coupling these outputs together may result in incorrect output. To handle the problem another unit is called One Hot for carry has been added to the circuit. As it can be observed in Fig. 6 One hot adder1 and One-hot for carry1 have $R_0\times R_0$ transistors for each unit and One-hot adder2 has $R_1\times R_1$ transistors. One-hot adder4 and One-hot for carry3 have $2\times R_0$ transistors and the remained three units have $2\times R_1$ transistors. According to the values of R_0, R_1 and r obtained from (7), all required transistors have been calculated for odd and even n. The results of comparison have been shown in Table I. According to them a significant reduction in number of applied transistors is considered; however, the total delay of circuit is increased to four transistors delay, which is negligible versus the huge amount of reduced transistors. By using conventional OHRNS method for modulo (r^n-1), $(r^n-1)^2$ transistors are required. But as it can be observed in Table I, the proposed OHRNS adder decreases the number of applied transistors considerably. This reduction in number of applied transistors has a remarkable effect on decreasing the DP product.

VI. CONCLUSION

RNS is used widely for high speed arithmetic circuits according to its carry free property. OHRNS is a method which reduces the delay of addition and multiplication operation circuits to the delay of just one transistor; however, it has large power consumption according to the huge number of applied transistors.

In this paper, a novel method for One-Hot adder circuit has been proposed for modulo (r^n-1) which has significant improvements in terms of number of applied

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transistors and power consumption which, decreases delay-power product factor consequently.

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