A Testbed Concept for Cognitive Radio Prototyping

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***Abstract*—Future wireless systems are evolving towards a broadband and open architecture for efficient multi-service operation. This has a great impact on the terminal and infrastructure component design methodology for supporting multiple radio schemes. Cooperation in wireless networks, requiring cognitive radio implementations, will facilitate a new dimension in the evolution of multimedia communications. The growing price pressure requires ever increasing levels of integration efficiency, flexibility and future proofness at the same time, setting out in the digital baseband domain. In this manuscript, the authors will illustrate a platform based prototyping process, which combines the advantages of the flexibility of a digital signal processor with the efficient parallelization capabilities of a field-programmable gate array. The primary purpose of this platform is to allow a real-time capable implementation of cognitive radio systems. It allows the integration of the entire communication chain from the antenna to the decoded bit stream. Since the increasing computational complexity complicates the dimensioning of such platforms, scalability is a crucial design constraint for the presented concept.**

***Index Terms*—Cognitive Radio, Digital Signal Processor (DSP), Field-Programmable Gate Array (FPGA), Prototyping Platform, Testbed**

I. Introduction

Reconfigurability of transceivers for wireless access networks such as IEEE 802.11, IEEE 802.16, 3GPP LTE (Long Term Evolution) and various digital video broadcasting standards will become increasingly important in the forthcoming decade. An appropriately flexible and reliable software architecture allowing the concurrent processing of different controlling tasks for wireless terminals will hence be an important asset.

The hardware manufacturers are required to accelerate the development of new products to keep up with the decreasing product life cycles. Research activities in the last two decades showed that software-defined radio helps to overcome this problem [1], [2]. A transceiver can be considered as a software radio (SR) if its communication functions are realized as programs running on a suitable processor [1]. An ideal SR directly samples the antenna output which does not seem feasible with respect to e.g. power consumption and linearity as well as resolution requirements for ADCs (Analog-to-Digital Converters). A software-defined radio (SDR), however, is a practical and realizable version of an SR [1]: The received signals are sampled after a suitable band selection filter, usually in the baseband or a low intermediate frequency (IF) band. With the availability of software-defined radio based transceivers, the architecture can be used to implement multiple communication systems running on a common hardware platform by a simple reconfiguration process. Reconfigurability is not a new technique [1]. Already during the 1980s, reconfigurable receivers were developed for radio intelligence in the short wave range. However, reconfigurability became familiar to many radio developers with the publication of e.g. the special issues on software radios of the IEEE Communication Magazine [3]. Core part of such reconfigurable software-defined radio transceivers is a digital processor running the software. This software can be divided into a signal processing part and a scheduling part [4]. One major advantage of such a solution is the ease of implementation combined with very efficient debugging methods. Nevertheless, the computational capacity is insufficient for modern communication systems. Since the utmost goal for the design of new communication systems is a higher spectral efficiency, in particular the complexity of the channel decoding algorithms increases significantly. As a result, the requirements on the signal processing performance grow steadily. Hence, even the availability of multi-core digital signal processors does not allow real-time implementations of modern communication systems. To circumvent this limitation, hardware-based implementations of the digital signal processing blocks are favorable. Therefore, field-programmable gate arrays (FPGA) are suitable devices which allow the integration of highly parallelized algorithms on the one hand and reconfigurability on the other hand. However, one considerable disadvantage of the deployment of FPGAs is the effort for debugging the implemented signal processing algorithms.

A cognitive radio (CR) is an SDR that additionally senses its environment, tracks changes, and reacts upon its findings [5]. A CR is an autonomous unit in a communications environment that frequently exchanges information with the networks it is able to access as well as with other CRs. From the authors´ point of view, a CR is a refined SDR. SDR and CR transceivers differ from conventional transceivers by the fact that they can be reconfigured via control units. Such control units need information about the type and standard of the radio communications link and software modules for the signal processing path in order to reconfigure the receiver properly.

The platform presented in this document takes advantage of both concepts. Its core components are a powerful triple-core digital signal processor (DSP) in combination with an FPGA. This platform can be used as a prototyping platform for Cognitive Radio implementation as well as during standardization

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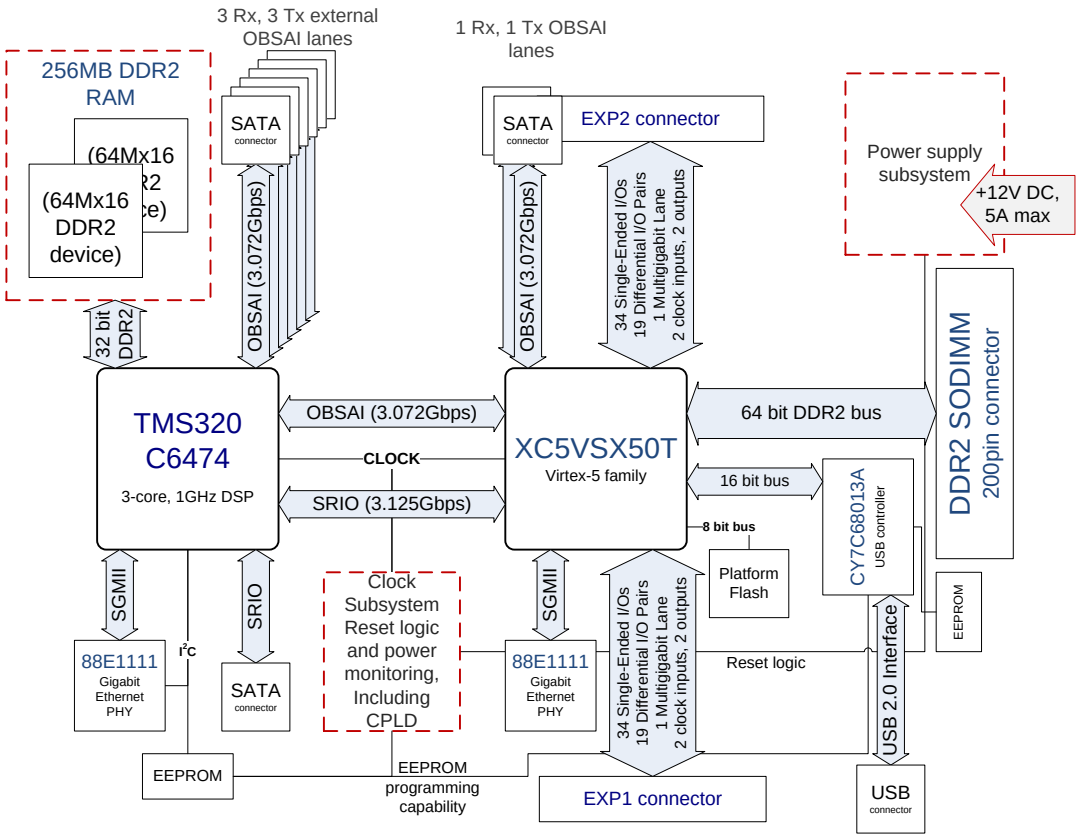

Fig. 1. *eFalcon* block diagram

processes and can be considered to fill the gap between the theoretical considerations for the algorithm design and the final system implementation. Due to its scalability this platform can be used even for next generation communication systems with multi-antenna features. In what follows, the prototyping platform developed by the authors is referred to as *eFalcon*.

The present document is organized as follows. After this brief introduction, Sect. II gives an overview of *eFalcon*. Since clock generation and distribution is a critical factor in platform design, Sect. III primarily addresses this aspect. In order to increase the computational performance of *eFalcon*, it exhibits interfaces for the interconnection of multiple platforms. This scalability aspect is discussed in Sect. IV. Sect. V presents a testbed concept for a Cognitive Radio. Finally, a conclusion is given in Sect. VI.

II. Platform Overview

As discussed in Sect. I, a prototyping platform consisting of a combination of a DSP and an FPGA is desirable. A block diagram of *eFalcon* is shown in Figure 1. Core part of this platform is the Texas Instruments triple-core DSP TMS320C6474 running at 1 GHz system clock. The DSP has 256 MB of DDR2 Random Access Memory (RAM) attached which enables the implementation of memory intensive applications. The interfaces to external components consist of a Gigabit Ethernet link, three full duplex OBSAI (Open Base Station Architecture Initiative) or CPRI (Common Public Radio Interface) lanes, commonly referred to as antenna interface, and a Serial RapidIO (SRIO) link. The clock generation and distribution network described in Sect. III provides a reference clock which is used to generate the system clock by a processor-internal phase-locked loop (PLL). The DSP supports several boot modes using either I^2C, Ethernet or SRIO.

Besides the top-level scheduling functionality, the DSP is the central signal processing unit. Depending on the hardware/software split carried out between DSP and FPGA, the DSP firstly carries out the synchronization on the incoming data signal received from the antenna interface. After a successful synchronization, a channel estimation is performed. In what follows, the incoming signal is equalized and demodulated. In general, the output of the demodulator is a likelihood information, which is fed into the channel decoder. The DSP contains very flexible hardware accelerators for Viterbi and Turbo decoding since convolutional and turbo codes can be found in a large number of communication standards. In case of channel codes like LDPC (Low-Density Parity-Check) codes employed e.g. in various modern video broadcasting standards [6], the DSP's signal processing capability is not sufficient to decode the incoming signal stream in real-time. In that case, the FPGA which is directly attached to the DSP can be used to design a DSP co-processor dedicated to a specific signal processing task. Besides the potential DSP co-processing capability, the FPGA, namely a Xilinx

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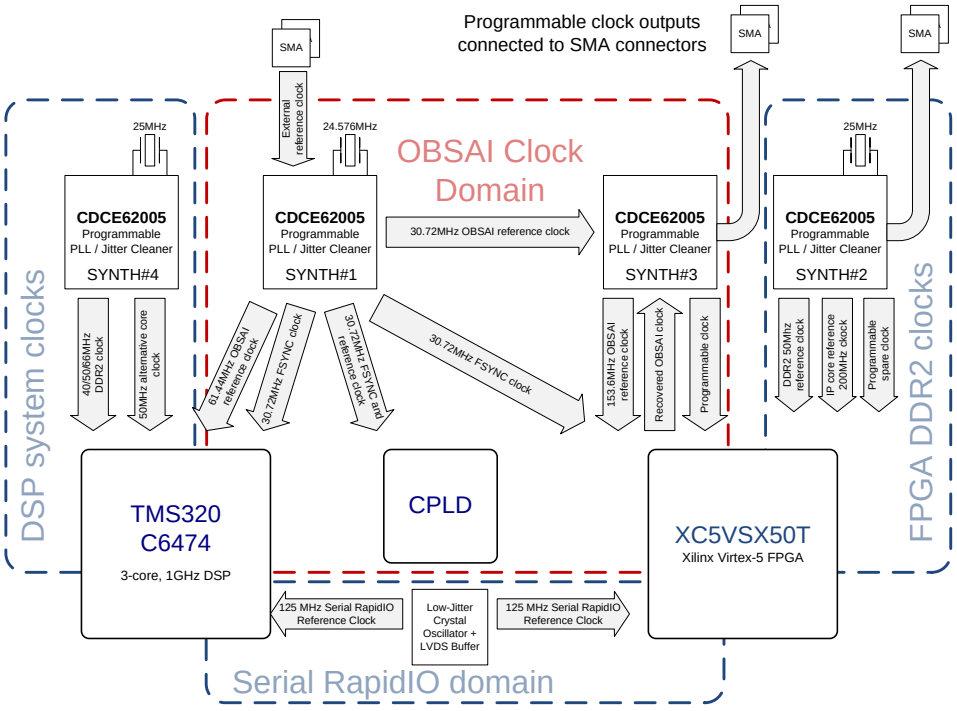

Fig. 2. *eFalcon* clock subsystem

XC5VSX50T, implements additional interfaces to external peripheral devices. Besides Gigabit Ethernet, a USB 2.0 interface is attached to the FPGA which can be used to communicate with conventional PC hardware. The connection to the DSP is realized using OBSAI, CPRI or SRIO. The FPGA offers the capability of attaching a DDR2 SODIMM which can be used to extend the memory capability of the platform significantly. Spare high-speed serial ports are routed to proprietary connectors which can be used with a variety of protocols.

One major task of the FPGA is to act as a bridge between the high-speed serial interfaces of the DSP and the parallel interfaces of analog-to-digital (A/D) or digital-to-analog (D/A) converters. Therefore, the FPGA offers a full implementation of the Avnet EXP Expansion Connector Specification [7] consisting of two connectors with 34 single-ended and 19 differential I/O pairs each. In addition, this interface consists of lines for clock inputs and outputs as well as high-speed serial connectivity. The FPGA can be used to post-process baseband data calculated by the DSP and submit it to the D/A conversion process. Digital up-conversion, up-sampling and filtering algorithms are applied in this step. In the A/D conversion process, the FPGA pre-processes the incoming data before transmitting it to the DSP. Signal statistics, which act as an input for an automatic gain control (AGC), are calculated. These statistics consist of long-term averages as well as fast detect features to enable over-range indication and can also be used to remove DC offsets. Further processing consists of digital down-conversion in case of intermediate frequency (IF) sampling, sampling rate adaptation and filtering. The FPGA is also ideally suited for the application of synchronization blocks which usually consist of autocorrelation or cross-correlation based algorithms.

In case the signal processing capability of one platform is not sufficient to operate a communication standard in real-time, additional platforms can be easily attached to increase the performance, cf. Sect. IV.

Due to the large number of different devices, a complex power supply design is mandatory. *eFalcon* works with an input voltage of 12 V. Switching regulators are used to generate voltages less than this input voltage at a high efficiency and directly supply the multitude of digital devices. Voltages which are used to supply analog parts of devices, especially the PLLs, are generated using linear low-dropout regulators. All voltages are monitored and reported to a central glue logic, which is implemented in a CPLD (Complex Programmable Logic Device). This device is the first device which is properly configured after applying power and, hence, coordinates the start-up procedure.

III. Clock Generation and Distribution

Modern digital systems have strict requirements on the clock references. Both the DSP and the FPGA contain on-chip PLLs which need to be supplied with a suitable reference frequency. These signals are required to derive the core clocks as well as the reference clocks for the high-speed serial links. Figure 2 shows a general block diagram of the platform clock subsystem. Most of the reference clocks in the system are generated by a Texas Instruments CDCE62005 device which is a fully integrated PLL including a voltage controlled oscillator

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(VCO). A programmable loop filter is also integrated on the chip. All platform clocks generated by the CDCE62005 devices can be split into two general classes. The first class contains the 30.72 MHz derivatives which are used in the OBSAI and CPRI clock domain. The second clock class includes all other clocks which are derivatives of 25 MHz. The reference clock of 125 MHz which is necessary for SRIO is generated by a dedicated crystal oscillator. Both Ethernet PHY chips contain an internal PLL and a 25 MHz crystal resonator as frequency reference. The USB controller uses a 24 MHz external crystal resonator to generate the necessary clock for the FPGA-to-USB data transfer. Besides an internal generation of the PLL reference frequency, all devices have the capability to be fed by an external reference. These external references are routed to coaxial connectors which can be used by an external clock distribution network to synchronize an arbitrary number of platforms. This is an important feature for the case that multiple platforms are connected to work on a single signal processing task.

IV. Scalability

eFalcon is based on a flexible architecture which paves the way towards a rapid implementation of algorithms deployed in modern communication systems. It offers the opportunity to directly attach two daughter cards following the Avnet EXP Expansion Connector Specification. One possible scenario is the implementation of a full transceiver chain so that one EXP interface is used for attaching an A/D converter board and the second one is used for attaching a D/A converter board. Furthermore, it is possible to establish a multi-antenna system with two receive or two transmit antennas.

One crucial aspect during the concept phase of *eFalcon* was scalability in order to be prepared not only for current communication systems but also for next generation systems with increased complexity requirements. On the one hand, *eFalcon* consists of multiple serial high-speed interfaces such as OBSAI, CPRI and SRIO to allow intra-board communication but also board-to-board communication with data rates beyond 1 GBit/s. On the other hand, the elaborate clock distribution concept of this platform allows an accurate synchronization of multiple platforms. Thus, the interconnection of two or more prototyping platforms by a combination of serial high-speed interfaces and a clock synchronization enables the implementation of multi-antenna systems with even more than two antennas. In that case, one platform acts as a master device which is responsible for the clock generation and distribution to the attached platforms acting as slaves as well as for the main scheduling parts of the signal processing chain.

V. Cognitive Radio Implementation Aspects

Figure 3 shows the Cognitive Radio demonstrator concept implemented using the *eFalcon* platform.

The concept consists of a transmitter branch which is intended for the real-time generation of arbitrary signal waveforms. The baseband signal in either complex inphase and quadrature (I/Q) or real valued intermediate frequency (IF)

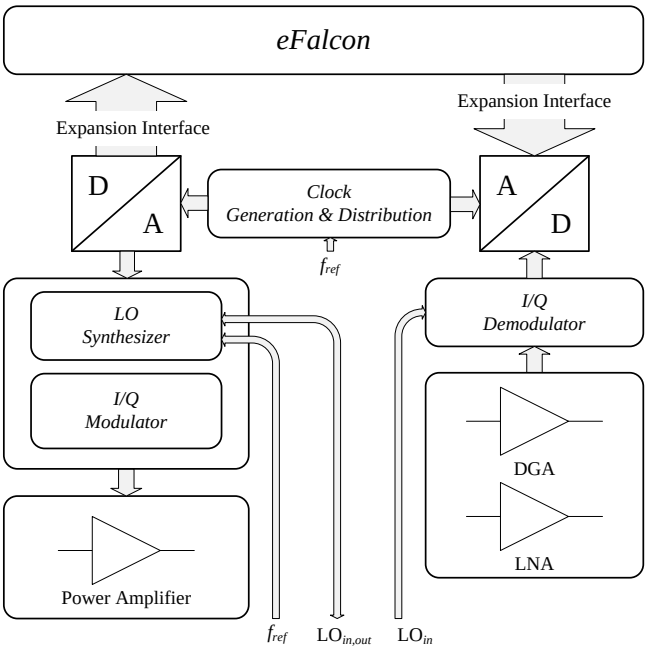

Fig. 3. *eFalcon* Cognitive Radio demonstrator concept

representation is generated using the *eFalcon* platform and is fed into a D/A converter. After a suitable reconstruction filter, the resulting analog signal is upconverted to a carrier frequency using an I/Q modulator. The local oscillator (LO) signal which is used in the up-conversion process is generated by an LO synthesizer and ranges from 300-4800 MHz. The synthesizer accepts external reference signals which can be used to synchronize the LO phase in case of multi-antenna applications. In addition, the LO signal can be externally fed in or distributed to other platforms. The I/Q up-converter is followed by an optional power amplifier branch which can be used to obtain signal levels up to +30 dBm. Optionally, the up-converter can also be driven by an IF signal.

The receiver branch consists of a gain stage implemented by a combination of a low noise amplifier (LNA) and multiple digitally controlled amplifiers (DGA) which allow the amplification of signals at very low input levels. The gain vectors which lead to an optimal behaviour in terms of noise figure and linearity are calculated in the *eFalcon* platform according to the signal level detectors implemented at several positions within the amplifier chain. The resulting signal is fed into an I/Q demodulator which converts the signal to complex baseband using an external LO signal. The down-converter can also be configured for IF applications where the I/Q branches can be used for the implementation of a Hartley image reject receiver [8]. The baseband signal is sampled and the resulting signal samples are transferred to the *eFalcon* platform using the expansion interface. The *eFalcon* platform performs the desired cognitive operation and reports the results to a data sink.

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VI. Conclusion

Within this document, the authors presented a Cognitive Radio demonstrator concept. Besides powerful digital baseband processing capabilities, the demonstrator concept consists of analog transmitter and receiver branches which allow signal sensing applications in the range of 300-4800 MHz. The architecture based on a combination of a triple-core digital signal processor and a field-programmable gate array paves the way towards rapid implementation of arbitrary communication systems and Cognitive Radio concepts accompanying the standardization process. Thereby, the advantage of both digital processors running software and programmable logic allowing massive parallelization to guarantee real-time operation has been merged to one single platform. The basic ideas during the concept phase were a high flexibility, modularity and scalability to even allow the integration of multi-antenna systems.

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