Area and Speed Efficient Layout Design of Shift Registers using Nanometer Technology

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***Abstract*— The paper presents an area and speed efficient CMOS layout design of shift register on 180 nanometer (nm) technology. The proposed shift register is designed using Serial In Serial Out (SISO) and Serial In Parallel Out (SIPO) techniques. Shift registers are commonly used in large number of sequential circuits and processors for temporary storage of data. The area and speed of developed layout designs are improved by optimized placement and routing for layout. The schematic and layout of both designs are simulated and analyzed using Cadence software. It can be observed from simulated results that the delay of SISO register is 0.97 ns and the delay of SIPO register is 0.71 ns. The SISO register shows 78.6% improvement in delay and SIPO register shows 27.46 % improvement in delay. The silicon area consumption of SISO register is 140.6 nm x 129.49 nm and SIPO register is 130.98 nm x 85.91 nm to provide cost effective solution for Very Large Scale Integration (VLSI) applications.**

Keywords- CMOS; Flip Flop; Shift Register; SISO; SIPO; VLSI.

I. INTRODUCTION

The new era of technology had a great impact on the field of VLSI, which is constantly under examination by many researchers throughout the world. It involves mainly increase in speed, reduction of area and power consumption [1]. Most vital component of the Integrated Circuits (ICs) for temporary storage of data is a Flip Flop. It stores a logical condition of one or more input signals using external clock [2]. Flip-flops are used in majority of computational circuits to store the data and provide adequate processing time to different circuits inside a system. In CMOS circuits, D Flip Flop (DFF) is essential building block and is responsible for the delay and total power dissipation calculations of any electronic system. Shift registers, which are created with the help of D flip-flops, have their intensive applications in various VLSI fields. The design of a shift register includes an N-bit shift register, made out of N number of Flip Flops [3][4][5].

A register is a circuit with two or more D Flip Flops connected together such that they all work exactly in the same way and a single clock synchronizes all the flip flops [6][7]. Each of these flip-flops has the ability of storing a single logic i.e., 0 or 1. There are limited compositions of 0 and 1 that can be stored into a register. These combinations are called the state of the register. Flip-Flops can store data in multiple sizes like 4, 8, 16, 32 or even 64 bits. Thus, several Flip Flops are combined to form a register to store whole data [8][9]. Fully custom 4-bit CMOS shift register consumes less power and less area as compare to semi custom and auto generated designs [10]. Double Edge Triggered Flip Flops are bi-stable flip-flop circuits in which data is latched at rising and falling edge of the clock signal. Using such flip-flops permits the rate of data processing to be preserved while using lower clock frequency. Therefore, power consumption in DETFF based circuits is less [11].

Three important factors related to nanometer technology based shift registers are power, delay and area. Most of the existing designs are concentrating on power factor without considering others. Some are working on power and area factors by ignoring delay factor which is very important these days for real time applications. So in order to fill these gaps related to shift register designs, optimized SISO and SIPO registers are developed in this paper to provide area efficient cost effective solution for real time applications. The rest of this paper is organized as follows. Section II presents shift register overview. In Section III, schematic design and simulations are presented. Section IV explains the layout design and analysis. Finally, Section V concludes the paper with the future work.

II. SHIFT REGISTER

The main use of shift register is transmission of data after storage in serial or parallel manner. Serial means steady progression of bits in sequential manner and parallel means progression of all bits at the same time. Generally, shift registers are classified according to their structure into four different operating modes:

1. Serial-In Serial-Out (SISO) - The data is fed serially as input and the shifted output also occurs serially, one bit at a time in either left or right direction under clock control.

2. Serial-In Parallel-Out (SIPO) - The register is loaded with serial data, one bit at a time, with the output being stored in parallel form.

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3. Parallel-In Serial-Out (PISO) - The data is loaded in parallel form into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

4. Parallel-In Parallel-Out (PIPO) - The parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse [12].

A. *Serial In Serial Out Shift Register*

Fig. 1 shows an example of four-bit SISO shift register using Single Bit Flip-Flop (SBFF).

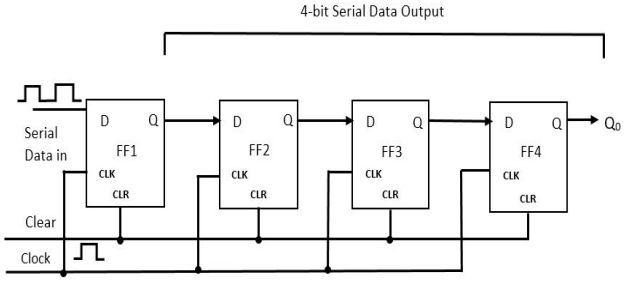

Figure 1. Serial-In Serial-Out Shift Register

A 4-bit SISO shift register is shown which takes four clock pulses to store the data bits and additional four cycles to transfer the data bits out from the register [12][13].

B. *Serial-In to Parallel-Out (SIPO)*

Fig. 2 shows a four-bit SIPO shift register which takes four clocks to process the input data and single clock to transfer the output data [10][11].

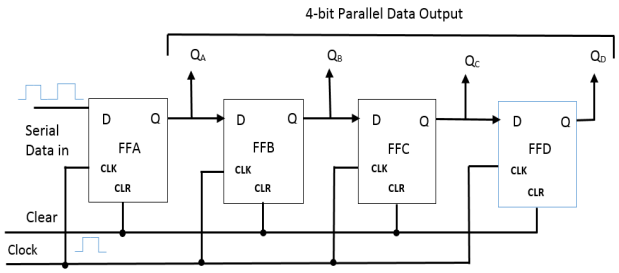

Figure 2. Serial-In to Parallel-Out 4-bit Shift Register

Every clock pulse impacts the register by shifting the data of every stage one place to the right. This data value at the output can now be read directly from QA. After the fourth clock pulse has ended the 4-bits of data are stored in the register and will remain there provided clocking of the register has stopped.

III. Schematic Design Simulation

The schematic of SISO register has been designed and simulated using 1.8V operating voltage on 180nm technology. Fig. 3 shows the schematic design of D flip-flop using NAND modules with power consumption of 746.8mW and delay of 0.245ns.

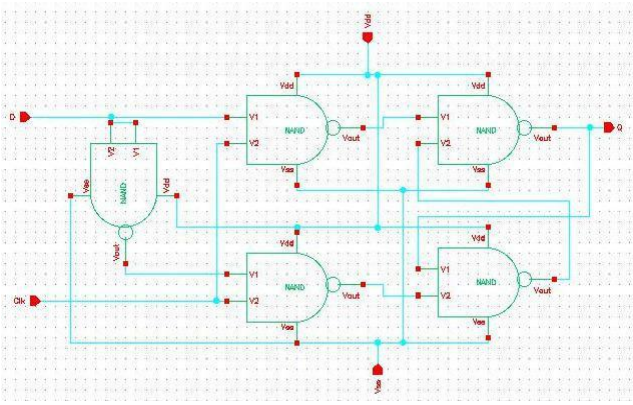

Figure 3. Schematic Design of D Flip-Flop

D-Flip Flop module was created and four such modules were combined together to design SISO register schematic as shown in Fig. 4. The developed SISO register has shown power consumption of 0.549mW and delay of 0.97ns.

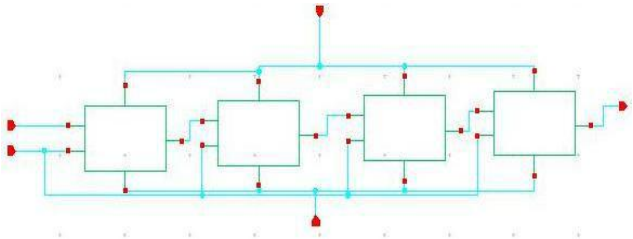

Figure 4. Schematic of SISO Shift Register

Analog simulation of designed SISO register has been performed for logic verification. The transient and DC responses of proposed SISO register are shown in Fig. 5 and Fig. 6 respectively.

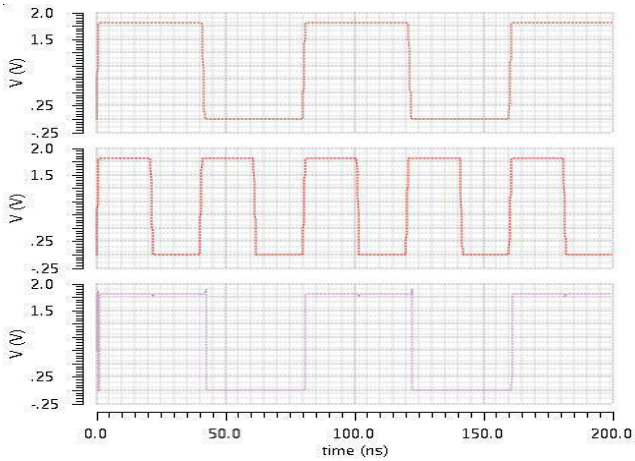

Figure 5. Transient Response of SISO Shift Register

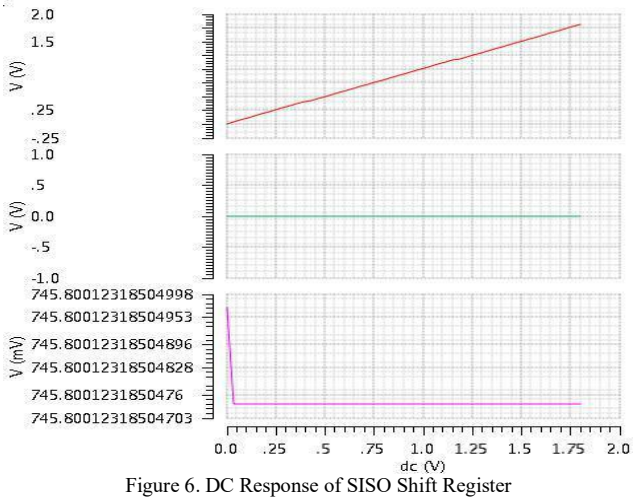

Figure 6. DC Response of SISO Shift Register

To improve the speed factor SIPO shift register schematic is designed as shown in Fig. 7. The developed SIPO register has shown power consumption of 0.5493 and delay of 0.71ns.

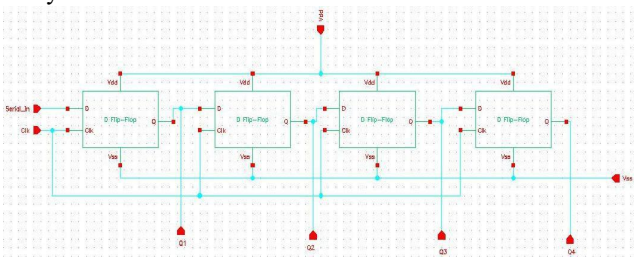

Figure 7. Schematic of SIPO Shift Register

The logic of developed SIPO register has been verified using analog simulation. The transient and DC responses of proposed SIPO register are shown in Fig. 8 and Fig. 9 respectively.

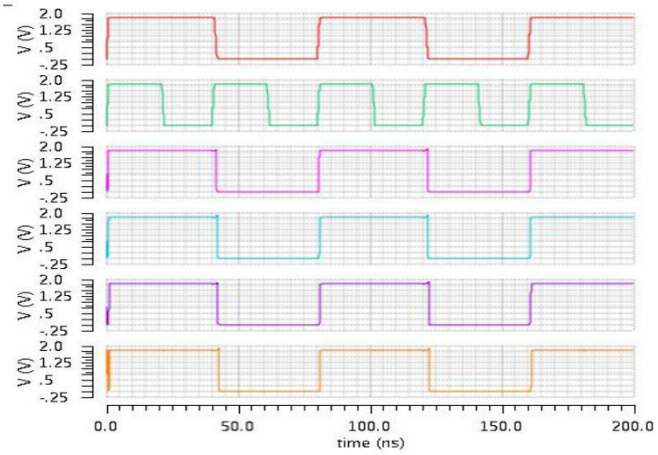

Figure 8. Transient Response of SIPO Shift Register

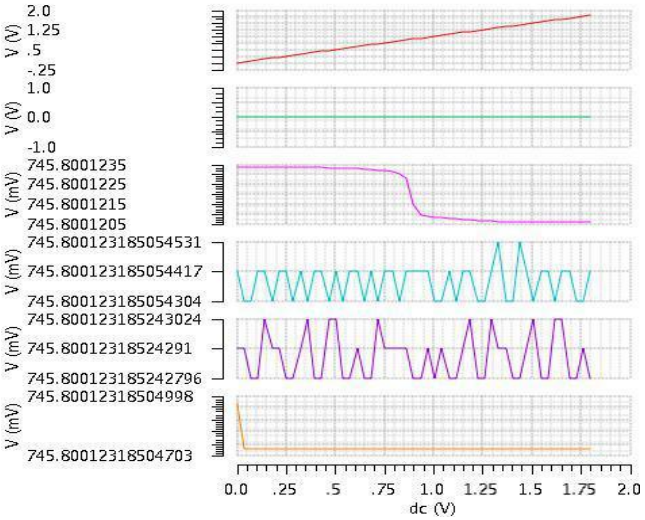

Figure 9. DC Response of SIPO Shift Register

After the evaluation of circuits is done with the help of simulations, then we proceed to the final step i.e., layout of shift registers.

IV. Layout Design Analysis

D-Flip Flop layout is developed using optimized NAND gates which consumes an area of 36.945mm x 33.44mm as shown in Fig. 10.

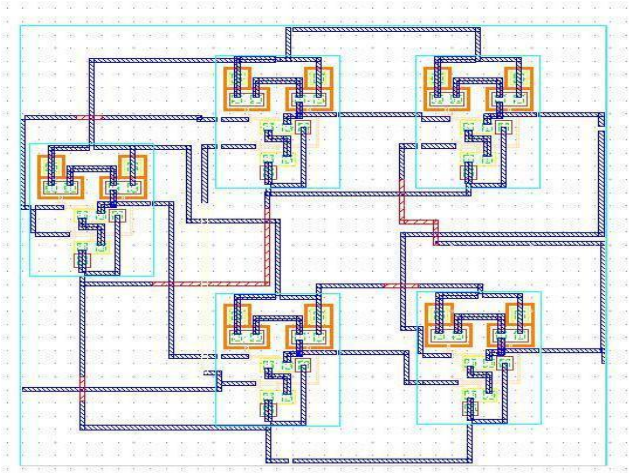

Figure 10. Layout Design of D flip-flop

D-Flip Flop layout module is created and four such modules are combined together to develop final layout of SISO register as shown in Fig. 11. The proposed SISO register layout has shown area consumption of 130.98nm x 85.91nm and power consumption of 0.536mW. Finally layout Vs schematic (LVS) comparison has been performed to verify the design performance as shown in Fig. 12.

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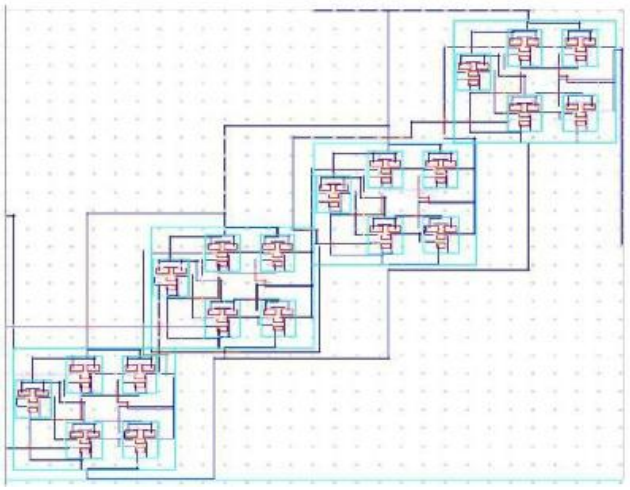

Figure 11. Layout Design of SISO Shift Register

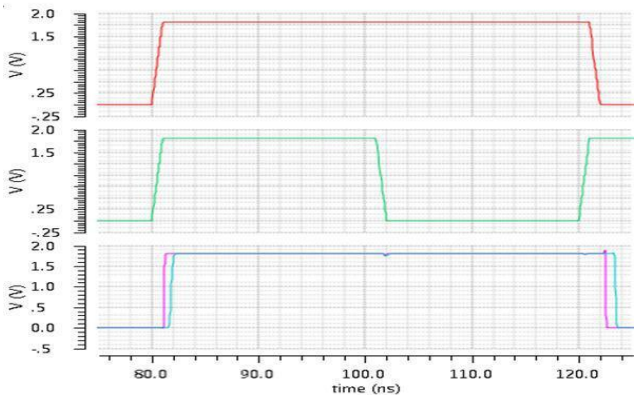

Figure 12. SISO Register LVS Comparison

Similarly layout of SIPO register has been developed with D-Flip Flop by using optimized placement and routing as shown in Fig. 13. The proposed SIPO register layout has shown area consumption of 130.98nm x 85.91nm and power consumption of 0.43mW.

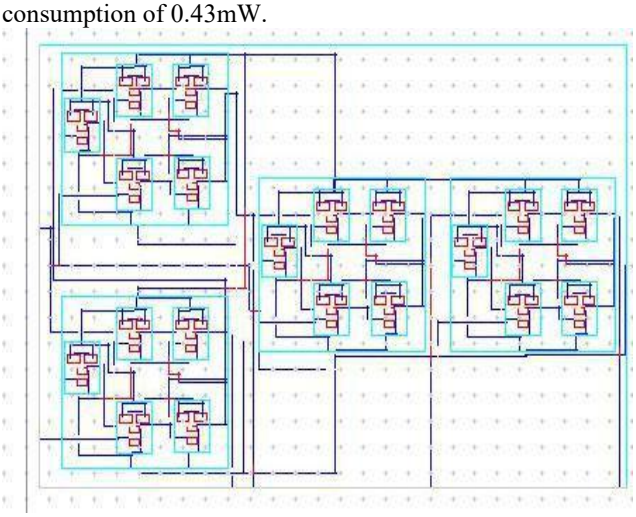

Figure 13. Layout Design of SIPO Shift Register

Layout Vs Schematic (LVS) comparison of SIPO shift register has been performed to verify the performance of developed design as shown in Fig. 14.

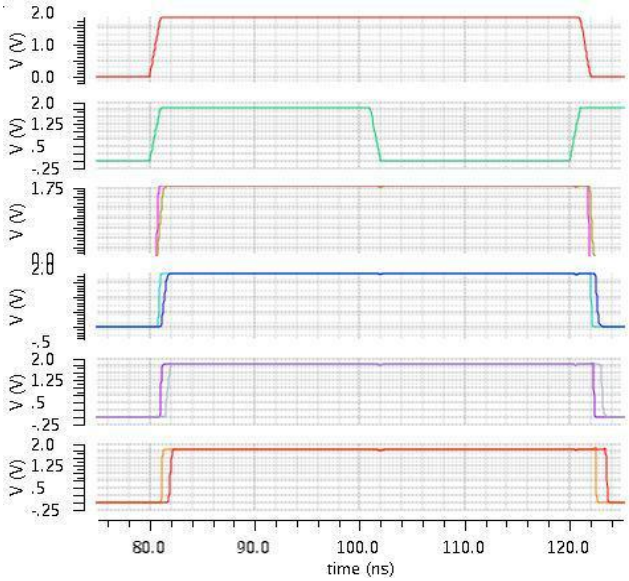

Figure 14. SIPO Register LVS Comparison

Table 1 shows the area and speed analysis of proposed SISO and SIPO registers. It can be observed from the table that SIPO design provides better speed as compared to SISO design, while consuming same amount of area.

TABLE I. PERFORMANCE ANALYSIS OF PROPOSED DESIGNS

Design Technique	Area (nm^2)	Delay(ns)
SISO	140.6*129.49	0.97
SIPO	130.98*85.91	0.71

TABLE II. DELAY COMPARISON

Design Technique	Existing Design [13]	Proposed Design
SISO	1.71 ns	0.97 ns
SIPO	0.905 ns	0.71 ns

The delay comparison of proposed designs with existing designs [13] is shown in Table 2. It shows that proposed SISO register provides 78.6% improvement in delay and SIPO register provides 27.46% improvement in delay as compared to existing designs.

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V. CONCLUSION AND FUTURE WORK

Area and speed efficient 4-bit SISO shift register and 4-bit SIPO shift register are designed on 180 nm technology. These designs were improved using optimized placement and routing technique. The proposed designs were developed by using D Flip Flop modules based on optimized NAND gate layout. The developed SIPO register has shown better speed as compared to SISO register by consuming same area. The proposed SISO register has shown 78.6% improvement in delay and proposed SIPO design has shown 27.46% improvement in delay as compared to existing designs. The proposed optimized designs have consumed very less silicon area to provide cost effective solution for VLSI applications. In future work, designs can be further optimized by developing improved placement and routing algorithm.

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