A 2.45 GHz CMOS Voltage Controlled Ring Oscillator for Active Transponder

Jubayer Jalil, Manum Bin Ibne Reaz, Labonnah Farzana Rahman,
Mohammad Marufuzzaman and Mohammad Syedul Amin
Department of Electrical, Electronic and Systems Engineering,
Universiti Kebangsaan Malaysia
43600 Bangi, Selangor, Malaysia
jubayer.jalil@gmail.com, mamun.reaz@gmail.com, labonnah.deep@gmail.com,
marufsust@gmail.com, syedul8585@yahoo.com

***Abstract*—An improperly designed voltage controlled oscillator (VCO) for radio frequency (RF) phase locked loop (PLL) simply degrades performance of wireless communication. This paper proposes a low power ring oscillator based VCO developed for 2.45 GHz operated active readerless RFID transponder compatible with IEEE 802.11b protocol. In favor of easy integration and implementation of the module in small die size, a 3-stage differential delay cell has been adopted to fabricate the proposed voltage controlled ring oscillator (VCRO). 0.18 µm CMOS process is used for designing the proposed VCRO with 1.8 V power supply. Simulated results show that the proposed VCRO will work in the tuning range of 2.32 - 2.85 GHz and dissipate only 11.25 mW of power at 2.45 GHz. Thus, the proposed VCRO will be a vital module for active readerless RFID transponder.**

Keywords-VCRO; RFID; Transponder; CMOS; Differential.

I. INTRODUCTION

Radio-frequency identification (RFID) is a smart identification system, relying on storing and remotely retrieving data using devices called tags or transponders. The typical RFID system comprises one or several readers which communicate with many tags simultaneously. Nowadays, implementations of RFID systems are extensively introduced in the supply chain, public transportation and biomedical applications. The operating frequency ranges of current RFID systems established for international standards extend from 135 KHz to 2.45 GHz [1]. In the RFID systems, tags can be categorized generally into two types: Passive and Active based on the power source. Passive tags use the magnetic field of readers as a source of energy and thus communicate with the readers. Active tags are battery-powered devices that have an active transmitter onboard. Unlike passive tags, active tags generate RF energy by themselves and this autonomy from the reader means that they can communicate at long distances dissipating more power than their counterparts.

At present, RFID deployment in numerous applications is a key challenge for technologist due to multiple standardization issues and expensive vendor specific readers. Moreover, RFID tags operating in several bands—high-frequency (HF) (13.56 MHz), ultra-high-frequency (UHF) (860–915 MHz), and microwave band (2.4 GHz), have limited operational range, less than 2m to maximum 9m [2].To overcome these concerns, a concept of reader-less RFID system based on IEEE 802.11b or Wi-Fi technology has been proposed [3]. In that system, RFID transponder will be battery-powered active device and its operating frequency will be 2.45 GHz (unlicensed ISM band). Moreover, conventional reader will be replaced by wireless network interface card (WNIC) utilizing desktop computer or laptop to make the system generic. However, effective use of active transponder's power is undoubtedly a crucial issue to implement this reader-less RFID system successfully.

During its activation, a RF transceiver of operating in gigahertz range usually dissipates substantial amount of power. That is why a direct conversion RF transceiver was proposed to implement the readerless transponder [4]. In this analog transceiver, one of the major blocks is the frequency synthesizer or local oscillator, which is done typically by using phase lock loop (PLL). This PLL is composed of phase detector (PD), low pass filter (LPF), voltage controlled oscillator (VCO) and frequency divider shown in Fig. 1. In this type of PLL-based frequency synthesizer, the most power hungry module is VCO, which generates frequency and changes the oscillating frequency varying control voltage.

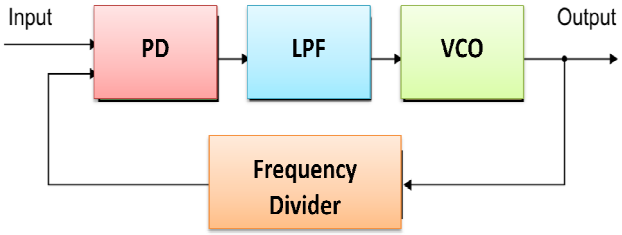

Figure 1. Block diagram of PLL based frequency synthesizer

Until now, LC-type and RC-type of CMOS VCOs have been used in wireless communication systems [5]. These VCOs performances are usually analyzed by low phase noise, low power dissipation, low voltage operation, high speed oscillation, multi-phase application, supply sensitivity reduction, simplified integration method, small layout area and wide tuning range. So far, LC based VCO has low level of phase noise among all CMOS VCOs [6]. However, it has narrow tuning range, greater power

Copyright (c) IARIA, 2012. ISBN: 978-1-61208-213-4

dissipation and large die area [7]. In addition, it is very difficult to integrate inductor in digital CMOS technology [8]. These shortcomings of LC-VCO are overcome by ring based VCO or better known VCRO. Recently, VCRO are widely accepted not only in wireless communication but also in optical communication and many more applications of the emerging ultra-wide band (UWB) and wireless sensor networks (WSNs).

VCRO can be implemented by single-ended or differential architecture of delay cell. Usually a number of delay cell blocks are connected in a positive or regenerative feedback loop for building a ring oscillator (RO). In VCRO, single ended ring topology comprises of inverters and each inverter is made up of an NMOS and PMOS transistors. On the other hand, differential topology is made up of a load (active or passive) with a NMOS differential pair. Currently, differential circuit topology is getting popularity among designers as it has common-mode rejection of supply and substrate noise [9]. Moreover, it could be formed by odd or even number of stages and is possible to achieve both in-phase and quadrature outputs in DROs [10].

In this paper, a unique differential delay cell has been proposed in 0.18 µm CMOS process designing in DA-IC of Mentor Graphics environment. The novel delay cell will be used for the proposed VCRO of readerless RFID transceiver. While designing the module for 2.45 GHz operating frequency, power consumption should be reduced to improve the performance of the transponder. In this research work, it is focused on widening the tuning range and reduction of power of the VCRO.

This paper will be organized as follows: Section II discusses the details of oscillator design; Section III describes construction of delay cell and its operation; Section IV presents simulation results and comparisons with other works; a conclusion is drawn in Section V.

II. VCRO ARCHITECTURE

For incorporation of this ring oscillator, only three of differential amplifiers or inverter stages are connected in a single delay path formation as shown in Fig. 2. Several novel delay cells have been demonstrated to compose the two-stage ring VCO, but extra power is inevitably needed to provide an excess phase shift for oscillation satisfying Barkhausen criterion. On the other hand, implementation of 4-stage of RO consumes considerable amount of power. Though three-stage ring oscillator cannot produce quadrature outputs like 2-stage or 4-stage RO, nevertheless it is faster than its four-stage counterpart. Moreover, in three-stage RO, fulfillment of proper start-up conditions can easily be attained unlike even number ROs, where latch-up frequently occur. Thus, the use of 3-stage is chosen to increase the oscillation and reduce power consumption at the same time.

Principle operation of this oscillator is that if one of the nodes is excited, the pulse will propagate through all the stages and will reverse the polarity of the initially excited node. For start-up and oscillation criteria, the transfer function for this ring oscillator with the number of stages set to 3 and can be represented as,

$$H(S) = \frac{-{A_0}^3}{\left(1+\frac{S}{\omega_0}\right)^3} \quad (1)$$

where A_0 denotes voltage gain of each delay cell and ω_0 denotes 3dB bandwidth at each stage.

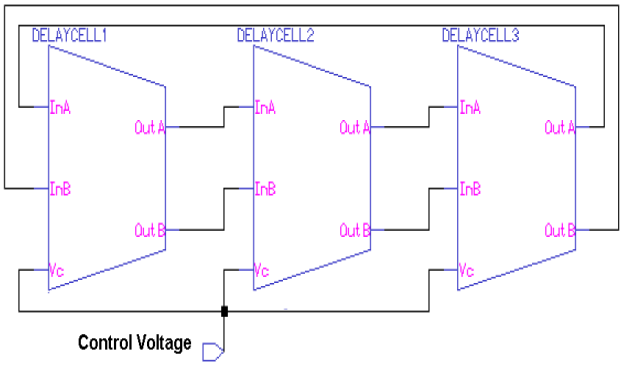

Figure 2. Architecture of the three-stage ring oscillator

As one of the criteria for oscillation is a phase shift of 180° that is each stage contributes with 60^0 of phase shift, the frequency at which it occurs given as,

$$\omega_{osc} = \omega_0 . tan\left({}^{180^\circ}/_{N}\right) \quad (2)$$

The other criterion for oscillation is a loop gain greater than 1 at ω_{osc}. Thus, it has been calculated the minimum voltage gain per delay cell by inserting the oscillation frequency expression of (2) into the gain equation found from (1). By solving this calculation, yields the minimum voltage gain of 2 (two) for each delay cell.

For every signal cycle, there is a downward as well as an upward transition. Since the high-to-low (t_{pHL}) and low-to-high (t_{pLH}) propagation delays associated with these transitions are not usually equal, the average propagation delay is given by

$$T = \frac{(t_{pHL}+t_{pLH})}{2} \quad (3)$$

The oscillation frequency for an *N*-stage ring is derived from the average propagation delay *(T)* of the inverter. A propagating signal will have to pass twice through the chain of delay cells, for a total delay of *2NT*, to complete one period. Thus, the frequency of the oscillation *(f)* is expressed as,

$$f = \frac{1}{2NT} \quad (4)$$

III. PROPOSED DELAY CELL ARCHITECTURE

In this research, novel delay cell architecture for the VCRO has been proposed as shown in Fig. 3. The

Copyright (c) IARIA, 2012. ISBN: 978-1-61208-213-4

proposed combination of the delay cell circuit is preferred as it alleviates necessity of tail current transistor caused flicker noise [11]. Additionally, it will improve output voltage stability without redundant bias circuit, which occupies a large space in chip.

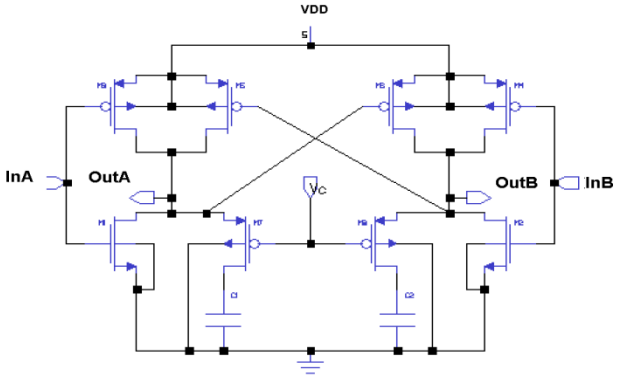

Figure 3. Schematic diagram of the proposed delay cell

A pair of CMOS differential push-pull inverter will be used as inputs in the new delay cell architecture, which is also shown in Fig.3. The push-pull inverter will consist of two different sizing of PMOS and NMOS. Additionally, two cross-coupled PMOS transistors will be connected in parallel with inverters PMOS transistors. These cross-coupled PMOS transistors will be introduced for fast switching speed. Sizes of all four PMOS in the cell will be chosen equally for smooth oscillation. In addition, a serially connected PMOS with a load capacitor of 0.1 pF will be employed in parallel with each NMOS input for frequency tuning.

The operation of the delay cell can be described considering half-cell circuit. While the input, *InA* will be high (near VDD), the input, *InB* will be low (equal to zero volt). This will turn on NMOS of the node, *InA*. On the other hand, PMOS of the input node, *InA* and cross-coupled PMOS connected in parallel with this input PMOS will remain off. Then voltage of the output node, O*utA* will be grounded. During that period, charge from the capacitor *(C_l)* will be discharged, or in other words, a path will be formed, which sinks current from O*utA* to bring its potential to 0 V. Similarly, if the input, *InA* will turn into 0 V, then the input, the input, *InB* will be high (near VDD). Zero potential of the input, *InA* will turn on PMOS and turn off NMOS simultaneously. Cross-coupled PMOS connected in parallel with the input PMOS of the node, *InA* will also remain switched on at this time. Thus, the discharged capacitor will be recharged again through these PMOS transistors. However, in both operations, a PMOS tuning transistor will control the overall charging and discharging of the load capacitor.

IV. SIMULATION RESULTS AND COMPARISONS

The proposed delay cell circuit has been verified by using the ELDO RF simulator (Mentor Graphics) of the CEDEC process. To determine the center frequency of the proposed delay cell circuit, the simulated output of the VCRO is shown in Fig. 4. If the control voltage is set to 0.22 V, frequency of 2.45 GHz is achieved as shown in Fig. 4. The supply voltage is set to 1.8 V and the 0.1 pF load capacitor is selected in the circuit for reducing die area.

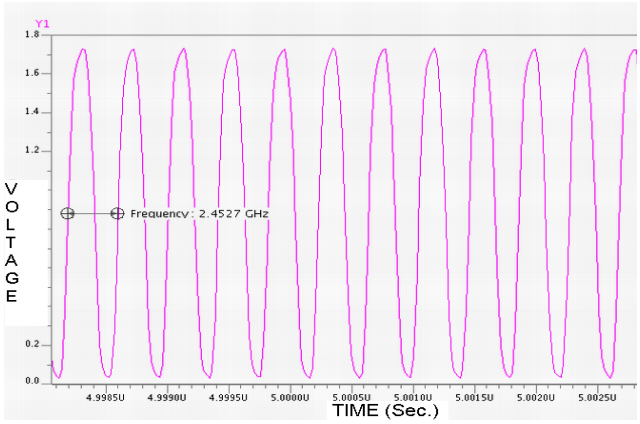

Figure 4. Simulated output of the proposed VCRO

In order to validate the proposed circuit in wide frequency range, the simulation is done at different control voltage. The output of different control voltages are shown in Fig. 5. In Fig. 5, it is being shown that if the control voltage is set to 0 V the proposed circuit is able to work in 2.32 GHz frequency. While VCRO's control voltage is increased to 1.1 V, the circuit oscillates in 2.85 GHz frequency. It is observed that by increasing the control voltage made the circuit working in higher frequency without changing the oscillation output voltage, i.e., the amplitude remains constant with increasing frequency. The voltage gain of VCO ($Kvco$) *i*s given by

$$Kvco = \frac{fmax - fmin}{Vmax - Vmin} \quad (5)$$

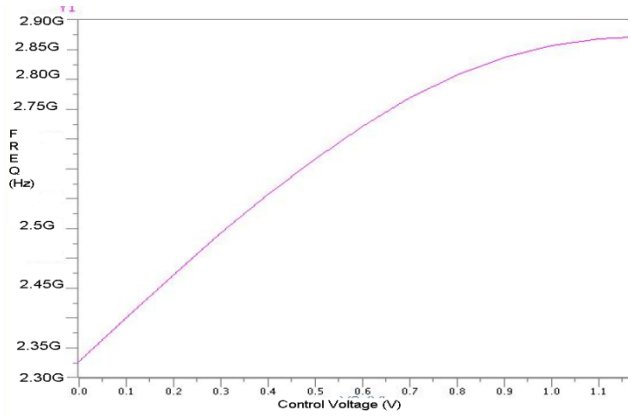

Figure 5. Simulated tuning range

A frequency-tuning ratio of 18.60% is attained from 2.32 GHz to 2.85 GHz. The gain of VCRO is achieved 480 MHz/V from (5). Since IEEE 802.11b protocol required 2.4 GHz to 2.5 GHz frequency, the proposed delay circuit will make the VCRO working on that frequency range

Copyright (c) IARIA, 2012. ISBN: 978-1-61208-213-4

which will be certainly a key component of readerless RFID transponder. It exhibits a single side-band phase noise of -112 dBc/Hz at 10 MHz offset frequency from a center frequency of 2.45 GHz shown in Fig. 6.

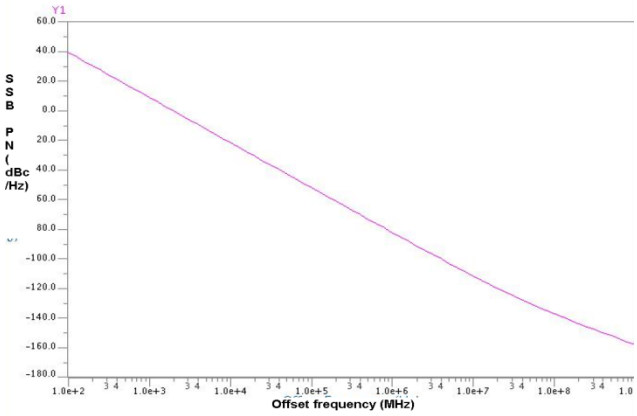

Figure 6. Simulated single side-band phase noise

TABLE I: PERFORMANCE COMPARISONS OF CMOS VCRO

Architecture	Center Frequency (GHz)	Tuning Range (GHz)	Supply Voltage (V)	Power (mW)	CMOS Process (µm)
4 stage, Dual delay loop [11]	0.9	0.75-1.2	3	-	0.6
2 stage, Single delay loop [12]	0.9	0.66-1.27	2.5	15.5	0.5
2 stage, Single delay loop [13]	0.9	0.73-1.43	1.8	65.5	0.18
4-stage , Dual delay loop [14]	-	1.77-1.92	1.8	13	0.18
3 stage, Single delay loop [**This work**]	2.45	2.2-2.85	1.8	11.25	0.18

Finally, the performance comparisons of CMOS VCRO of various technologies are shown in Table 1. Compared to other research works, it is shown that the proposed VCRO dissipates lowest power, which is around 11.25 mW and can operate in very high frequencies than others.

V. CONCLUSION AND FUTURE WORK

Despite the continuous improvement in the-state-of-the-art of CMOS VCOs', these devices still remain the most key blocks of RF PLLs. In this paper, a ring VCO has been proposed developed for active readerless RFID transponder. The simulated results showed that its operating frequency is 2.45 GHz, which will be compatible with the readerless RFID transponder and able to work with IEEE 802.11b protocol. In future, the research will be concentrated in the area of improving phase noise to increase the signal-to-noise ratio as well as improving figure of merit (FOM) of VCRO.

ACKNOWLEDGMENT

The authors would like to express sincere gratitude to the Ministry of Science Technology and Innovation (MOSTI) for supporting this research project through its MOSTI/BGM/R&D/20 (Brain Gain Malaysia) and UKM-AP-ICT-20-2010 (Arus Perdana) program.

REFERENCES

[1] Y. S. Hwang and H. C. Lin, "A new CMOS analog front end for RFID tags," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2299-2307, July 2009.

[2] V. Pillai, H. Heinrich, D. Dieska, P. V. Nikitin, R. Martinez, and K. V. S. Rao, "An ultra-low-power long range battery/passive RFID tag for UHF and microwave bands with a current consumption of 700 nA at 1.5 V," *IEEE Trans. Circuits Syst. I, Reg. Papers* , vol. 54, no. 7, pp. 1500-1512, July 2007.

[3] F. R. Labonnah, M. B. I. Reaz, M. A. M. Ali, Mohd. Marufuzzaman, and M. R. Alam, "Beyond the WiFi: Introducing RFID system using IPv6", in *Proc. of the Kaleidoscope: Beyond the Internet? - Innovations for Future Networks and Services, ITU-T*, pp.1-4, 13-15 December 2010, Pune, India.

[4] J. Jalil, M. B. I. Reaz, M. S. Amin, F. R. Labonnah, and Mohd. Marufuzzaman, "Development of 2.45 GHz analog front-end for readerless active RFID transponder", in *Proc. of Regional Engineering Postgraduate Conference (EPC)*, 6 pages, 4-5 October 2011, UKM, Bangi, Malaysia.

[5] M. Moghavvemi and A. Attaran, "Performance review of high-quality-factor, low-noise, and wideband radio-frequency LC-VCO for wireless communication," *IEEE Microw. Mag.*, vol. 12, no. 4, pp. 130-146, June 2011.

[6] O. Casha, I. Grech, and J. Micallef, "Comparative study of gigahertz CMOS LC quadrature voltage-controlled oscillators with relevance to phase noise," *Analog Integr. Circ. Sig. Process.*, vol. 52, no. 1-2, pp. 1-14, 2007.

[7] M. Moghavvemi and A. Attaran, "Recent advances in delay cell VCOs," *IEEE Microw. Mag.*, vol. 12, no. 5, pp. 110-118, August 2011.

[8] B. Leung, "A novel model on phase noise in ring oscillator based on last passage time," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51,no. 3, pp. 471–482, March 2004.

[9] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. of Solid-State Circuits*, vol. 34, no. 6, pp. 790-804, June 1999.

[10] Y. Toh and J. A. McNeill, "Single-ended to differential converter for multiple-stage single-ended ring oscillators," *IEEE J. of Solid-State Circuits*, vol. 38, no. 1, pp. 141-145, January 2003.

[11] C. H. Park and B. Kim, "A low-noise, 900-MHz VCO in 0.6-µm CMOS," *IEEE J. of Solid-State Circuits*, vol. 34, no. 5, pp. 586-591, May 1999.

[12] W. S. T. Yan and H. C. Luong, "A 900-MHz CMOS low-phase-noise voltage-controlled ring oscillator," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 2, pp. 216-221, February 2001.

[13] Z. Q. Lu, J. G. Ma, and F. C. Lai, "A low-phase-noise 900-MHz CMOS ring oscillator with quadrature output," *Analog Integr. Circ. Sig. Process.*, vol. 49, no. 1, pp. 27-30, 2006.

[14] Z. Z. Chen and T. C. Lee, "The design and analysis of dual-delay-path ring oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 3, pp. 470-478, March 2011.

Copyright (c) IARIA, 2012. ISBN: 978-1-61208-213-4