High Speed and Ultra Low-Voltage CMOS Carry Propagation Chain using Floating-Gate Transistors

Yngvar Berg
Department of Informatics
University of Oslo
Oslo, Norway
Email: yngvarb@ifi.uio.no

***Abstract*—Ultra low-voltage (ULV) CMOS logic for high-performance applications is presented. By applying floating capacitors we can increase the current level of MOS transistors for supply voltages below $500mV$. The current level of the transistors may be increased by a factor 40 for supply voltages below 0.3V. Simple NAND gates are presented using different topologies. The NAND gates are exploited to provide a high-speed and ultra low-voltage serial carry chain. Compared to conventional serial CMOS carry gates the delay is reduced by a factor 10 or more. Simulated data are based on *SpectreS* simulator provided by *Cadence* and are valid for 90nm TSMC CMOS process.**

***Keywords*-CMOS; Low-Voltage; Carry; High-Speed; Floating-Gate; Pass Transistors.**

I. INTRODUCTION

The demand for high-speed digital circuits is ever increasing. At the same time the supply voltages in modern CMOS processes are reduced in order to prevent transistor failure due to short channel effects. The low supply voltage is a challenge for high-speed circuit design. With the emergence of sensor and biomedical applications that require ultra low energy [1], [2], we have to adequately address design optimization near the minimum-energy point. It has long been established that for most logic families the minimum-energy point occurs in the subthreshold operational region of the MOS transistors and that the value of the minimum energy is set by leakage current.

Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. The general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of high-speed circuits. The supply voltage region addressed in this paper is between $200mV$ and $400mV$. In this region traditional CMOS logic design is hampered with subtreshold current which both reduces the circuit speed and robustness. In the approach presented in this paper the main transistors are operating above the threshold voltage for ultra low supply voltages. For a supply voltage equal to $300mV$ the delay of the proposed carry gates is reduced to less than 10% of a conventional CMOS carry gate while the noise margin is increased due to an enhanced current level. The delay variation is reduced accordingly due to large driving currents. The energy required to drive the gates are comparable to conventional CMOS [3].

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay is of great interest for the implementation of modern digital systems. Arithmetic circuits, like adders and multipliers, are also one of the basic components in the design of communication circuits.

The ultra low-voltage circuits presented in this paper are derived from digital floating-gate circuits [4]. In Section II, we introduce ultra low-voltage semi-floating-gate logic and compare the performance to conventional, i.e., complementary CMOS. ULV NP domino inverters are described and the potential delay reduction and increased performance in terms of minimum-energy-point (MEP) is presented. In Section III, we present novel ULV NAND and AND gates using enhanced pass transistors. Different ultra low-voltage carry gates are presented in Section IV. The high-speed ULV carry gates can be used in simple serial adders to reduce the complexity of parallel conventional CMOS adders for supply voltages below $500mV$.

II. ULTRA-LOW-VOLTAGE SEMI-FLOATING-GATE LOGIC

The ULV logic styles presented in this paper are related to the ULV domino logic style presented in [5]. The main purpose of the ULV logic style is to increase the current level for low supply voltages without increasing the transistor widths. We may increase the current level compared to complementary CMOS using different initialization voltages to the gates and applying capacitive inputs. The extra loads represented by the floating capacitors are less than extra load given by increased transistor widths. The capacitive inputs

 ISBN: 978-1-61208-302-5

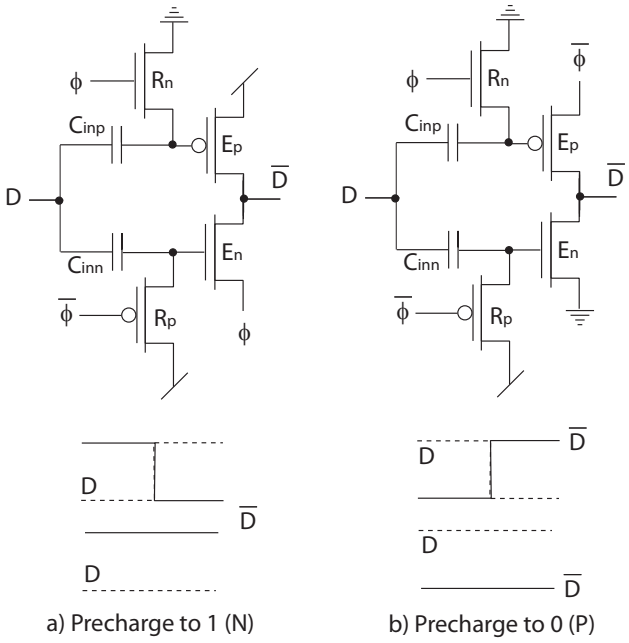

Figure 1: ULV domino inverters.

lower the delay through increased transconductance while increased transistor widths only reduce parasitic delay. Furthermore, the accuracy of the capacitor values are not critical and the process variations and temperature will only have a significant impact on the transistor currents through the high relative transconductance in the subthreshold region. The ULV logic styles may be used in critical sub circuits where high speed and low supply voltage is required. The ULV logic styles may be used together with more conventional CMOS logic and will require a specialized CMOS process. The floating capacitors can be either poly-poly, metal-metal or MOS parasitics.

The simple dynamic edge and level ULV inverters [5] are shown in Figure 1. Apply a clock signal to power the inverter, i.e., either ϕ to E_n to and V_{DD} to E_p, or $\overline{\phi}$ to E_p and GND to E_n and precharge to 1 or 0 respectively. The gate resembles NP domino logic. In order to hold the precharged value until an input transition arrives the E transistor connected to a supply voltage is made stronger than the other E transistor. The function of the inverter can be described as $\overline{O} = \overline{A}D$

The different ULV logic styles are defined by the applied terminal inputs as shown in Table I. ΔV is the output voltage swing. The simple model for the noise margin NM' is given by the ratio of the ON current and the OFF current. The capacitive division factor, $\frac{Cin}{CT}$ where C_T is the total capacitance seen by a floating gate is assumed to be 0.5. The delay is relative to a standard complementary CMOS inverter. The ON and OFF currents of a complementary CMOS inverter is given by the effective gate source voltages V_{DD} and $0V$ respectively. Assuming $\frac{Cin}{CT} = 0.5$ where C_T is the total capacitance seen by a floating gate, we may estimate the delay, dynamic and static power and noise margins of the different ULV logic styles relative to a complementary CMOS inverter.

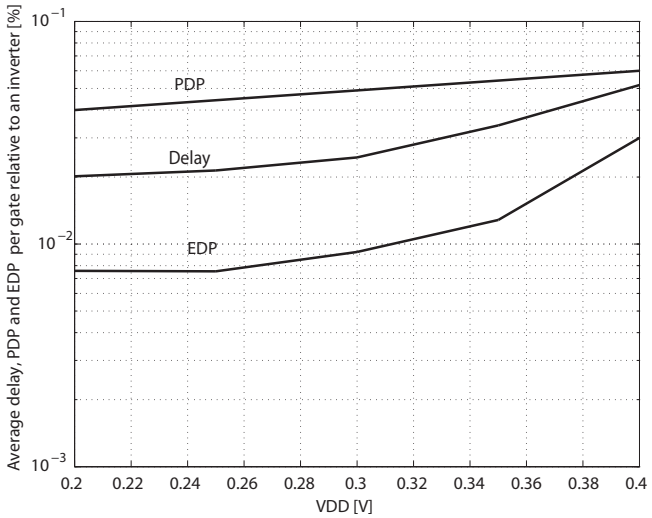

Figure 2: Performance.

The ULV domino inverters can exploited to improve speed for ultra low supply voltages. Relative delay, Power-Delay-Product (PDP) and Energy-Delay-Product (EDP) for ULV inverter compared to complementary CMOS is shown in Figure 2, the delay for supply voltages below 0.4V can be reduced to less than 5%.

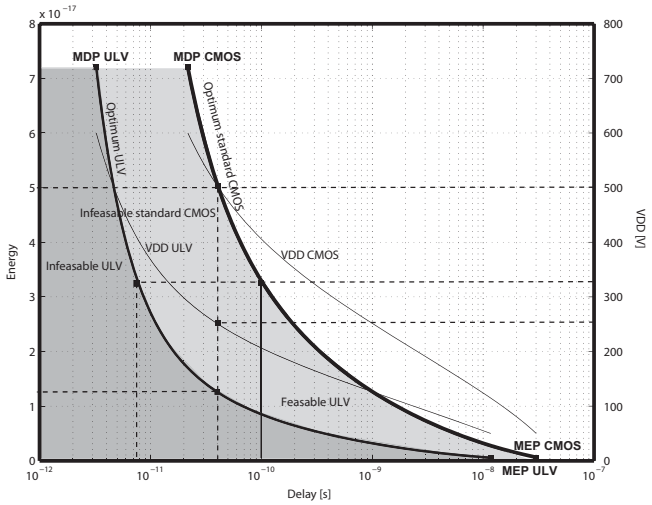

Figure 3: Energy delay trade-off, complementary CMOS and ULV.

The optimum energy-delay trade-off in standard CMOS logic, shown in Figure 3, is traditionally close to the minimum-delay point (MDP). The region left of the optimum energy-delay curve is not feasible for conventional or standard CMOS logic. By applying a current boost provided

Table I: ULV LOGIC STYLES

ΔV	E_p	E_n	$V_{gs}\ I_{ON}$	$V_{gs}\ I_{OFF}$	NM'	Relative delay	Style	Comment
$\pm\frac{V_{DD}}{2}$	$\overline{\phi}$	ϕ	$\frac{5V_{DD}}{4}$	$\frac{3V_{DD}}{4}$	$\frac{V_{DD}}{2}$	$\approx 10\%$	DU	Dynamic
V_{DD}	$\overline{\phi}$	GND	$\frac{3V_{DD}}{2}$	$\frac{V_{DD}}{2}$	V_{DD}	$\approx 5\%$	DNU	Dynamic prech. 0
$-V_{DD}$	V_{DD}	ϕ	$3\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2}$	V_{DD}	$\approx 5\%$	DPU	Dynamic prech. 1

by the ULV logic the optimum energy-delay curve is moved to the left in Figure 3, which yields a significant reduction in delay for low supply voltages or a specific energy level. The improvement of the current boost can be exploited in different ways. Firstly, we can for a specific ultra-low supply voltage obtain significant speed improvement. For example, assuming a supply voltage equal to 330mV the delay can be reduced to approximately 5% compared to standard CMOS at the same energy level. Secondly, if a system is required to operate at a certain speed, we can for meet the speed requirement for a lower supply voltage for the ULV logic than for standard CMOS. Assuming a gate delay equal to 40ps, the required supply voltage for standard CMOS is 500mV whereas the required supply voltage for the ULV logic is 250mV. The energy consumed by the ULV logic will be approximately 25% compared to standard CMOS. Hence, the ULV transistors can be exploited for ultra low-voltage and high-speed design and ultra low-voltage low-energy design.

III. ULV AND AND NAND GATES

Different applications of the ULV domino inverter is shown Figure 4. The inverters can be used to implement AND2 and NAND2 functions by using one of the inputs to set the precharge level. The gates in Figure 4 can be described as a pass transistor with an increased current level. The delay of the gates are dependent on the input delay. If we consider the gate in a) we observe that the evaluate transistor E_n acts as a pass transistor for the input $\overline{B}$ when $\overline{B}$ switches from 1 to 0 and the other input A switches from 0 to 1. The delay of the AND2 and NAND2 gates are less than 8% of a standard complementary NAND gate for supply voltages below $500mV$. For a supply voltage equal to $300mV$ the delay of a NAND2 gate is 310ps whereas the delay for a complementary NAND2 gate is more than 6ns.

The different configurations of the AND/NAND ULV gates are given in Table II. Consider the NAND gate in Figure 5 a). The response of the gate is depending on the closk signals and inputs:

- Figure 5 b) $\phi = 1$, precharge. The output is precharged to 1 and the gate of the evaluate transistor E_n and E_p are recharged to 0 and 1 respectively. The input A is precharged to 0 and the input $\overline{B}$ is precharged to 1.
- Figure 5 c) $\phi = 1$ and $A = 0$ (no change) and $\overline{B} = 1$ (no change). The gate of the evalluate transistors are not changed and the output remains high.

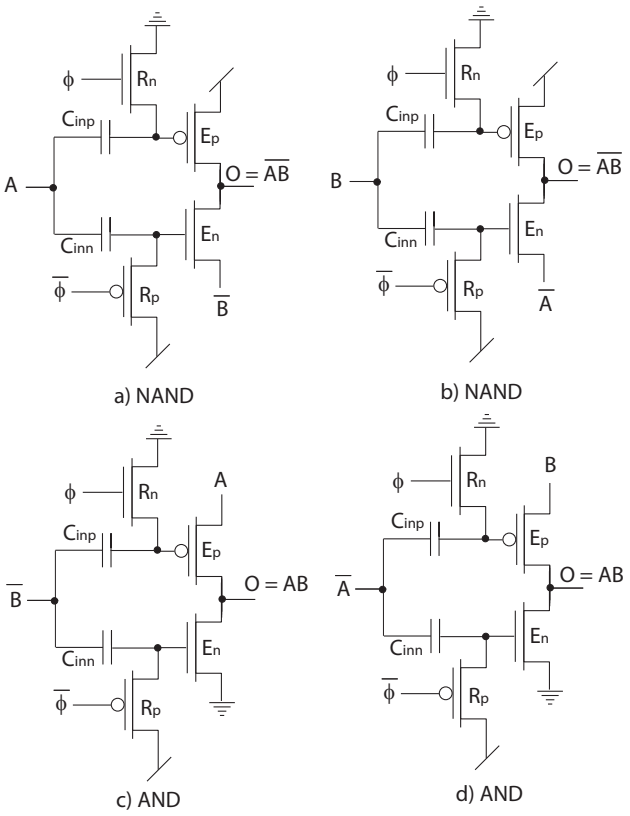

Figure 4: ULV domino AND and NAND gates.

- Figure 5 d) $\phi = 1$ and $A = 0$ (no change) and $\overline{B} = 0$ (transition).The output remains high due to a strong pMOS evaluate transistor E_p.
- Figure 5 e) $\phi = 1$ and $A = 1$ (transition) and $\overline{B} = 1$ (no change). The nMOS evaluate transistor E_n is enhanced and the pMOS evaluation transistor E_p is weakened. The output will not be affected by this condition.
- Figure 5 f) $\phi = 1$ and $A = 1$ (transition) and $\overline{B} = 0$ (transition). The nMOS evaluate transistor E_n is enhanced and the pMOS evaluation transistor E_p is weakened and the ouput will be pulled to GND (0) by an enhanced nMOS evaluate transistor.

An alternative and simplified NAND gates using an ULV pass transistor is shown in Figure 6 a). The NAND gate in recharge/precharge mode, i.e., output precharged to 1 and inputs B and $\overline{A}$ precharged to 0 and 1, is shown in b) and the simplified circuit equivalents for different inputs are shown

Table II: DIFFERENT CONFIGURATIONS

A	B	O	Function
A	$\overline{B}$	O	a)
0	0⇓	1	NAND
0	1	1	NAND
1⇑	0⇓	0⇓	NAND
1⇑	1	1	NAND
$\overline{A}$	B	O	b)
0⇓	0	1	NAND
0⇓	1 ⇑	0⇓	NAND
1	0	1	NAND
1	1 ⇑	1	NAND
A	$\overline{B}$	O	c)
0	0⇓	0	AND
0	1	0	AND
1⇑	0⇓	1⇑	AND
1⇑	1	0	AND
$\overline{A}$	B	O	d)
0⇓	0	0	AND
0⇓	1 ⇑	1⇑	AND
1	0	0	AND
1	1 ⇑	0	AND

in Figure 6 c) to f). For input $\overline{A} = 1$ (no change) shown in c) and d) the output will remain high. Details of operation are:

- Figure 6 c) $B = 0$ (no change) and $\overline{A} = 1$ (no change). The output remains high unless some other circuitry pull the output down to 0 by an enhanced nMOS transistor. If so the gate of the evaluate transistor will be pulled to 0 and turn off the evaluate transistor E in order to prevent the output to affect the input $\overline{A}$.
- Figure 6 d) $B = 1$ (transition) and $\overline{A} = 1$ (no change). The evaluate transistor E is enhanced and the output will remain high unless some other circuitry pull the output down to 0 by an enhanced nMOS transistor. If so the gate of the enhanced evaluate transistor will be pulled to 0 and turn off the evaluate transistor E in order to prevent the output to affect the input $\overline{A}$.
- Figure 6 e) $B = 0$ (no change) and $\overline{A} = 0$ (transition). The evaluate transistor E is not enhanced and the output may be pulled to 0 or remain high depending on other circuitry. If there are no other transistor driving the output, the output will be pulled slowly towards 0. The time constant for the pull-down is however much higher than the time constant for an active pull-down by an enhanced evaluate transistor.
- Figure 6 f) $B = 1$ (transition) and $\overline{A} = 0$ (transition).The output is pulled to 0 by the enhanced evaluate transistor E.

IV. ULV CARRY GATES

We can use the NAND gates shown in Figure 4 to implement a high speed ULV carry function. By combining three NAND2 gates we obtain the carry defined by $\overline{C_{out}} = \overline{AB} + \overline{AC_{on}} + \overline{BC_{in}}$. Furthermore, we may assume that the inputs A and B will arrive prior to the carry input signal in a serial carry propagation chain. By applying the A and B inputs to the source of the evaluate transistors we minimize the worst case propagation delay. If $A \neq B$ the carry output is only dependent on the carry input, which is the worst case scenario for a serial adder.

A ULV carry gate is shown in Figure 7. By using 3 ULV NAND gates from Figure 4 we can implement the

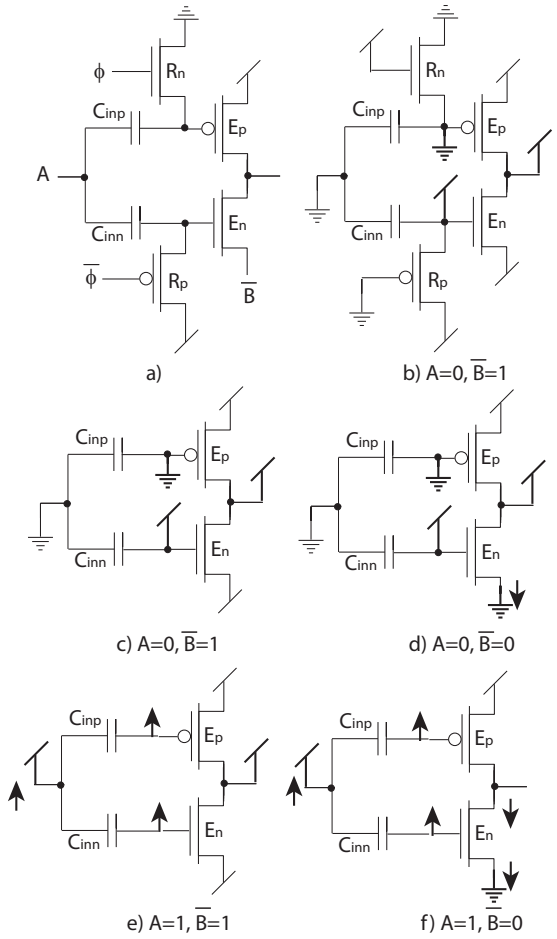

Figure 5: Simplified circuit equivalents for the NAND gate.

Table III: TRUTH TABLE FOR CARRY GATE

C_{in}	A	B	$\overline{A}$	$\overline{B}$	$\overline{C_{out}}$	C_{out}
0	0	0	1	1	1	0
0	0	1 ⇑	1	0 ⇓	1	0
0	1 ⇑	0	0⇓	1	1	0
0	1 ⇑	1 ⇑	0⇓	0⇓	0⇓	1 ⇑
1 ⇑	0	0	1	1	1	0
1 ⇑	0	1 ⇑	1	0⇓	0⇓	1 ⇑
1 ⇑	1 ⇑	0	0⇓	1	0⇓	1 ⇑
1 ⇑	1 ⇑	1 ⇑	0⇓	0 ⇓	0⇓	1 ⇑

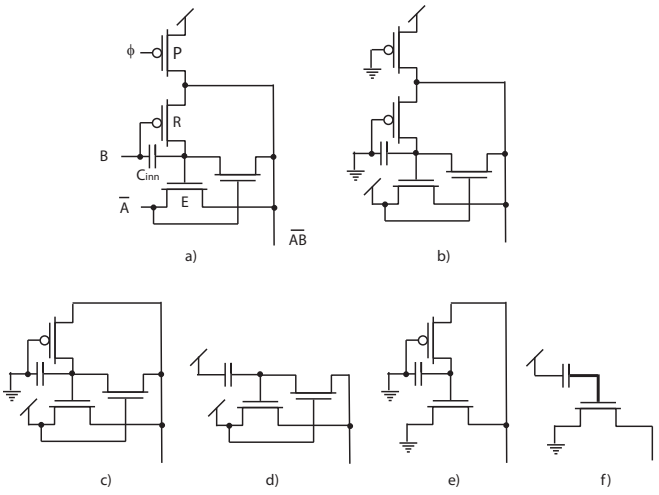

Figure 6: NAND ULV pass transistor gates.

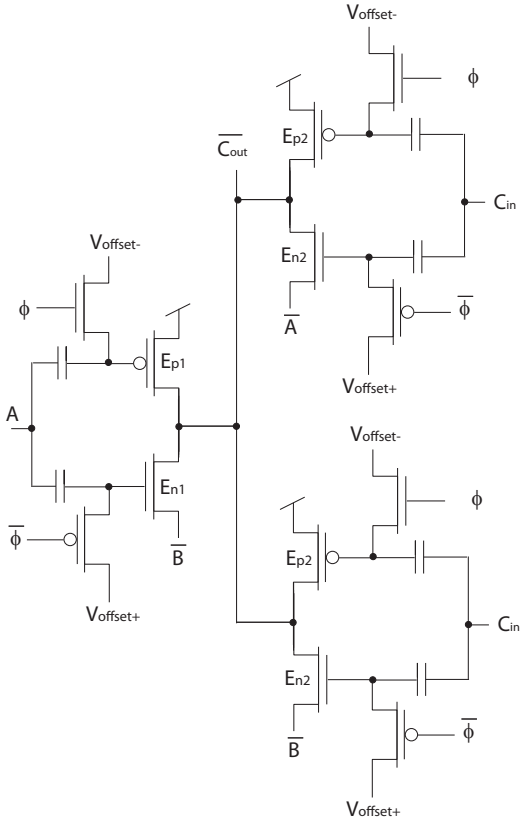

Figure 7: $\overline{C_{out}} = \overline{AB + AC_{in} + BC_{in}}$.

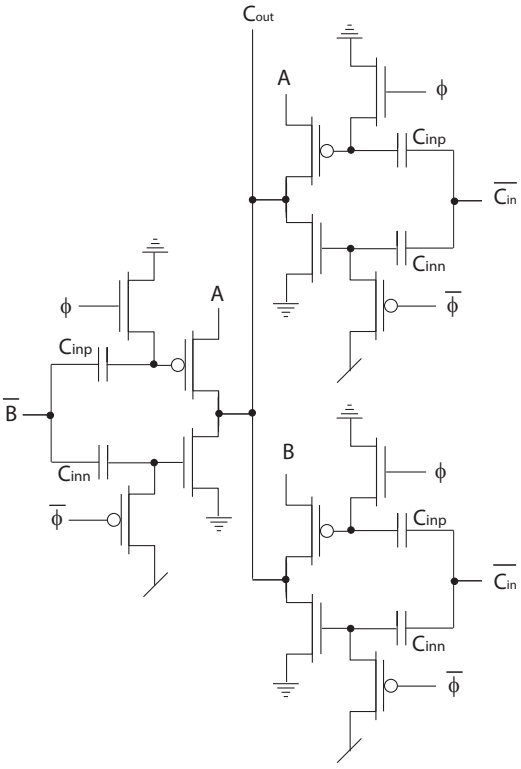

Figure 8: $C_{out} = AB + AC_{in} + BC_{in}$.

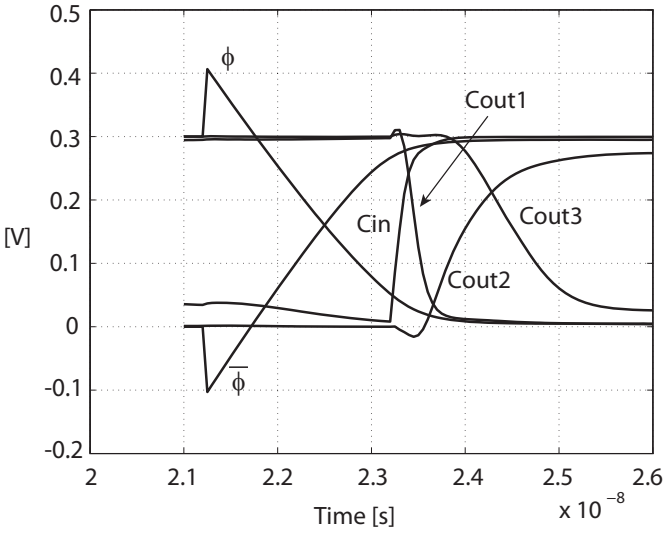

Figure 9: Preliminary simulation data for the ULV carry chain.

carry invert function. The carry input C_{in} is applied to the evaluate transistors of two NAND gates. The output carry is precharged to logic one whereas the input carry is recharged to 0. Alternate carry bits have different polarities, as shown in Figure 8. The truth table is shown in Table III.

Preliminary simulation data for the ULV carry chain using the carry gates in Figures 7 and 8 is shown in Figure 9. The clock signal ϕ and $\overline{\phi}$ are provided by large complementary inverters and the large fall and rise time compared to the ULV carry gate of these signals are evident. The delay through a complementary inverter is $2.2ns$ and the delay for a complementary carry gate is more than $5ns$ for a supply voltage equal to $300mv$. The delay for the ULV carry chain is $175ps$ for bit 1, $501ps$ for bit 2 and approximately $650ps$

 ISBN: 978-1-61208-302-5

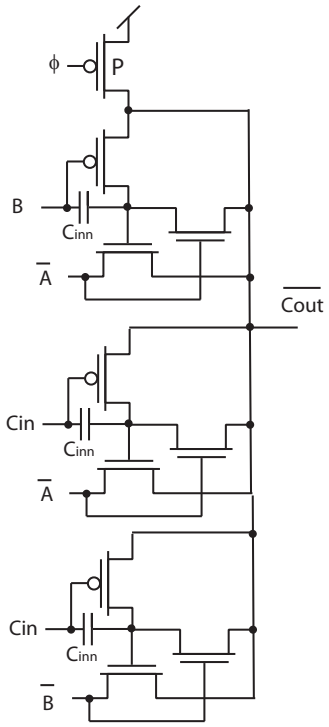

Figure 10: Alternative carry gate using pass transistor.

for the following bits.

An alternative carry gate exploiting the NAND gates in Figure 6 is shown in Figure 10. This gate has less transistors and less capacitive input load than the carry gate in Figure 7. The carry input signal is used to initiate the precharge the output, hence the output will be precharged to 1 until the input carry signal arrives unless the carry output is pulled to 0 by $A = B = 1$. Note that the carry signals is only applied to recharge transistors and input capacitors and not as pass inputs. The carry input is precharged to 0, which turns on the recharge transistors. In the same phase, the output is precharged to 1 while the inputs $\overline{A}$ and $\overline{B}$ are precharged to 1.

V. Conclusion

The potential of ultra low-voltage domino and pass transistor CMOS has been presented. Different NAND and AND gates have been presented and are applied in ULV carry chains. Preliminary simulation results shows potential speed improvement of the proposed carry gates compared to complementary CMOS by a factor of 10 or more. Simulated data are based on *SpectreS* simulator provided by *Cadence* and are valid for 90nm TSMC CMOS process.

References

[1] A.P. Chandrakasan, S. Sheng and R.W. Brodersen, “Low-power CMOS digital design” , IEEE Journal of Solid-State Circuits, Volume 27, Issue 4, April 1992 Page(s):473 - 484

[2] N. Verma, J. Kwong and A.P. Chandrakasan, “Nanometer MOSFET Variation in Minimum Energy Subthreshold Circuits” , IEEE Transactions on Electron Devices, Vol. 55, NO. 1, January 2008 Page(s):163 - 174

[3] . Berg and O. Mirmotahari, ”Novel high-speed and ultra-low-voltage CMOS NAND and NOR domino gates ”, In CENICS 2012: The Fifth International Conference on Advances in Circuits, Electronics and Microelectronics. International Academy, Research and Industry Association (IARIA). ISBN 978-1-61208-213-4. Chapter. s 5 - 10.

[4] Y. Berg, D.T. Wisland and T.S. Lande, “Ultra Low-Voltage/Low-Power Digital Floating-Gate Circuits”, IEEE Transactions on Circuits and Systems, vol. 46, No. 7, pp. 930–936,J uly 1999.

[5] Y. Berg,“Novel Ultra Low-Voltage and High Speed Domino CMOS Logic”, In proc. IEEE/IFIP International Conference on VLSI and system-on-Chip (VLSI-SoC), Madrid 27-29 September 2010.

 ISBN: 978-1-61208-302-5