Robustness of the Ultra Low-Voltage Domino Gates CMOS

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***Abstract*—In this paper, we elaborate on the dimensioning of the ultra low voltage gate with keeper. We compare the gate configuration to ULV5 and demonstrate the potential and weaknesses of the new gate configuration with the keeper. We also pinpoint the crucial signal paths (mainly regarding the clock drivers) while also providing an overview of the propagation through a chain of gates.**

Keywords-NP domino logic; ultra low voltage; floating-gate; CMOS, high-speed; clock drivers; 90 nm process.

I. INTRODUCTION

For decades, technology has been driven by scaling the size of the transistor. We have evolved a fabrication process to reduce the size from several micrometres (μm) to tens of nanometres (nm). The heart of technology is the transistor and it has been one of the key components that has allowed the plethora of portable electronic gadgets that enrich our everyday lives. Unfortunately, millions of transistor chips fabricated using modern processes suffer from very low yields (<50%) [1]. Meanwhile, the consumer market has dramatically increased demand for sophisticated portable electronics, such as handheld computers and smart-phones.

Portable electronics drive the need for low power and low voltage due to a limited budget set by a fixed maximum battery mass. Soon, we will see research toward embedded circuits in human bodies and the need to harvest energy will become more evident. Several approaches exist to lower the energy consumption. One of the most fundamental and effective approaches is to lower the supply voltage [2], [3], [4]. When the supply voltage is reduced to hundreds of millivolts, it is known as Ultra Low Voltage (ULV) [5], [6]. However, scaling of the supply-voltage has an adverse effect on the speed of operation of the design. The main challenge is to obtain high speed at supply-voltages that are as low as possible. To maintain good response times at ultra low supply voltages, the threshold voltages of the transistors must also be reduced [7]. Unfortunately, this requires a change to the CMOS fabrication process. The multiple-V_{dd} technique has been proposed for low voltage high performance circuit designs [8] without the need to change the fabrication process. Floating-Gates (FG) have also been proposed for ULV and Low Power (LP) logic [9]. Unfortunately, modern processes face significant gate leakage due to the thin oxide. A ULV floating-gate inverter employing a frequent recharge technique has shown good properties for achieving high speed at ultra low voltages [10] Even though the ULV gate has shown good performance it also has limitations, due the leakage at the semi-floating-gates (SFG). A differential ULV gate has been proposed which includes a keeper function [11]; it is argued to have the speed of an ULV but the stability of a standard CMOS gate.

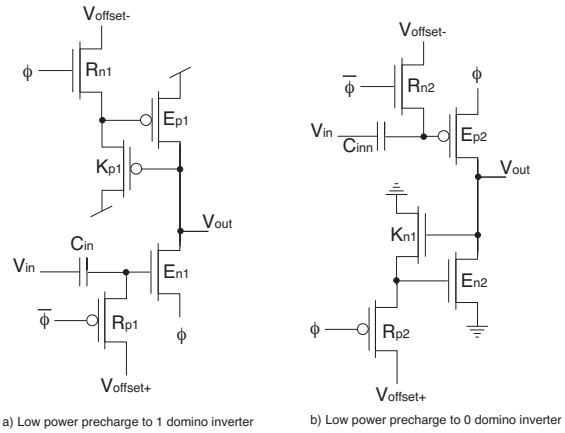

Figure 1. Low power ULV inverter based on domino logic with floating-gate. This gate configuration is known as ULV5 (the fifth modification). The symbols are recharge transistor (R_{p} and R_{n}), evaluation transistor (E_{p} and E_{n}), keeper transistor (K_{p} and K_{n}), clock signal (ϕ).

In this paper, we elaborate more on the attributes of the ULV gate and its modification to resemble a precharge logic. Furthermore, we discuss the inclusion of a keeper transistor that enables reduction of the static power consumption. The main aim of this paper is to evaluate the advantages and reliability that the modification allows in terms of delay response, transistor matching and power consumption. We also discuss secondary effects such as clock driver dimensioning.

The structure of this paper is as follows: in Section II, the ULV5 and the keeper transistor modification of the ULV structure are presented. In Section III, a discussion of the results achieved is given. Finally, the paper concludes by

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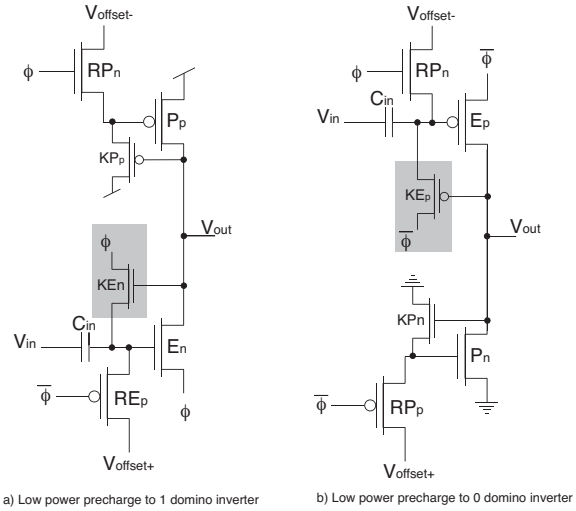

Figure 2. The ULV5 gate is modified by adding a keeper transistor (KE_n and KE_p) to the evaluation transistors, highlighted in the gray box.

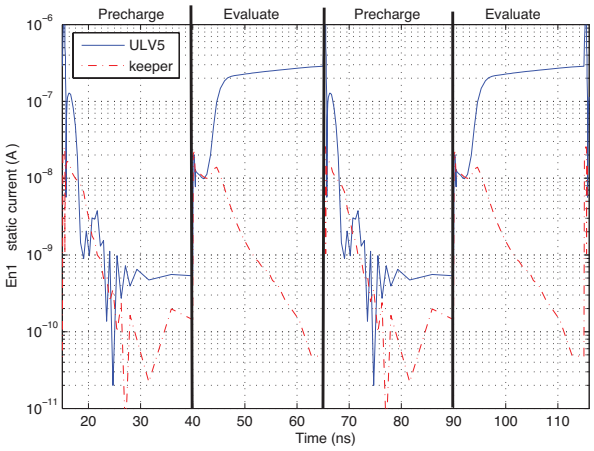

Figure 3. Simulation of a ULV5 with keeper. The plot shows the current dissipation through the *En* for the input signal with no transition (presented in section II(a).

highlighting the optimal design parameters. The simulation results demonstrated throughout this paper were obtained using a simulation produced in a TSMC 90 nm process environment provided by Cadence.

II. Ultra Low Voltage Gate with Keeper

The ULV gates have been presented in five evolution steps, from ULV1 to ULV5 [12], [13]. The most recent modification of ULV5 is presented in [12], with an additional improvement made by adding a keeper transistor to the evaluation transistor in the N- and P-domino logic gates. The ULV5 without the keeper transistor is illustrated in Figure 1, while modification of the gate with the keeper transistor is illustrated in Figure 2. The keeper transistors (KE_n and KE_p) are highlighted in gray. Considering Figure 2(a), the transistor KE_n would contribute to weaken the pull-down transistor (E_n) when the output (V_{out}) is to be kept high (V_{dd}). The signal flow for a precharge 1 domino inverter with the keeper transistors would be as follows, for input with:

(a) **Non-transition** - The output is to be kept high. The KE_n would be turned off, the gate of P_p would be low (0) and hence V_{out} is held high through P_p to V_{dd} . The feedback from the keeper transistor KE_n would pull the floating-gate at the input of E_n to the source of the KE_n, which, at the time, would be 0 (ϕ= 0). Given time, the keeper transistor KE_n would turn the En completely off and moreover significantly lower the static power consumption during the evaluation period.

(b) **Positive transition** - The output would, as a result of the input transition, be pulled towards 0 through the E_n-transistor. As the output V_{out} decreases, the feedback keeper KP_p-transistor would increasingly turn on and contribute to the shut-down of the pull-up transistor P_p. In turn, this would increase the speed of pulling V_{out} to 0. The more V_{out} is lowered, the weaker the keeper transistor KE_n contribution to the floating-gate at the E_n.

The main improvement made by adding the keeper transistor is the significant decrease of static power consumption. This is primarily due to the shut-down of the evaluation transistor, which competes with the precharge transistor during the evaluation period for a non-transition input. The current consumption during a clock cycle for a non-transition input for both the ULV5 and the ULV5 with keeper configurations is shown in Figure 3. The simulation results show that the keeper configuration has a current dissipation factor approximately 10,000 times lower through the E_n.

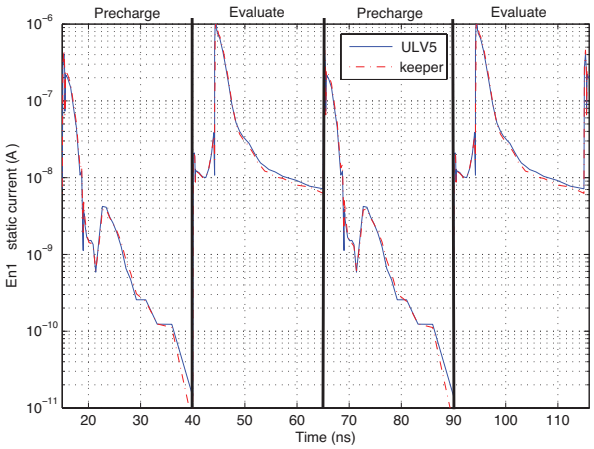

Figure 4. The simulation of a ULV5 with keeper. The plot shows the current dissipation through the *En* for the input signal with a positive transition (Section II(b).

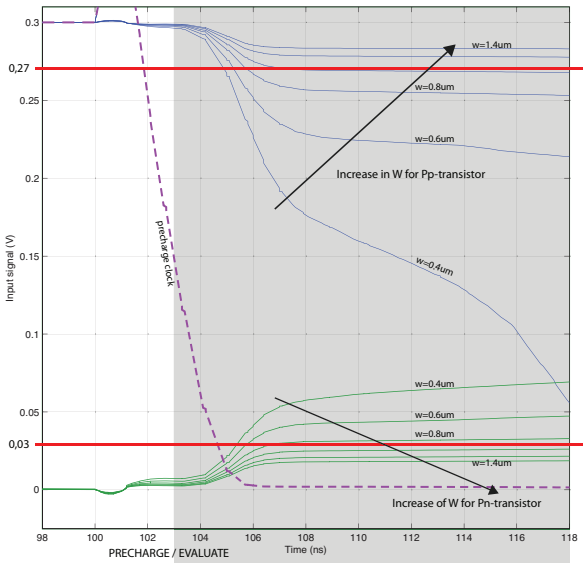

Figure 5. Parametric simulation with changes based on the width of the precharge transistors. The plot shows the evaluation period for a ULV5 (without keeper), and its ability to hold the output (V_{out}) for the case of a non-transition at the input (Section II(a)).

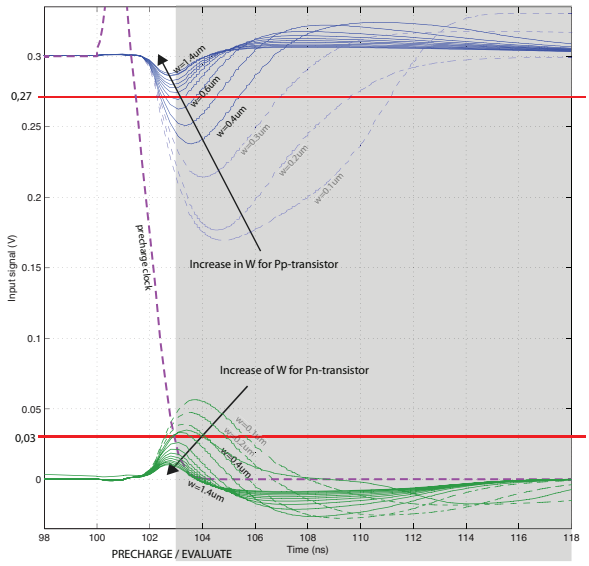

Figure 6. Parametric simulation for the ULV5 with keeper. The width of the precharge transistors are parameterised for the case of a non-transition at the input during an evaluation period. This plot is based on the same simulation environment as for the ULV5 without the keeper, shown in Figure 5.

During the precharge period, the current dissipations are different due to the starting point of the floating-gates and the specific DC voltage at the output V_{out}. For a positive input transition the current dispassion is equal, hence the high speed of the gate is ensured. The simulation result for the gate with a positive transition is shown in Figure 4. The ULV5 with keeper configuration is therefore a great improvement in terms of static power, while all other beneficial attributes are maintained compared with standard CMOS. In the following section, we are to elaborate on the details of the different elements within the gate. We aim to analyse which dimension gives the best overall effect.

Table I
THE TRADE-OFF FOR DELAY AND LOAD FOR THE ULV5 WITH KEEPER.

(μm) Ci	Time (ns) In 50%	Out 50%	(ns) Delay
0.5	-	-	-
1.0	5.81	7.30	1.49
1.5	5.58	5.96	0.38
2.0	5.47	5.73	0.26
2.5	5.41	5.62	0.21
3.0	5.38	5.56	0.18
3.5	5.35	5.51	0.16
4.0	5.33	5.48	0.15
4.5	5.32	5.46	0.14
5.0	5.31	5.44	0.13
5.5	5.30	5.43	0.13

III. SIMULATION RESULTS AND DISCUSSION

We start by elaborating on the effect of the capacitive input to the gates. The dimension of the input capacitance (C_i) directly affects the gate by attenuating the transition (the input voltage swing) and thus increasing the delay. The lower C_i is, the more significant the role the parasitic gate-capacitances play. The higher C_i is, the higher the load (C_L) that is required to burden the previous gate. Therefore, there should be a trade-off between the amount of parasitic capacitance and the load. Our parametric simulation for the gate with keeper configuration considering parameterisation of C_i is shown in Table II, with focus on the gate delay. From the table, we have chosen to use a 2.5 fF input capacitance. The input capacitance for the N- and P-domino gates has different input gates, hence nMOS and pMOS; therefore considerations must be made regarding matching of the nMOS and pMOS transistors for both evaluation and precharge. Transistor matching for the nMOS and pMOS for these low supply voltages (V_{dd}) has different mobility abilities. Matching of the nMOS and pMOS for a standard CMOS inverter is shown in Table II. The dimensions of the evaluation transistors are preferably kept at a minimum, especially concerning matching of the C_i. This leads to the dimensioning of the precharge transistors, hence these directly affect the matching of the evaluation-transistors and the precharge through relative values. The other side-effect of changing the precharge transistors is the fact that the

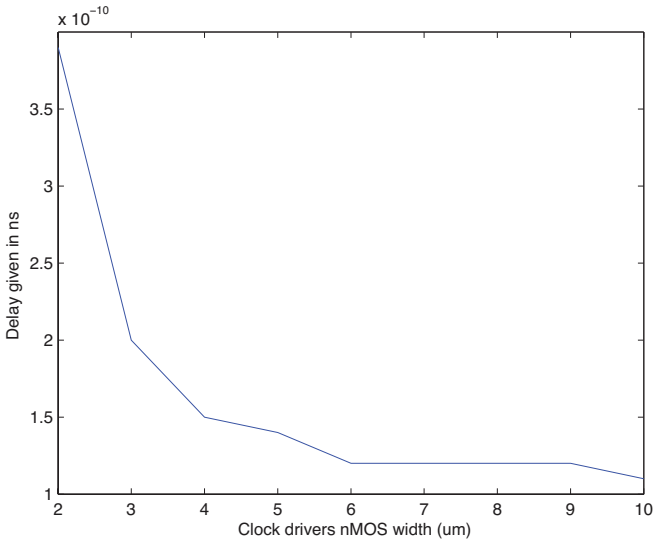

Figure 7. Simulation plot regarding the delay of the clock drivers dependency on the width of the nMOS of the clock driver.

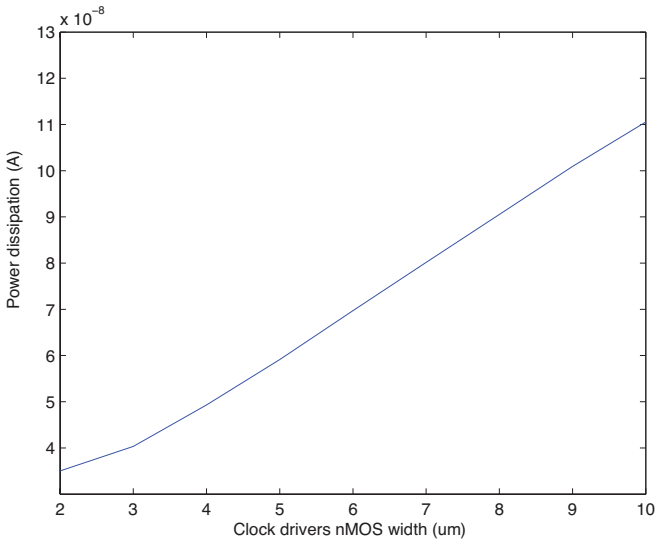

Figure 8. Simulation plot for the power dissipation through the clock driver for the specified gate based on the parameterised width of the nMOS.

precharge delay would be either longer or shorter. The delay in precharge (isolated) is of no concern due to the fact that we can use a skew clocking strategy, and the only aspect of importance is the DC value of the level, either V_{dd} or ground. The other consideration when dimensioning the precharge-transistors is their ability to hold the signal. This is of particular importance for the ULV5 configuration. As shown in Figure 5, the larger the width of the precharge transistor the better, and the longer it holds the output value in the case of a non-transition. For the ULV5 with the keeper configuration, shown in Figure 6, we see that holding of the value is of no concern. We would particularly like to stress the fact that a ULV5 with keeper can actually have a configuration with width of the precharge transistor as small as 100 nm. In this case, we are able to lower the area consumption for an overall perspective. One potential issue which needs to be addressed is that, contrary to CMOS domino logic, the clock signals (drivers) play a more dominant role. The clock signals are not only connected to the gate node of the transistors, but also to the drain/source of the evaluation transistors, specifically to the E_n, E_p, KE_n and KE_p transistors. Hence the clock drivers must be strong enough to not become a bottleneck for the evaluation. The most crucial path is for the E_n and E_p. In Figure 9, the critical path is shown in red. In the case shown in Figure 9(a), of an evaluation for a positive transition at the input, the evaluation transistor E_n must pull the output V_{out} down to ground. The critical path shows that the nMOS of the clock driver has a bottleneck issue; it must be large enough to pull through all the current dissipation and at the same time not increase the overall power dissipation. Our simulation results indicate that the optimal size for the nMOS width of the clock-driver is 4.0μm , with a length of 200 nm. The pMOS is kept minimum, thus the pull-up and pull-down of the clock driver is skew matched. Figure 7 shows the effect of the delay of the gate with regard to the increase in the width, while in Figure 8 illustrates the power consumption through the same node. Figure 10 and Figure 11 show the energy (PDP) and the EDP, respectively.

Width (μm)	
pMOS	nMOS
0.50	0.57
1.00	1.15
2.00	2.95
3.00	4.85
4.00	6.80
5.00	8.80
6.00	11.00

Table II
MATCHING OF THE NMOS AND PMOS FOR A STANDARD CMOS INVERTER GATE, SIMULATED WITHIN THE SAME CONDITIONS AS THE REST OF THE GATES IN THIS PAPER. THE SUPPLY VOLTAGE IS SET TO 300 MV.

IV. CONCLUSION

In this paper, we have elaborated on the matching and dimensioning of different elements of the ULV gate. We have demonstrated the potential improvement concerning static power dissipation of the ULV5 with keeper configuration compared with the unmodified ULV5. Furthermore, we have discussed the importance of the clock drivers dimensions. In particular, we have considered the issue of bottlenecks for

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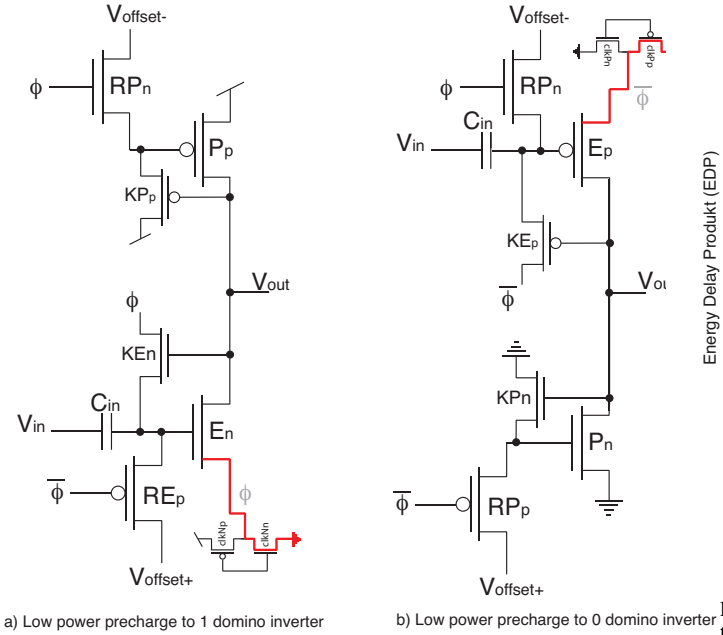

Figure 9. The ULV5 with keeper domino gate, with single clock driver. The highlighted critical path is shown in red.

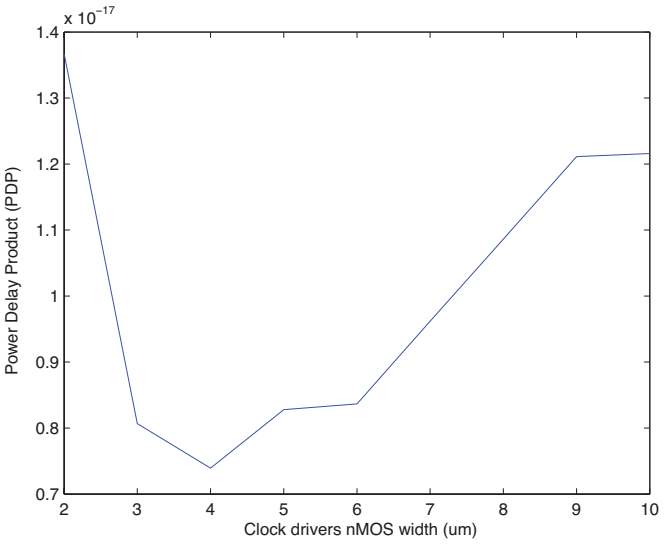

Figure 10. Simulation plot for the calculated energy (PDP) dissipation for the clock driver based on the parameterised width of the nMOS.

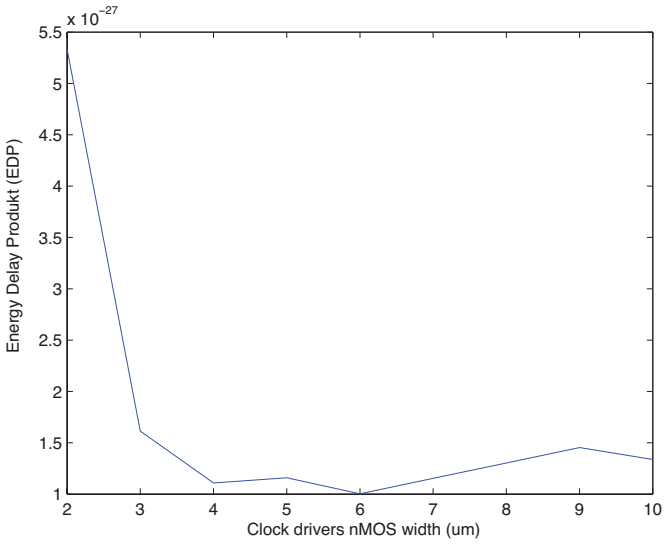

Figure 11. Calculated values for the EDP for different widths of the clock drivers nMOS.

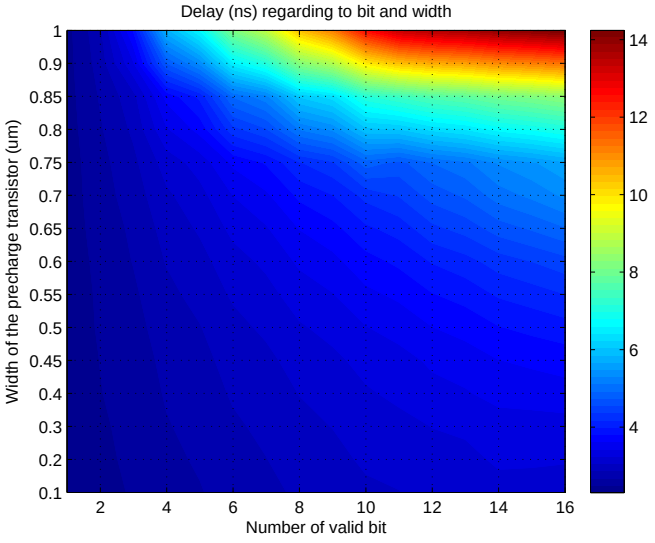

Figure 12. The ULV5 without the keeper is simulated to plot the relation between number of bits in a chain and the width of the precharge transistor. The delay is given in ns. The evaluation transistor size is kept minimal.

the evaluation transistors. The optimal values obtained in this work are Ci=2.5 fF, and the width of the clock driver (crucial path) is 4.0μm , with a length of 200 nm. The supply voltage was 300 mV and all transistors were kept to a minimum size except for the precharge transistor. The optimal dimensions for the precharge depend on the delay and the length of the chain used for each design. For the ULV5 without the keeper, we have simulated the relationship between the number of bits in a chain and the width of the precharge transistor. The delay is plotted in Figure 12, and the representative hold time (the time-slot which holds the output value valid) is shown in Figure 13. Finally, Figure 14 shows the valid bits and the same configurations. There was a significant improvement for the ULV5 with keeper, especially in holding a value valid, resulting in a higher bit chain.

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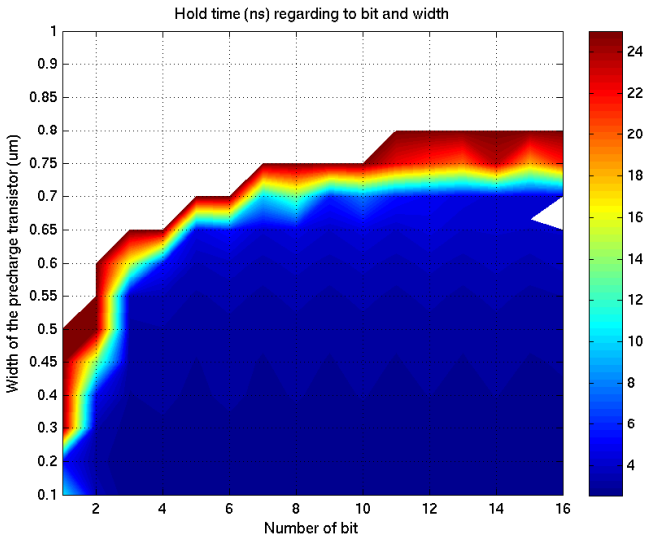

Figure 13. The ULV5 without the keeper is simulated to plot the relation between number of bits in a chain and the width of the precharge transistor. The hold time (the time-slot over which the output is kept valid) is given in ns.

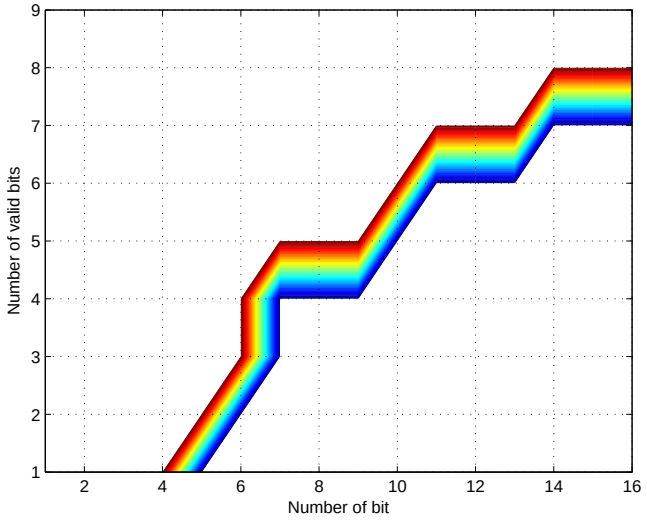

Figure 14. The simulation plot shows the development of the valid bit through the chain for different widths of the precharge transistor.

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