Robustness Study of SiC MOSFET Under Harsh Electrical and Thermal Constraints

To an in-depth physical failure analysis

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***Abstract*— The improvement of power conversion systems makes SiC devices very attractive for efficiency, compacity and robustness. However, their behavior in response to short circuit mode must be carefully studied to ensure the reliability of systems. This study deals with a SiC MOSFET. After the description of the component structure and its electrical performances, the paper presents some preliminary results for robustness evaluation in harsh electrical and thermal conditions. Extensive studies are underway to try to correlate the electrical measurements with an in-depth structural analysis.**

Keywords-SiC MOSFET; Robustness; Failure analysis; Short-Circuit.

I. INTRODUCTION

The SiC powers Metal Oxide Semiconductor Transistors (MOSFET) are very attractive for high temperature application in automotive or aeronautics. The isolated gate and the low drain to source resistance in on-state (R_{DSon}) make them ideal for using the MOSFET as a switch for all power electronics applications where efficiency, compacity and robustness are needed.

First, SiC MOSFET had been realized since 1986 [1] even if oxide on SiC were studied before. Many challenges in design have been made in order to expect higher frequencies switching than with Silicon Insulated Gate Bipolar Transistor (IGBT) and with higher operating temperature [7]. Investigations of different types of structures with 4H-SiC or 6H-SiC polytypes have been proposed with different challenges [8] and the vertical power devices double implanted MOSFET (DIMOS) shows very good performances due to its higher bulk mobility [9].

In order to evaluate the robustness of this type of MOSFET, several tests are possible. High temperature gate-bias (HTGB) and high temperature reverse-bias (HTRB) tests are common qualification tests for discrete semiconductor devices [10] however the short-circuit test [4][6][11] is one of the most used to evaluate the ruggedness of power devices during conduction. By using this test on a commercial 1.2 kV SiC Power MOSFET, the thermal instability and the electro-thermal behaviour are investigated in [11] by the mean of a state-of-art IR thermographic set-up. Othman et al. [4][6] present a comparison study on performances, reliability and robustness between SiC MOSFET and JFET devices. The aim of the studies is to evaluate the abilities and effects of each technology on the conception of power converter for avionic applications and to analyse their capability to withstand with harsh electrical constrains. The purpose of this paper is to present preliminary experimental results that could help to understand impact of the physical failure on the performance of the SiC MOSFET. First, the DIMOS is characterised in short circuit test. Then, two failure mechanisms are put in light with microstructural analysis.

II. COMPONENT UNDER TEST

The device under test (DUT) is a 1.2 kV SiC-MOSFET with continuous drain current I_{Dmax} equal to 24 A at 25 °C. The DUT is a vertical DIMOS transistor and its structure for an elementary cell is presented in Figure 1.

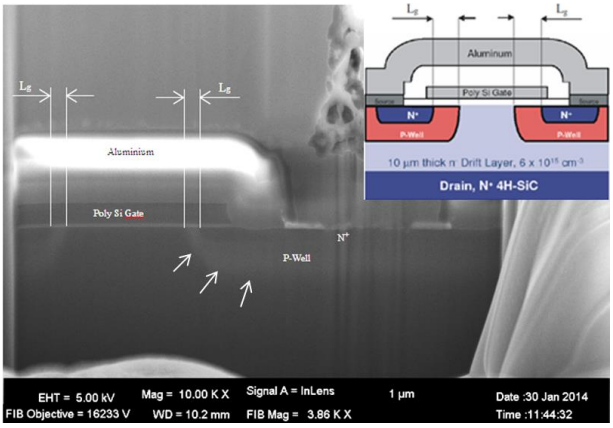

Figure 1. Structure investigation of DUT.

The Poly-Silicon Gate is isolated from the lateral channel with a thin oxide layer and the channel length is Lg. The Drain terminal is connected to the bottom of the device and is coupled to the channel through a drift layer that contributes to the on-state resistance and allows to apply large voltages between Drain and Source during off-state.

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The other two terminals are fixed on the top of the device and the Source electrode, which is made of Aluminum, entirely covers the top face except on the Gate bonding wire pad.

Finally, the die is brazed on a Copper base plate that carries out the heat preventing from over self-heating during electrical conduction. The brazing, an alloy of Tin, Silver and Antinomy, is limited to a maximum operating temperature of 260°C.

As our main goal is to correlate the physical failure analysis of the DUT and the analysis of its cross section structure with the help of Scanning Electron Microscopy (SEM) after Focused Ion Beam (FIB) sample etching, the first step is to make sure that the depackaging process has no impact on the DUT electrical behavior. In order to verify this point, we have compared current-voltage (IV) characteristics before and after opening.

III. IVT CHARACTERIZATION

The static behavior of the transistor is studied over the recommended range of operating temperature according to the constructor datasheet (from -55 °C to +135 °C). Our study is restricted to the evolution of the drain current I_D depending on temperature variation, reflecting the behavior of the transistor.

To perform the current-voltage-temperature (IVT) measurements while providing thermal stabilization of the DUT, three experimental means have been implemented. For the negative temperatures, a cold forced air system is used; for positive and high temperatures, a Peltier module and a plate heating resistor are required. A thermocouple sensor, positioned as close to the base plate of the DUT as possible, controls its temperature. This setup provides a good accuracy and a satisfactory stability during measurements.

Pulsed mode is suitable to avoid any self-heating of the DUT during the static measurements. To satisfy this requirement, the pulse drain temporally includes the gate pulse. The pulse drain duration is fixed to 3 microseconds, with a duty cycle equal to 0.15%.

The output curves I_D (V_{DS}, T) in Figure 2 are plotted for a low gate voltage V_{GS} equal to 10V over a temperature range extending from -50 °C to 135 °C showing a steady increase in the drain current with the temperature increase.

The input curves I_D (V_{GS}, T) in Figure 3 are plotted for the same values of temperature, and for an output voltage V_{DS} equal to 18 V. The measurements suggest, as expected, a significant reduction in the threshold voltage V_{th} as a function of temperature.

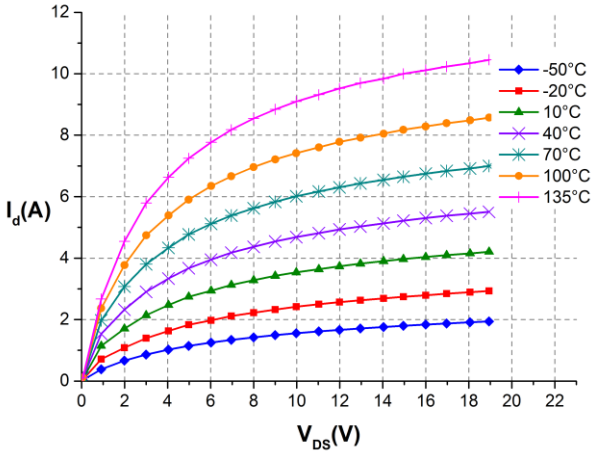

Figure 2. Output characteric I_D (V_{DS},T) for different temperatures with V_{GS} = 10V.

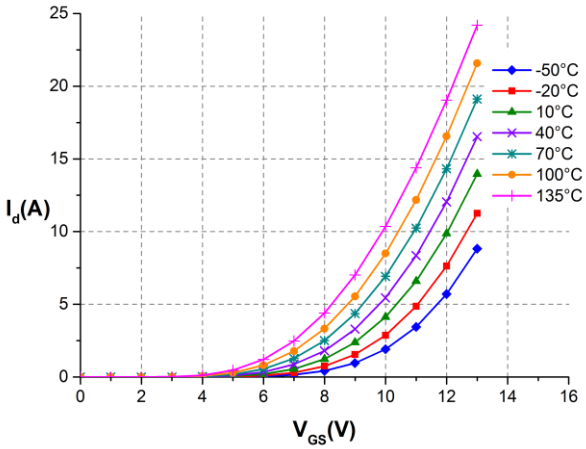

Figure 3. Input characteric I_D (V_{GS},T) for different temperatures with V_{DS} = 18V.

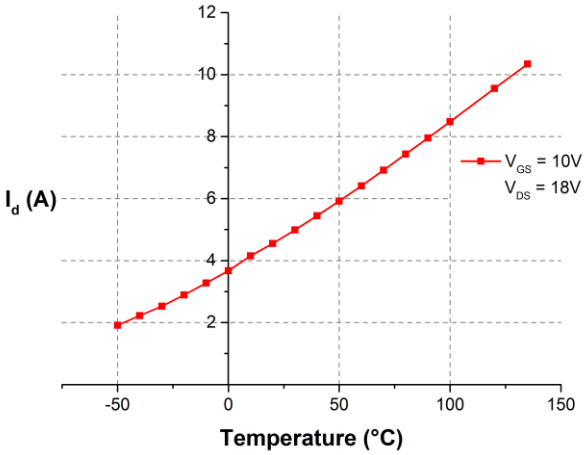

Figure 4. Drain current I_{Dsat} variation versus the temperature for V_{GS}=10V and V_{DS} =19V.

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The variation of the drain current is given in Figure 4 in the area of near saturation of the output characteristic, for a gate voltage VGS equal to 10 V and for a drain voltage VDS equal to 19 V.

IV. ROBUSTNESS

Once the fresh electrical characterization of the devices achieved, a stress campaign is carried out under short circuit tests at room temperature, T = 25 °C. We apply a drain voltage of 600V without any output load. During the short circuit phase, the DUT is maintained in the on-state by applying a gate voltage of 20V and is then switched off by reverse biasing the gate [6]. Dedicated test bench schematic circuit is shown in Figure 5.

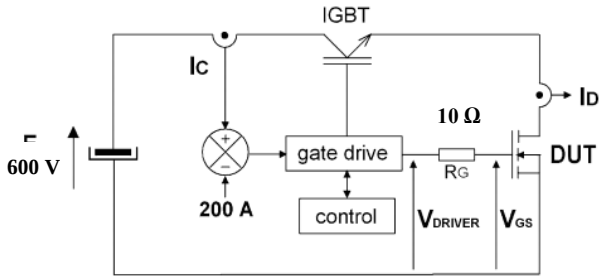

Figure 5. Test circuit for short circuit robustness analysis [6].

The first step consists in evaluating the energy responsible for the failure over long pulse duration. We applied the short circuit stress to a first component DUT1 for long pulse duration until complete failure. Figure 6 reports waveforms (V_{Driver}, V_{GS} and I_D) measured during the short circuit test. The corresponding dissipated energy before failure is about 0.96 J. Results indicate that the device was capable to sustain short circuit tests for a gate drive duration t_{SC} equal to 16 µs.

From these observations, we apply the same constraints to a second component DUT2 by applying successive short circuit tests with pulse duration t_{SC} increased by 2 µs at each test. In these conditions of experimentation, we try to determine the critical energy that is the maximum value of energy controllable by the DUT.

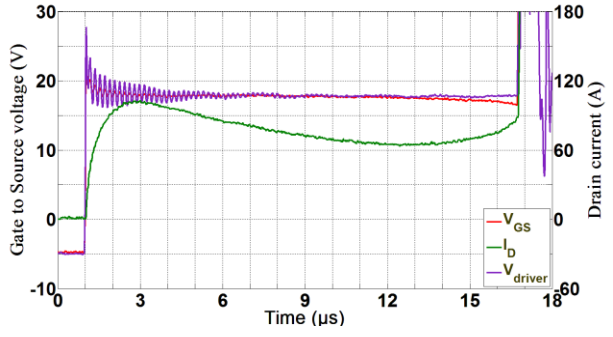

Figure 6. DUT1 : Robustness analysis under long pulse short circuit.

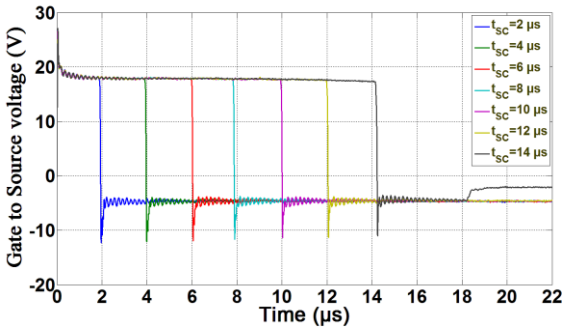

Figure 7. DUT2 : Evolution of gate to source voltage during short circuit tests showing a gate leakage current.

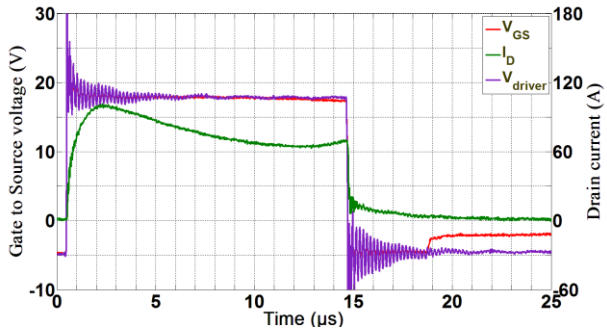

Figure 8. Failure of DUT2 during short circuit test, V_{DS} = 600V, t_{SC}=14µs, T=25 °C.

As illustrated, Figure 7 shows gate voltage waveforms measured during short circuit operations. The last short circuit stress of t_{SC} = 14µs applied to DUT2 causes the device failure. Figure 8 reports waveforms (V_{Driver}, V_{GS} and I_D) measured during the last short circuit test

V. DISCUSSION

A. Static I-V characteristics of the DUT

The drain current expression in linear operating region is given by (1), which describes the evolution of I_D (V_{GS}, V_{DS}) characteristic. For drain-source voltage (V_{DS}) values lower than V_{GS}-V_{th}, the drain current characteristic is linear, the behavior of the component is then like of a linear voltage-controlled inductance.

$$I_D = \frac{\mu_n W C_{ox}}{L} \cdot \left[(V_{GS} - V_{th}) V_{DS} - \frac{{V_{DS}}^2}{2} \right] \qquad (1)$$

Where W and L are respectively the gate width and the gate length, μ_n is the charge-carrier effective mobility and C_{ox} is the gate oxide capacitance per unit area.

The drain voltage corresponding to saturation mode is defined by the difference between the applied gate voltage and the threshold voltage that is, $V_{Dsat} = V_{GS}$-V_{th}. The V_{Dsat} value read from the output curve of Figure 2, for a temperature of 40 ° C, is equivalent to 10 - 2.9 (V), that to say 7.1V. Beyond this value, for increasing V_{DS}, the

component works in saturation mode and the current value maintains substantially the I_{Dsat} value. Then, the current value is independent from V_{DS} and its expression is given by (2). By experimental measurement, we found a decrease in Vth with temperature over a range from -50 °C to 135 °C. For a given value of V_{GS}, equation (2) predicts an increase of the saturation current I_{Dsat}, which is experimentally verified.

$$I_{Dsat} = \frac{\mu_n W C_{ox}}{L} . \left[\frac{(V_{GS} - V_{th})^2}{2} \right] \quad (2)$$

More rigorously, we should also take into account the evolution of the mobility μ_n which decreases with temperature [5]. V_{th} is also decreasing with temperature; the two variations (μ_n and V_{th}) have an opposite effect on I_{Dsat}. Threshold voltage variation is predominant at low gate voltage [2][3], which corresponds to our IVT characterizations as shown in Figures 2 and 3. The opposite behavior occurs for high gate voltage values, i.e., V_{GS} equal to 20V corresponding to robustness tests conditions presented in section IV.

B. Robustness

It is clearly seen during these robustness tests that the two devices had different failure mechanisms.

As shown in Figure 6, DUT1 fails after thermal runaway by the rapid increase in the drain current due to failure in short-circuit between drain and source. Similar failures were observed for SiC JFET devices for which increase of the temperature beyond the fusion limit of the device metallization was proposed in order to explain failures [4].

However, the transistor DUT2 first turns-off safely and short-circuits current falls down to zero as seen in Figure 8. But, few microseconds after the switch-off, a sudden short-circuit is observed between gate and source. So, gate failure occurred during transistor's off state after short-circuit but no failure occurred between drain and source electrodes. According to some authors, the gate oxide could be destroyed and the device became uncontrollable [6]. The time between the end of short-circuit and the gate failure may be due to temperature diffusion inside the device, which delay heating on the gate oxide

In Figures 6 and 8, we can clearly notice that a significant leakage current appears about 12 µs after the beginning of the short circuit, which seems to be responsible for the devices failures even if the failures seem to be different regarding the gate to source voltage evolution at failure. The decrease of the gate to source voltage during short circuit seems to show degradation between gate and source electrodes during this particular test [4].

C. Structural analysis of degradations

The stressed component DUT1 presenting GDS short-circuit degradation was unpacked and an example of a FIB cut (Focused Ion Beam) is given in Figure 9.

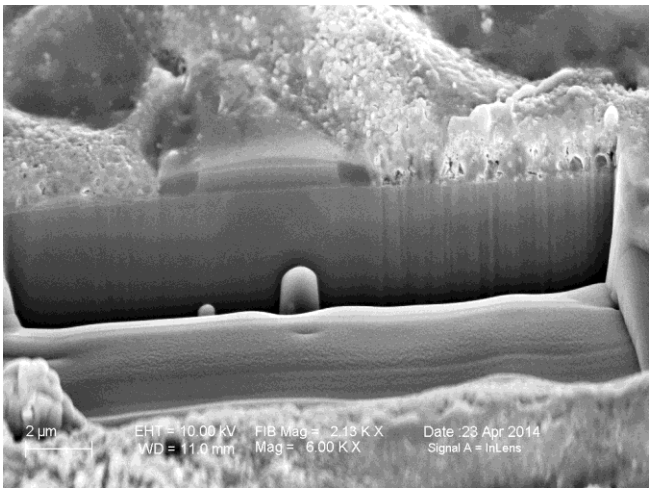

Figure 9. Material degradation analysis of DUT1.

Analyzing the figure, we could make the following observations:

- We are able to identify the different elements of the structure of the MOSFET,
- The aluminum layer corresponding to the source contact largely melted.

However the reduction of the oxide over the gate polysilicon may be due to the unpacking process; further tests will be performed.

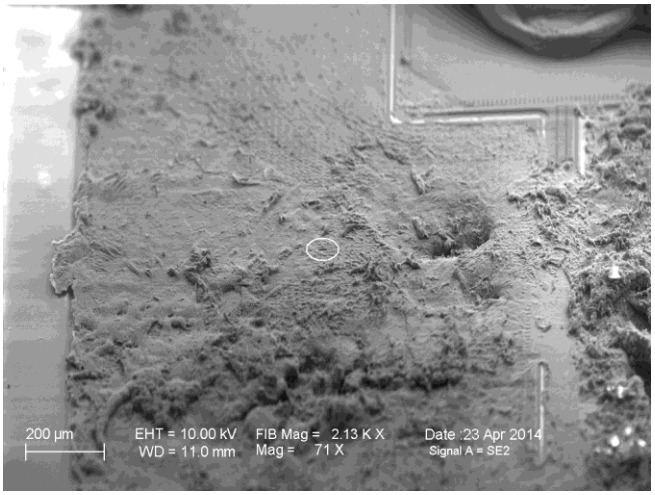

Figure 10. FIB cut location and surface degradation of DUT1.

Regarding the gate oxide, between channel and polysilicon gate, it does not appear to have been damaged by the stress but the FIB cut was performed in a randomly selected location and not where the surface degradations appeared to be the strongest Figure 10.

VI. CONCLUSION

A complete thermal IVT characterization has been performed and shows a behavior consistent with the manufacturer's data. Short circuit tests, conducted under extreme conditions, showed a destruction of the two devices

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under test. However, different failure modes were observed. To better understand the failure mechanisms, current studies are carried out under softer short circuit test in order to highlight significant variations in electrical measurements. Defects generated in the device structure will be located and analyzed by SEM and FIB in the aim to correlate these observations with the electrical measurements.

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