Scan-shift Power Reduction Based on Scan Partitioning and $\bar{Q}$-D Connection

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***Abstract*—Excessive test power consumption is a great concern in modern VLSI testing. This paper presents an efficient scan-shift power reduction scheme based on scan chain partitioning and $\bar{Q}$-D connection. After partitioning the scan chains into several segments equally, selective $\bar{Q}$-D connection is introduced to reconfigure each segment, which only exploits the $\bar{Q}$ output port of the scan flip-flop and no additional hardware or routing overhead will be introduced. Experimental results show that the proposal can achieve 3.43% scan-shift power reduction on average with the help of selective $\bar{Q}$-D reconnection after scan partitioning. Furthermore, the proposed scan-shift power reduction technique can be acceptable for Built-In Self-Test (BIST) and non-BIST scan-based testing architecture without affecting test application time, test fault coverage, performance and routing overhead of the circuit under test.**

Keywords*—scan partition; $\bar{Q}$-D connection; low power test; scan-shift power.

I. INTRODUCTION

With the complexity and performance of very large scale integrated (VLSI) circuits growing, the power consumption density of advanced VLSI is rapidly increasing since the supply voltage cannot be reduced so much due to its noise margin [1]. Furthermore, power consumption in at-speed scan testing is significantly higher than that during normal functional operation, while modern VLSI testing aims to perform at-speed or even faster than at-speed testing to test the chip for high-quality screening [2][3]. Therefore, the increasing power consumption during testing has been a serious concern, which can result in voltage drop, yield loss, reliability problems and even heat damage of the Circuit Under Test (CUT) [4]–[6].

To address these problems, many testing power reduction methodologies have been proposed, such as X-filling approaches which explore the reassignment of don't care bits in test cubes to reduce switch activities [7]–[9], low power Test Pattern Generation (TPG) techniques that modify the architecture of TPG like Linear Feedback Shift Register (LFSR) to reduce the transitions of inputs of the CUT [10]–[12], test vector reordering methods through changing the order of the test vectors to reduce the number of transitions between two consecutive vectors [13][14], and power-aware Automatic Test Pattern Generation (ATPG) techniques [15][16], and so on.

For scan-based testing, scan-shift power is defined as the dynamic power consumption dissipated by serial shift operations during scan-in of test stimuli and scan-out of responses, while capture power is defined as the power consumption occurred in responses capturing mode [12][17]. Scan-shift power can be effectively reduced by scan cells reordering, which is one of the most attractive techniques to reduce scan-in and scan-out transitions by rearranging every scan cell with proper position [18][19]. However, this approach usually costs excessive high routing hardware and computation time according to the increasing number of scan cells. Selective reconfigurable inverters are inserted between scan cells to decrease the switching activities in the scan chains during shift operation in [20], which is claimed to be suitable for any scan architecture. Unfortunately, this technique not only requires large area and control cost, but also influences the performance of the CUT. Scan architecture modification techniques through modifying the scan architecture to reduce scan test power by inserting gates or partitioning scan chains into several segments [21]–[26]. Low power jump scan architecture is utilized by Chiu and Li [21] to reduce test power with penalty of speed performance degradation, while low power Illinois scan architecture is proposed by Chandra et al. [22] to reduce scan-in shift power but not suitable for decreasing the test power dissipated during scan-out shift operation.

Scan partitioning/segmentation is another scan architecture modification technique, which divides a given scan chain into several segments to cut down the shift process for full scan chain into a sequence of segment-wise shifts [23][24]. Scan partitioning scheme with scan freeze flip-flops and status registers is introduced by Kim et al. [23] to reduce the scan-shift power consumption. The test application time of the previous scheme will be raised since it requires additional test clock cycles to scan-in the configuration data stored in status registers. In [24], the given scan chain is partitioned into s segments, and only one segment is active during the scan shift operations, while all other segments are clock gated in hold mode to retain the scan test data. This approach is very efficient to reduce scan-shift power and can be applicable to Built-In Self-Test (BIST) and non-BIST schemes without affecting test application time, fault coverage, performance of the CUT and/or the scan cell routing cost.

In this paper, we propose a scan-shift power reduction scheme based on scan partition and $\bar{Q}$-D connection. After evenly partitioned each scan chain into several segments as in [24], $\bar{Q}$-D connection is introduced to reconnect two consecutive scan cell for every segments, which will reduce the scan-shift power further. The proposed scheme requires no additional hardware with respect to [24] and keeps all advantages of [24], which is suitable for BIST and non-BIST test environments without penalty of test quality, performance degradation or additional hardware of the CUT.

The rest of this paper is organized as follows. Section II describes the scan-shift power metric and related works. Section III presents the proposed scan-shift power reduction scheme. The experimental results and comparison are shown in Section IV. Finally, Section V concludes this paper.

II. RELATED WORK

A. Scan-shift Power Metric

As mentioned above, scan-shift power is the dynamic power consumption dissipated during shift operations, which generally depends on the switching activity or transitions

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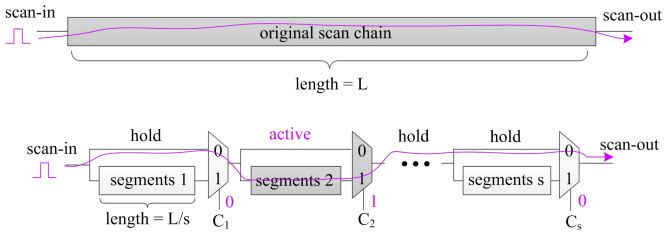

Figure 1. Shift operations of original scan chain and partitioned scan segments

occurred in the scan chain. Therefore, we utilize the widely used Weighted Transition Metric (WTM) [27][28] for the scan-shift power evaluation in this work. *Scan-in power* is the dynamic power consumption dissipated during scan-in of test stimuli, which can be calculated as (1), according to WTM [27][28].

$$WTM_{in} = \sum_{i=1}^{N} \left[\sum_{j=1}^{L-1} (t_{i,j} \oplus t_{i,j+1}) \times j \right] \quad (1)$$

where N is the number of test vectors, L is the length of scan chain and $t_{i,j}$ is the j^{th} bit of test vector t_i.

According to WTM [27][28], *scan-out power* can be calculated as (2), which is the dynamic power consumption dissipated during scan-in/out of test responses.

$$WTM_{out} = \sum_{i=1}^{N} \left[\sum_{j=1}^{L-1} (r_{i,j} \oplus r_{i,j+1}) \times (L-j) \right] \quad (2)$$

where N is the number of test vectors, L is the length of scan chain and $r_{i,j}$ is the j^{th} bit of test response r_i.

Therefore, the total number of weighted transitions of *scan-shift power* can be calculated as (3) according to WTM [27][28], since it is the sum of *scan-in power*, *scan-out power* and the total number of transitions between the MSB of the previous test response and the LSB of current test vector, which will propagate from the first scan cell to the last in the scan chains during scan-out operations.

$$WTM = WTM_{in} + WTM_{out} + \sum_{i=1}^{N-1} (t_{i+1,L} \oplus r_{i,1}) \times L \quad (3)$$

where $t_{i+1,L}$ is the LSB of test vector t_{i+1}, $r_{i,1}$ is the MSB of test response r_i, and r_i is the corresponding response of test vector t_i.

B. Scan Partition and Scan Hold

In [24], a low power scheme based on scan partition and hold is proposed, which is shown in Figure 1. After equally partitioning the scan chain into s segments, a multiplexer is utilized to connect two consecutive segments and each multiplexer is controlled by signal C_j ($1 \leq j \leq s$). During scan shift operations, only single signal of C_j is set to high, and the corresponding segment j is working in scan-in/out operations, while others are hold in bypass state. Note that, working in hold mode means that the scan cells of this segment will retain their scan test data unless the corresponding control signal C_k jumps to high. Therefore, the scan test data of every segment only require to scan-in/out through itself after scan chain partition and hold, while it need to shift through the full scan chain until it arrive at the appropriate position before scan partitioning. For example, if a transition exists between the last two scan cells of the scan chain ($Length = L$) for a test vector, this transition will propagate from the first scan cell to the $L-1$ scan cell before utilizing the low power scheme in [24], where it will cause $L-1$ scan cell transitions during scan-in operations. After partitioning the scan chain as shown in Figure 1, this transition will only propagate through the last segment, where only $L/s-1$ scan cell transitions will occur. Hence, the scheme in [24] can reduce the scan-shift power significantly without affecting test application time, fault coverage, performance and/or the scan cell routing cost of the CUT. Furthermore, this low power scheme can be easily extended to multiple scan chains test architecture.

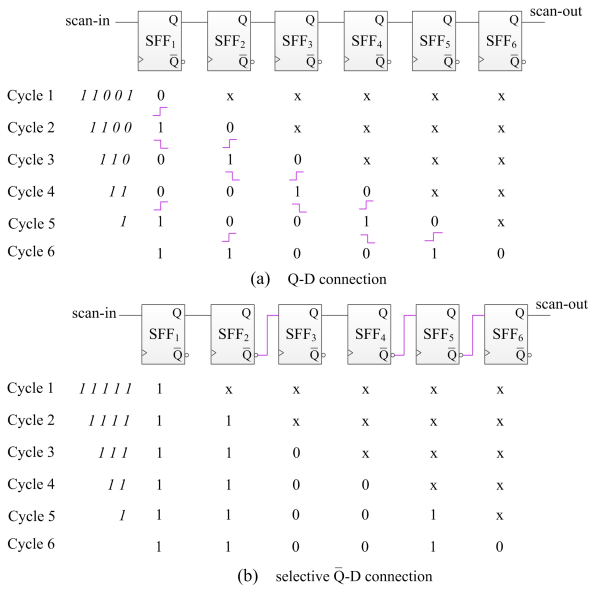

Figure 2. Example of selective Q̄-D connection [25]

C. Q̄-D Connection

Without introducing additional hardware and routing cost, selectively replacing the Q-D connection with Q̄-D connection between two consecutive scan cells in the scan chain can also reduce the switching activity during scan shift operations effectively [25][26]. For example, assume the scan chain include 6 scan cells and test vector t=110010 be applied to the chain. If only the Q-D connection is utilized to chain all scan cells, 11 transitions will occur in order to apply the test vector t, as shown in Figure 2(a). However, if we selectively configure the sub-chain of scan cells SFF2-SFF3, SFF4-SFF5 and SFF5-SFF6 with Q̄-D connection, the reconfigured pattern t'=111111 will be shifted into the scan chain instead to actually apply the original test vector t to the CUT, where no transition will occur during scan-in shift operations, as shown in Figure 2(b). It is obvious that, the scan-shift power can be reduced similarly without requiring any additional logic or routing cost, and it can be simply extended to multiple scan chains with multiple test patterns.

III. Proposed Scheme

In order to further reduce the scan-shift power, we apply the Q̄-D connection technique as in [25][26] into the segments

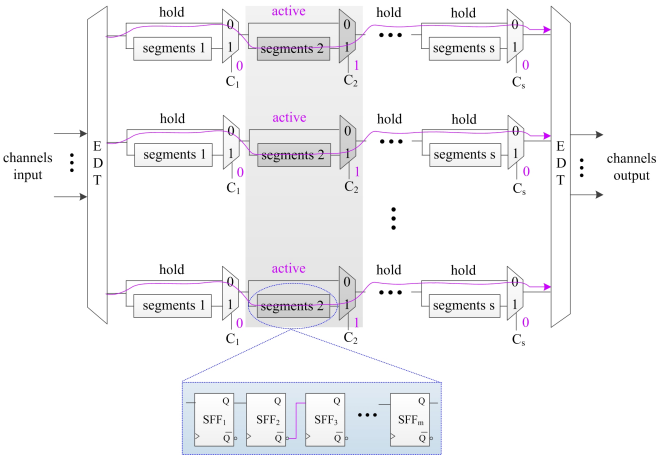

Figure 3. Proposed low power scan architecture

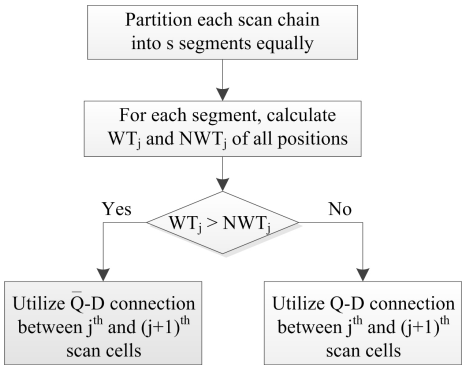

Figure 4. Selective Q̄-D reconnection flow

after partitioning the scan chains as in [24]. The proposed low power scan test architecture is shown in Figure 3. Firstly, every original scan chain is equally partitioned into s segments, where each segment has L/s scan cells and L is the length of scan chain. The scan-in and scan-out ports of each segment are connected to a multiplexer, and a signal C_i is utilized to control it. If and only if single C_i is set to high, each i^{th} segment for every scan chain is active for scan-in stimuli and scan-out responses, and others are hold to retain their scan test data and bypass the scan data of the corresponding active segment during scan shift operations as in [24]. Unlike in [24], where all scan cells are chained in Q-D connection, we selectively introduce Q̄-D connection as shown in the broken blue block in Figure 3 to reconfigure each segment after scan partitioning to further reduce the scan-shift power. It is obvious that, no additional hardware or routing overhead will be introduced to apply the selective Q̄-D connection technique after scan partitioning as shown in Figure 3.

Then, we will describe the procedure how to select Q-D or Q̄-D connection to chain each two consecutive scan cells for all segments in detail. The proposed selective Q̄-D connection flow is shown in Figure 4. First of all, we will show the calculation of WT_j/NWT_j , which denotes the the total number of weighted transitions/nontransitions between the j^{th} and $(j+1)^{th}$ scan cells in a given segment after scan partitioning for scan-in/out all test stimuli and responses. Assume each segment has $L_s = L/s$ scan cells, according to the scan-shift power metric WTM [27][28] described above, WT_j and NWT_j $(1 \leq j \leq L_s - 1)$ can be calculated as (4) and (5), respectively.

$$WT_j = j \cdot \sum_{i=1}^{L_s}(t_{i,j} \oplus t_{i,j+1}) + (L_s - j) \cdot \sum_{i=1}^{L_s}(r_{i,j} \oplus r_{i,j+1}) \quad (4)$$

$$NWT_j = j \cdot \sum_{i=1}^{L_s}(t_{i,j} \odot t_{i,j+1}) + (L_s - j) \cdot \sum_{i=1}^{L_s}(r_{i,j} \odot r_{i,j+1}) \quad (5)$$

where $\sum_{i=1}^{L_s}(t_{i,j} \oplus t_{i,j+1})$ / $\sum_{i=1}^{L_s}(t_{i,j} \odot t_{i,j+1})$ denotes the total number of transitions/nontransitions between the j^{th} and $(j+1)^{th}$ scan cells after scan-in all test vectors, while $\sum_{i=1}^{L_s}(r_{i,j} \oplus r_{i,j+1})$ / $\sum_{i=1}^{L_s}(r_{i,j} \odot r_{i,j+1})$ denotes the total number of transitions/nontransitions after scan-out all test responses.

As shown in Figure 4, after calculating all WT_j and NWT_j of each segment for all positions between every two consecutive scan cells, we can selective Q̄-D connection to connect the j^{th} and $(j+1)^{th}$ scan cells if WT_j is greater than NWT_j like in [27], then the reconfigured WT_j will be lower than NWT_j and the scan-shift power will decrease. Otherwise, the Q-D connection will be utilized to chain these two scan cells. It should be noted that the corresponding actual test vectors and expected responses would be changed exactly according to the selective Q̄-D connection modification in segments.

TABLE I. TEST INFORMATION OF THE EXPERIMENTAL BENCHMARK CIRCUITS

Circuits	Inputs	Outputs	FFs	Gates	Faults	Tests	FC%
s5378	35	49	179	2779	4603	257	99.13
s9234	36	39	211	5597	6927	371	93.48
s13207	62	152	638	7977	9815	467	98.46
s15850	77	150	534	9775	11725	430	96.68
s35932	35	320	1728	16353	39094	65	89.81
s38417	28	106	1636	22257	31180	885	99.47
s38584	38	304	1426	19405	36303	672	95.85
b14	32	54	245	9821	22802	934	99.22
b15	36	70	449	8437	21988	627	96.29

IV. EXPERIMENTAL RESULTS

To validate the efficiency of the proposed scan-shift test power reduction scheme, experiments on several comprehensive large full scanned ISCAS'89 [29] and ITC'99 [30] benchmark circuits have been performed. The proposed test power reduction algorithm for simulation was implemented in MATLAB language, and the test patterns and corresponding expected responses utilized for experiments were generated by ATALANTA [31] (ATPG program developed at the Virginia Polytechnic Institute and State University) with X-bits random filling.

The test information of the experimental benchmark circuits is shown in Table I. The first column lists the names of the experimental benchmark circuits. Columns *Inputs*, *Outputs*, *FFs* and *Gates* show the numbers of inputs, outputs, scan flip-flops and gates of each circuit, respectively. Columns *Faults*, *Tests* and *FC%* present the number of collapsed stuck-at faults,

TABLE II. EXPERIMENTAL RESULTS OF THE SCAN-SHIFT POWER REDUCTION

Circuits	Chains	Segments=1			Segments=4				Segments=10			
		WTM_org	Proposed	Red%	WTM[24]	Proposed	Red1%	Red%	WTM[24]	Proposed	Red1%	Red%
s5378	2	1943787	1830353	5.84	475445	446129	77.05	6.17	189055	179094	90.79	5.27
	4	957020	894791	6.50	236783	222825	76.72	5.89	97569	92744	90.31	4.95
	8	472727	444311	6.01	119366	113788	75.93	4.67	51077	49093	89.61	3.88
s9234	2	4156921	3920896	5.68	1030628	976505	76.51	5.25	415022	394734	90.50	4.89
	4	2078919	1963258	5.56	517131	490474	76.41	5.15	208462	198392	90.46	4.83
	8	1031100	977132	5.23	258703	246105	76.13	4.87	106534	103102	90.00	3.22
s13207	2	47429139	45694727	3.66	11830483	11416182	75.93	3.50	4744012	4565319	90.37	3.77
	4	23687048	22857670	3.50	5919628	5701246	75.93	3.69	2371718	2289642	90.33	3.46
	8	11828258	11417421	3.47	2955846	2857563	75.84	3.33	1184348	1147993	90.29	3.07
s15850	2	29954492	28916310	3.47	7508937	7231576	75.86	3.69	2999171	2912128	90.28	2.90
	4	14993840	14474703	3.46	3764599	3638574	75.73	3.35	1504874	1460581	90.26	2.94
	8	7508809	7233919	3.66	1883954	1818053	75.79	3.50	757582	733894	90.23	3.13
s35932	2	44583480	43197336	3.11	11136528	10800522	75.77	3.02	4466048	4319577	90.31	3.28
	4	22283208	21598096	3.07	5575176	5396458	75.78	3.21	2235874	2170487	90.26	2.92
	8	11136528	10800522	3.02	2785266	2698430	75.77	3.12	1118348	1083776	90.27	3.09
s38417	2	560130270	545065774	2.69	140001136	136904852	75.56	2.21	55957232	54708300	90.23	2.23
	4	279915781	272803452	2.54	69730362	67882401	75.75	2.65	28009380	27315453	90.24	2.48
	8	139987369	136913057	2.20	34888702	34072528	75.66	2.34	14015059	13706833	90.21	2.20
s38584	2	341905860	328755899	3.85	85430686	82361649	75.91	3.59	34207213	32932619	90.37	3.73
	4	171103848	164558597	3.83	42764732	41220279	75.91	3.61	17112858	16484005	90.37	3.67
	8	85433488	82374315	3.58	21379404	20627752	75.86	3.52	8554334	8255648	90.34	3.49
b14	2	12764758	12490791	2.15	3213032	3152867	75.30	1.87	1303873	1274219	90.02	2.27
	4	6503977	6359161	2.23	1621931	1583124	75.66	2.39	654453	640416	90.15	2.14
	8	3211276	3153979	1.78	813013	798713	75.13	1.76	331315	326930	89.82	1.32
b15	2	30278294	29451219	2.73	7615643	7426652	75.47	2.48	3051162	2975560	90.17	2.48
	4	15221233	14811558	2.69	3806116	3708708	75.63	2.56	1530697	1491193	90.20	2.58
	8	7615643	7426652	2.48	1902929	1862893	75.54	2.10	772079	753689	90.10	2.38
Avg.				3.63			75.87	3.46			90.24	3.21

test patterns and the fault coverage obtained from ATALANTA ATPG tool for each benchmark circuit.

Table II illustrates the experimental results. Column *Chains* lists the number of scan chains of each circuit used for simulation, which ranges from 2 to 8. Columns 3-5, 6-9 and 10-13 present the experimental results of each circuit after each scan chain partitioned into 1, 4 and 10 segments, respectively. The total original WTM calculated by (3) for each original scan circuit under different number of scan chains is shown in column *WTM_org*, and the WTM after scan chain partitioned as in [24] is shown in column *WTM*[24], while the WTM of the proposed scheme is listed in column *Proposed*. To clearly illustrate the efficiency of the proposal, the scan-shift power reduction percentage of the proposal with respect to the original scan circuit and scan partition in [24] are presented in columns *Red1%* and *Red%*, respectively. The last row of TABLE II gives the average percentage of scan-shift power reduction under different scan partition.

As shown in Table II, compared with the original scan CUT, the proposed scheme can obtain scan-shift power reduction about 75.87% and 90.24% on average under partitioned segments number in 4 and 10 respectively, which is a little more than $\frac{s-1}{s} \times 100\%$ (s is the number of partitioned segments). While compared with the scan partition in [24], with the help of the selective $\bar{Q}$-D connection technique, the proposed scheme can achieve 3.61%, 3.46% and 3.21% scan-shift power reduction on average for different circuit with different scan chains under scan partitioned segments number in 1, 4 and 10, respectively. The average scan-shift power reduction under different partitioning is about 3.43%. Furthermore, the proposal need no additional hardware or routing overhead over [24] to reduce the test power further. Therefore, the proposed scheme is a efficient scan-shift power reduction technique. It should be noted that, a careful trade-off between hardware overhead and scan-shift test power reduction should be made before determining the number of partitioned segments for each scan chain, since more segments means more hardware overhead and higher power reduction together.

V. CONCLUSION

Scan partitioning is an attractive technique to reduce the scan-shift test power. In this paper, the selective $\bar{Q}$-D connection technique was introduced after scan partition to further reduce the scan-shift power. Since $\bar{Q}$-D connection only exploit the $\bar{Q}$ output of the scan flip-flops instead Q to scan the test data to the next scan flip-flop, it won't require any additional test hardware or routing overhead. The experimental results indicate that the proposal can achieve more about 3.43% scan-shift power reduction on average after introducing selective $\bar{Q}$-D connection technique to scan chain partitioned segments. Furthermore, the proposed scheme keeps

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all advantages of [24], which is suitable for BIST and non-BIST test environments without penalty of test quality or performance degradation of the CUT.

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