Novel FGMOS based Voltage Differencing Buffered Amplifier and its Filter Applications

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***Abstract*—The work presents Floating Gate MOS (FGMOS) based low-voltage, low-power (LV/LP) variant of recently proposed Voltage Differencing Buffered Amplifier (VDBA). The proposed topology operates at low supply of ±1.35V with total power consumption of 0.745mW. The linearity of the Operational Transconductance Amplifier (OTA) stage of the proposed active element is observed to increase compared to the conventional VDBA and the same has been proved for several supply voltages. The application of the proposed circuit is verified through robust resistorless voltage mode universal biquad filters which are observed to implement standard filter functions. The simulations are performed through SPICE in 0.18µm technology to validate the workability of the proposed circuit. The work is intended to find applications in low-voltage, low-power battery-operated medical devices and other analog signal processing circuits.**

Keywords-FGMOS; Voltage Differencing Buffered Amplifier (VDBA); Operational Transconductance Amplifier (OTA); Universal Filter; Analog Signal Processing

I. INTRODUCTION

Analog signal processing (ASP) with the use of active elements employing Voltage Mode (VM) techniques is seen in existing research. VM techniques offer several advantages [1]. Among several VM active elements, VDBA has attractive properties of current mode technology such as reduced power consumption, larger bandwidth, wider linearity and higher slew rate compared to OP-AMP [2]. Furthermore, lower output impedance of VDBA compared to OTA eliminates loading effect which is suitable for VM circuit synthesis. These evidences demand ASP circuits with VDBA as a building block. Several modifications of VDBA have been suggested by Sotner et al. [3].

The demand for LV/LP electronics is inevitable in modern portable consumer electronics and battery-operated wearable and implantable biomedical devices. FGMOS techniques have dominated in this field of research with advantages of flexibility, controllability and tunability. Moreover, narrower bandwidth and relatively lower transconductance compared to the conventional MOS transistor are attractive features for biomedical devices since biological signals have extremely low amplitude and frequency. Applications of FGMOS in voltage buffer, analog inverter, winner-take-all (WTA), neural networks, electronic programming, squarers, current mirrors, multipliers, digital-to-analog and analog-to-digital converters have been reported [4]. Several research publications have dealt with CMOS implementations of VDBA [2][3][5]. Few VM active elements have been designed using the FG technique, such as Op Amp [6], OTA [7]-[10] and class AB output stage for CMOS Op-Amps [11]. As per authors' knowledge, suitable literature related to FGMOS based VDBA was not found.

This paper introduces a favorable structure of a new FGMOS VDBA suitable for VM ASP described in Section II. Implementation of second order active filters has been possible with the utilization of the active block. Two VM filters containing the proposed VDBA have been simulated and are given in Section III. The workability of the proposed circuits is confirmed by PSPICE simulations. These are discussed in Section IV. A comparison of the previously reported and the proposed VDBA is done. The use of proposed VDBA is confirmed with its applications to first and second form biquads and their capability in generating all filter functions. Section V concludes the results obtained.

II. PROPOSED FGMOS REALIZATION OF VDBA

Conception of the classical VDBA has been formulated in [2][5][12]. Using standard notation, port currents and voltages of CMOS VDBA can be described by (1):

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & \alpha & 0 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_W \end{bmatrix} \quad (1)$$

g_m is transconductance of VDBA, α is the corresponding voltage ratio ($\alpha = 1-\varepsilon_v$) and ε_v is voltage tracking error. The circuit symbol and schematic implementation of the proposed VDBA are shown in Figures 1 and 2 respectively. It has two fundamental blocks: OTA (M_1-M_9) and voltage buffer (M_{10}-M_{16}), both are realized by FGMOS variants of MOS differential pairs. FGMOS differential pair has been employed in OTA to ensure low voltage operation because of low FGMOS threshold voltage. In the differential pair

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formed by two floating gate (FG) transistors M1 and M2, one control input of each transistor is used for signal processing purpose, other control input is used for biasing, and hence an adjustable threshold voltage is achieved. The differential input voltage $V_{in} = V_{FG1} - V_{FG2}$, produces an output current that is voltage controlled current source (VCCS) [2]. V_{FG1} is the FG voltage at M1 given by $V_{FG1} = \frac{C_1}{C_T}V_N + \frac{C_2}{C_T}V_{bias}$ and the FG voltage at M2 is given by $V_{FG2} = \frac{C_1}{C_T}V_P + \frac{C_2}{C_T}V_{bias}$, where C_T is total capacitance, $C_T = C_1+C_2+C_{GS}+C_{GD}$. C_1 and C_2 are the FG capacitances. The current mirror load for the OTA is formed by M5 and M6. A voltage buffer is used in the output stage of the proposed circuit. It consists of a differential amplifier (M10 - M13) and a feedback transistor M14. The first control input of FGMOS M10 is V_Z terminal voltage. The input range of the OTA increases by the use of FGMOS transistors. The assumption is that identical MOSFETs and identical FGMOS transistors are used and all operate in saturation.

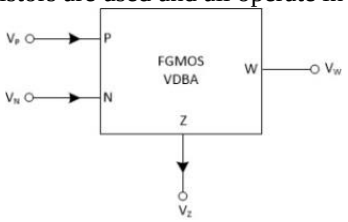

Figure 1. Circuit symbol: FGMOS VDBA

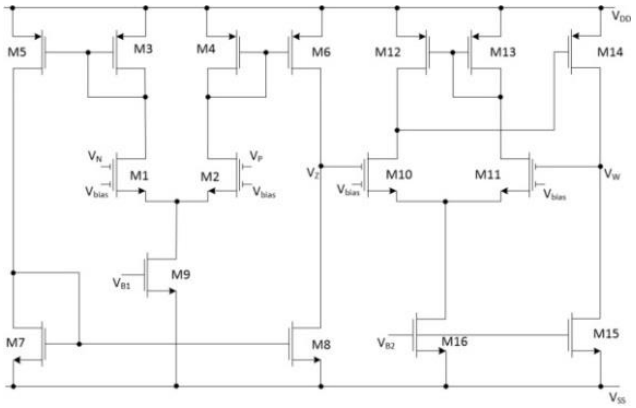

Figure 2. FGMOS implementation of the VDBA

Calculation of input range of the proposed OTA:

Condition for M2 to be in saturation is given by

$$V_{D2} \geq V_{FG2} - V_{T2} \quad (2)$$

and

$$V_{D2} = V_{G4} \quad (3)$$

$$V_{GS4} = V_{ov4} + V_{T4} \quad (4)$$

V_{ovi} and V_{Ti} are respectively the overdrive and threshold voltages of i^{th} transistor. (4) can be expressed as

$$V_{G4} - V_{S4} = V_{ov4} + V_{T4} \quad (5)$$

Substituting $V_{S4}=V_{DD}$ in (5) gives

$$V_{G4} = V_{ov4} + V_{T4} + V_{DD} \quad (6)$$

Using (2), (3) and (6) gives

$$V_{ov4} + V_{T4} + V_{DD} \geq V_{FG2} - V_{T2} \quad (7)$$

From Figure 2 the FG voltage of M2 is given as

$$V_{FG2} = \frac{C_1}{C_T}V_P + \frac{C_2}{C_T}V_{bias} \quad (8)$$

where C_1 and C_2 are the capacitances of FGMOS transistor and $C_T=C_1+C_2+C_{GS}+C_{GD}$, is the total capacitance.

Substituting V_{FG2} from (8) in (7) gives

$$V_{ov4} + V_{T4} + V_{DD} \geq \frac{C_1}{C_T}V_P + \frac{C_2}{C_T}V_{bias} - V_{T2} \quad (9)$$

$$V_P \leq \frac{C_T}{C_1}V_{ov4} + \frac{C_T}{C_1}V_{T4} + \frac{C_T}{C_1}V_{DD} - \frac{C_2}{C_1}V_{bias} + \frac{C_T}{C_1}V_{T2} \quad (10)$$

If $C_1=C_2$ and $C_T \approx C_1+C_2$, then (10) can be reduced to

$$V_P \leq 2V_{DD} + 2V_{ov4} + 2V_{T4} - V_{bias} + 2V_{T2} \quad (11)$$

The maximum input range of conventional VDBA is [2]

$$V_P \leq V_{DD} + V_{ov4} + V_{T4} + V_{T2} \quad (12)$$

On comparing (11) and (12), maximum input range is seen higher for proposed VDBA compared to the conventional. This has been proved through simulations in Section IV. Circuits proposed in the work are based on the simulation model of a 2 – input FGMOS transistor. It is assumed that the bulk transconductance of FGMOS is negligibly small.

III. FILTER APPLICATIONS

This section discusses filter applications of proposed VDBA. The filters consist of two cascaded FGMOS VDBA with two capacitors as passive components. Robust biquad filter configurations employing CMOS based VDBA have been proposed by Kacar et al. [2]. The proposed biquads (Figures 3 and 4) exhibiting filter functions are obtained on similar lines with the objective of low voltage operation. The nodal analysis of the proposed filters yield transfer functions given by (13) and (14). The relations for natural frequency and quality factor of FGMOS based Biquad 1 and Biquad 2 circuits are given by (15) and (16) respectively. For both biquads to realize standard filter functions, different values of V_1, V_2 and V_3 can be employed as given by Kacar et al. [2].

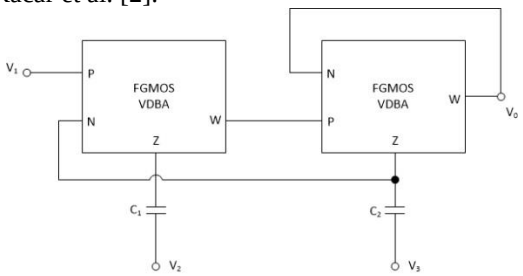

Figure 3. Proposed biquad 1 showing several filter functions

$$V_o = \frac{V_3\alpha_2 s^2 + V_2\frac{g_{mF2}\alpha_1\alpha_2}{C_2}s + V_1\frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}}{s^2 + s\frac{g_{mF2}C_1\alpha_2}{C_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1}{C_1C_2}} \quad (13)$$

$$V_o = \frac{V_3\alpha_2 s^2 - V_2\frac{g_{mF2}\alpha_2}{C_2}s + V_1\frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}}{s^2 + s\frac{1}{R_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}} \quad (14)$$

$$f_0(\text{Biquad 1}) = \frac{1}{2\pi}\sqrt{\frac{g_{mF1}g_{mF2}\alpha_1}{C_1C_2}} \quad (15a)$$

$$Q(\text{Biquad 1}) = \frac{1}{\alpha_2}\sqrt{\frac{g_{mF1}C_2\alpha_2}{g_{mF2}C_1}} \quad (15b)$$

$$f_0(\text{Biquad 2}) = \frac{1}{2\pi}\sqrt{\frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}} \quad (16a)$$

$$Q(\text{Biquad 2}) = R_1\sqrt{\frac{g_{mF1}g_{mF2}C_2\alpha_1\alpha_2}{C_1}} \quad (16b)$$

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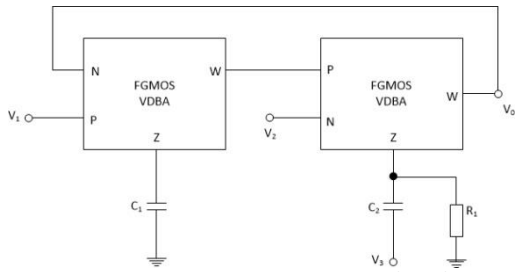

Figure 4. Proposed biquad 2 showing several filter functions

IV. SIMULATION RESULTS

All simulations are done with TSMC CMOS 0.18 µm technology, supply voltage ±1.35V, $C_{F1} = C_{F2} = 200$ fF. Model suggested by Rodriguez-Villegas [13] has been used to overcome DC convergence error because of FG. Aspect ratio values of transistors are given in Table I. Comparison of previous topologies with the proposed is done in Table II. An increase in the input range of OTA section of the proposed VDBA is seen. Reduced power consumption and transconductance is also observed. Increased bandwidth of the OTA stage is also seen. The gain of buffer stage of the proposed VDBA is ~1 and more reliable compared to previous topologies. DC transfer characteristic of the output stage of the proposed VDBA at bias voltages V_{B1} = 1V and V_{B2} = 0.45V is shown in Figure 5, where the linearity extends from -1V to +1.5V. The I_Z versus V_P and V_N is shown in Figure 6. The linearity extends in the range ±0.4V while a non-linear behavior is observed elsewhere. The operation of OTA stage of the proposed VDBA, depicting I_Z against V_P for different supply voltages is seen in Figure 7. Though the swing for which the OTA justifies its operation decreases by reducing the power supply; approximately ±350 µA at supply voltage of ±1.45V, ±300 µA at supply voltage of ±1.35V, ±250 µA at supply voltage of ±1.25V and ±200 µA at supply voltage of ±1.15V, the current swing provided for conventional VDBA reported in [2], is around ±140 µA, and that too for a supply voltage of ±1.5V which is high enough compared to the one simulated for the proposed VDBA. The linearity observed is in the range ±0.4V for the proposed VDBA performed at different supply voltages, while the linearity extends only upto a threshold of ±0.2V for the conventional VDBA [6]. This increase in the range of operation of the proposed VDBA can be accounted for the fact that the equivalent capacitance ratio, C_i/C_T (FG capacitance C_i) scales down the effective input signal at FG, resulting in a wider range. The frequency response depicting the transconductance of OTA stage and complete proposed VDBA are shown in Figures 8 and 9. One out of the two inputs of FGMOS transistors in the OTA stage is grounded. The transconductance of OTA stage of the proposed VDBA at bias voltage of 0.41V is 483µA/V. The bandwidth of input stage of the OTA is found to be 385 MHz at V_b = -0.41V. Biquad 1 implemented using FGMOS VDBA depicting standard filter functions are shown in Figure 10.

TABLE I. ASPECT RATIOS OF THE TRANSISTORS OF PROPOSED VDBA

Transistors	W(µm)	L(µm)
M_1, M_2, M_3, M_4, M_{10}, M_{11}, M_{15}, M_{16}	7	0.35
M_5, M_6	21	0.7
M_7, M_8	7	0.7
M_9	3.5	0.7
M_{12}, M_{13}, M_{14}	14	0.35

TABLE II. COMPARISON OF CONVENTIONAL AND PROPOSED VDBA

Comparison Parameters	***DO-VDBA [3]***	***FB-VDBA [3]***	***Conventional VDBA [2]***	***Proposed VDBA***
Technology (µm)	0.18	0.18	0.35	0.18
Supply (V)	± 1.2	± 1.2	± 1.5	± 1.35
No. of transistors	8 MOS	16 MOS	16 MOS	12 MOS + 4 FGMOS
Input range of OTA section(mV)	± 200	± 200	±200	±400
Power	Not reported	Not reported	0.97 mW	0.745 mW
Output impedance at V_w (kΩ)	0.053	130	Not reported	1.132
Transconductance (g_m) (µS)	865 at I_B = 100 µA	1740 at I_B = 100 µA	748 at V_{B1} = 0.44V, V_{B2} = 0.9V	483 at V_{B1} = 0.41V, V_{B2} = 0.643V
Port z impedance (kΩ)	170	130	Not reported	101.9
Bandwidth of OTA stage (MHz)	217 at I_B = 100 µA	70 at I_B = 100 µA	Not reported	385 at V_b = -0.41V
Gain of buffer stage (V_w/V_z)	0.962	0.962	Not reported	0.97

Passive component values chosen are $C_1 = C_2 = 100$pF and transconductances $g_{mF1} = g_{mF2} = 483$µA/V. VM biquad in Figure 4 were designed for f_0 = 0.815 MHz and Q-factor of 1. Various responses of the proposed universal filter (Figure 4) are shown in Figure 11. For simulations, equal passive capacitance values $C_1 = C_2 = 100$pF and $R_1 = 5$kΩ are chosen for natural frequency of 0.815 MHz and Q-factor of 1.024. It is seen from the frequency responses of Figures 10 and 11 that the proposed filters are capable of performing standard filter functions. The simulation results emphasize high linearity and high performance of the proposed VDBA in terms of reduced power consumption.

V. CONCLUSION

A new FGMOS realization of VDBA that operates on low voltage with reduced power consumption was presented. Realization of resistorless voltage mode biquad filters is possible with the proposed FGMOS based VDBA and are seen to implement standard filter functions. The benefits of the new proposed VDBA on the filter performance include low-power implementation and simpler circuitry. The proposed circuit and universal filters are intended to find applications in LV/LP ASP and consumer electronics.

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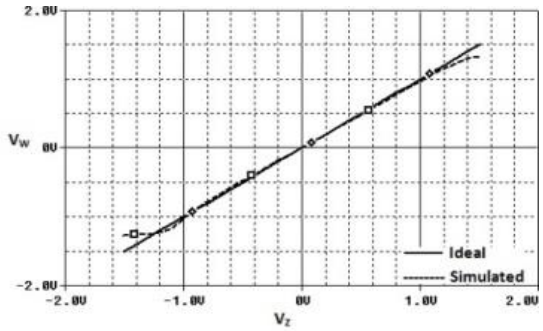

Figure 5. DC transfer characteristic V_W versus V_Z

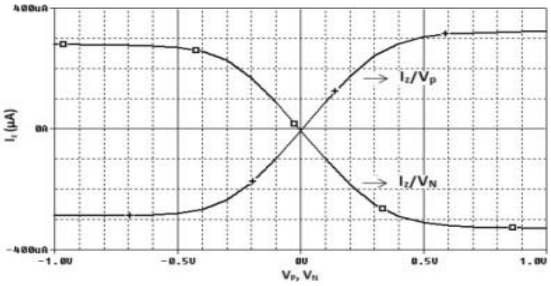

Figure 6. DC transfer characteristic I_Z vs V_P and V_N

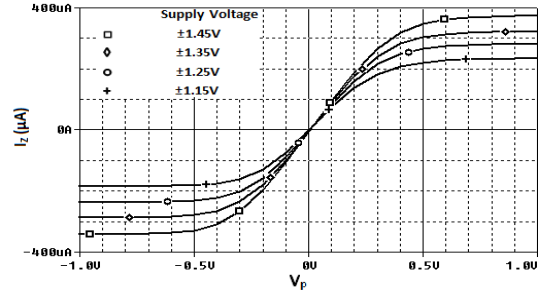

Figure 7. I_Z versus V_P at different supply voltages

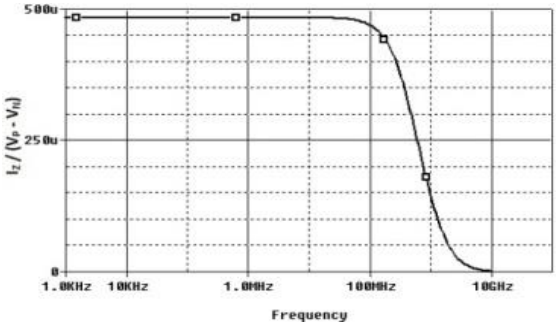

Figure 8. Frequency response of OTA stage

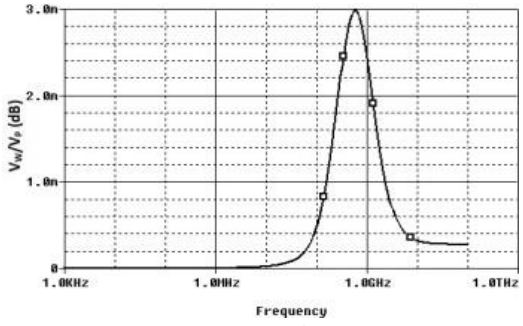

Figure 9. Frequency response of complete proposed VDBA

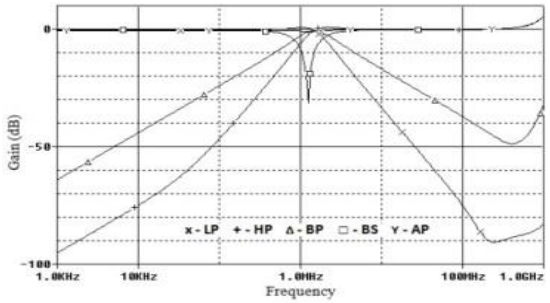

Figure 10. Various responses of proposed universal filter (Biquad 1)

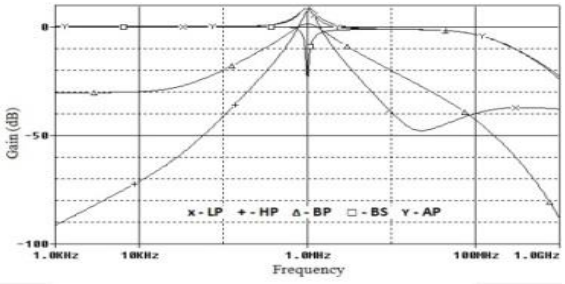

Figure 11. Various responses of proposed universal filter (Biquad 2)

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