A Watt-Level 4G LTE CMOS Reconfigurable Power Amplifier with Efficiency Enhancement in Power Back-Off

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***Abstract*—This paper presents a reconfigurable two-stage power amplifier (PA) for use in 4G LTE unmanned aerial vehicles (UAVs) applications. The PA using the TSMC bulk 65-nm CMOS process exhibits a saturated output power of 29.8 dBm, a power gain of 35.6 dB, a maximum power added efficiency (PAE) of 27.2 % at 2.5 GHz and maintains PAE over 10 % in the output power's 8 dB back-off zone as required by LTE's power-to-average power ratio (PAPR) specifications. The proposed reconfigurable PA architecture, which includes four sub PA cells with the power cell switching (PCS) technique, allows the high level of efficiency in back-off of output power. The four sub-PA cells are composed of three differential cascode stages, supplied by 3.3 V and implemented with the segmented bias (SB) technique to maintain the high level of PAE, reduce the DC power consumption and reconfigure the output impedance.**

Keywords- CMOS; Power Amplifier; transformer; segmented bias; differential; neutralization technique.

I. INTRODUCTION

Since UAVs are highly mobile devices, they need transceivers that minimize space and power consumption whilst facilitating mobile applications requiring high bit rates over wide coverage areas. CMOS, as a powerful platform, has recently demonstrated a tremendous interest in industry with a fully integrated radio system-on-chip (SoC) solution for transceivers. CMOS power amplifiers designed for wireless communications standard, such as LTE, LTE-A and WiMAX, require good performances about output power, efficiency and linearity.

Modern high-data-rate communication systems, using spectrally efficient modern scheme like Orthogonal Frequency-Division Multiplexing (OFDM) with a high power-to-average- power ratio (PAPR), require RF power amplifiers about high linearity and high efficiency. The main challenge for LTE power amplifiers is hence to achieve the good trade-off between high linearity and high efficiency over wide power range. Furthermore, delivering watt-level output power is another challenge for CMOS RF power amplifiers because of low break-down voltage and high knee voltage of transistors. Several techniques hence have been investigated to overcome this limitation of CMOS namely stacked transistors [3].

To find the best linearity/efficiency trade-off while reducing thermal problems, the power cell switching (PCS) technique [1][2], which can be used to combine output power from sub-PA cells, provides a high level of efficiency and preserves a good linearity. To push upper back-off efficiency of PA, a combination of the PCS technique and the segmented bias (SB) [4][5] helps PA not only operate with higher efficiency in a wider range of output back-off power (OBO) but also deal with the problem of short battery life of mobile devices.

This paper proposes a reconfigurable multi-mode RF power amplifier to further enhance efficiency in back-off power zone. The proposed PA is composed of four differential cascode segmented-biased sub-PA cells to achieve high output power and high back-off efficiency, as shown in Figure 1. Implemented in the TSMC bulk 65-nm CMOS process, the PA achieves high efficiency to 8 dB of power back-off and also substantially scales down the thermal power consumption. Its operation modes are controlled by two bias voltages (Vbias1, Vbias2) of each sub-PA cell and two supply voltages (Vdd1, Vdd2).

This paper is organized as follows: Section II discusses the concept and design of the reconfigurable power amplifier. Section III presents the post-layout simulation results. These results include the continuous-wave (CW) simulation data, which meet linearity and output power requirements, with high efficiency for 4G LTE signals at 2.5 GHz. The paper will finish with a short conclusion in Section IV.

II. CIRCUIT DESIGN

A. Design of the proposed reconfigurable power amplifier

The 2.5 GHz CMOS reconfigurable multi-mode power amplifier is implemented and simulated using Keysight's Golden Gate in post-layout simulation.

In Figure 1, the architecture of the proposed reconfigurable multi-mode power amplifier is introduced. The four parallel sub-PA cells are designed in three-stage differential cascode topology with the segmented bias technique and the neutralization technique. The transformer TR1 achieves the impedance matching between the 100 Ohm RF input and the input impedance of driver. The transformer TR2 is a power splitter and can be used as an inter-stage impedance matching network. The transformer TR3 combines the power from the four sub-PA cells and matches the impedance from the four sub-PA cells to the 100 Ohm RF output.

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By switching each sub-PA cell on/off and adjusting the bias point of each transistor in common source of sub-PA cells, this PA can be reconfigured to enhance back-off power efficiency.

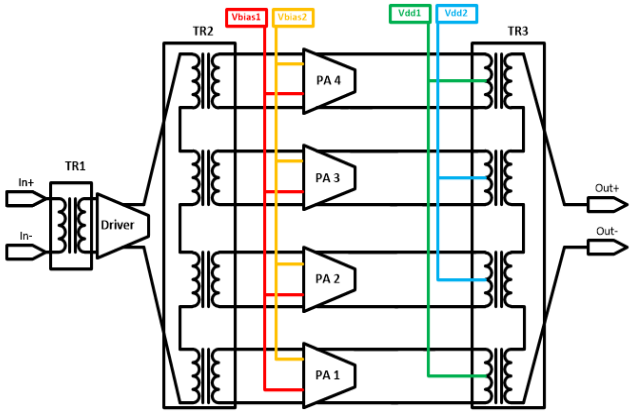

Figure 1. Architecture of the proposed reconfigurable multi-mode PA

B. Design of sub-PA cells

To stabilize each sub-PA cell, two neutralization capacitors C_9, C_{10} [6][7], which dramatically reduce the Miller effect capacitance of differential cascode, are carefully added for the sake of maintaining the circuit in the unconditionally stable region. Their chosen values are fixed at 1.23 pF.

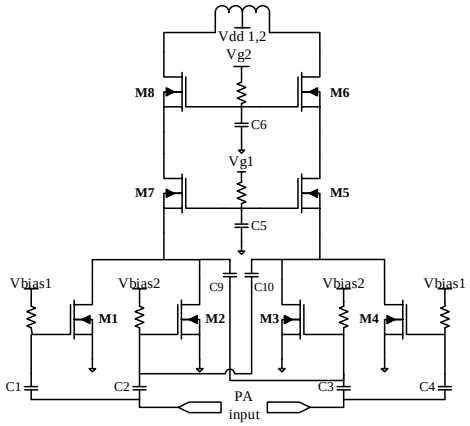

Figure 2. Sub PA cell with the segmented bias technique

In order to increase efficiency of the PA stage, a new topology based on individually biasing the common source stage is proposed in Figure 2. Stacked MOSFET differential cascode structure using deep N-well transistors consists of two common gate (CG) stages and one common source (CS) stage. The capacitors C_5, C_6 at the gates of each stacked transistor are chosen to balance drain source voltage swings of four transistors' CG stages. The external gate capacitance and the gate-to-source capacitance of each stacked transistor form a capacitive voltage divider to produce the proper in-phase voltage swing at the transistor's gate and drain [3]. Transistors M_5, M_6, M_7, M_8 are biased in class AB and sized with a width (W) and a length (L) of 60 µm and 60 nm, respectively.

In the CS stage, transistors $(M_1; M_2), (M_4; M_3)$ are biased separately in class AB with a size of W/3L (20 µm/60 nm) and class C with a size of 2W/3L (40 µm/60 nm) respectively. This method keeps the sub-PA cells in high power and high efficiency region due to the good performances of class AB amplifiers in low power region and of class C amplifiers in high power region. The segmented bias technique (SB) [4][5] allows to significantly scale down DC power consumption compared to class AB.

The estimated size of the sub PA cell's layout is 396.84 µm x 251.5 µm (Figure 10).

C. Design of Driver cell

The driver cell is designed with a differential cascode structure and biased in class AB with deep N-well transistors for the CG and CS stages (Figure 3). The supply voltage (Vdriver) is 2.4 V. This driver aims to increase a level of gain of the PA. The neutralization capacitors C_2, C_3 are also used to make this cell unconditionally stable. The size of the driver is 272 µm x 115.6 µm, as illustrated in Figure 10.

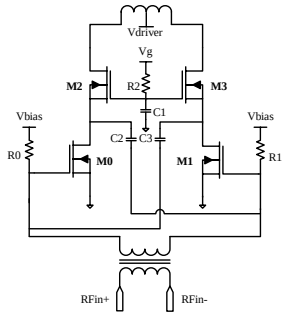

Figure 3. Driver's structure

D. Design of transformers

There are three stacked transformers (TR) [8][9] in the full design. The first one (TR1) in Figure 10 ensures the impedance matching between the driver's optimal impedance and the 100-Ohm input with the size of 252 µm x 674 µm. The second one (TR2) in Figure 10 converts the optimal output impedance of driver to the optimal input impedance of the four sub-PA cells with the size of 197.3 µm x 1706.1 µm. This transformer is also used as a splitter to distribute power homogenously to each sub-PA cell. The last one (TR3) in Figure 10 with the size of 209.3 µm x 1884 µm matches the optimal output impedance of the sub-PA cells to the 100 Ohm output. The transformer TR3 is carefully designed in order to be robust and reliable under high current levels from four sub-PA cells.

E. Reconfigurable states of PA

To fulfill the requirements of 4G LTE signals with high levels of efficiency, the PA can be switched into four possible states in Table. 1 to maintain efficiency over 10% in the 8 dB back-off power zone. The four states are defined by two bias voltages (Vbias1, Vbias2) of the common source transistors and two supply voltages: Vdd1 for the sub-PA cells (1, 4) and Vdd2 for the sub-PA cells (2, 3).

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TABLE 1. CONTROLLED STATES TO RECONFIGURE THE PA

State	Vbias1	Vbias2	Vdd2	Vdd1	Number of active PAs
1A	0.6	0.6	3.3	3.3	4
1B	0.6	0.45	3.3	3.3	
1C	0.45	0.45	3.3	3.3	
2	0.6	0.45	0	3.3	2 (PA 1, PA 4)

Three states 1A, 1B and 1C are used in the high power (HP) region. In these states, four sub-PA cells are all active. More current will be delivered to the load, therefore output power can be increased. These states are determined by Vbias1 and Vbias2 to satisfy the demands of efficiency, output power or linearity. State 2 is used in the medium power (MP) region. In this state, the sub-PA cells 2 and 3 are turned off by having their supply source (Vdd2) off, whilst the sub-PA cells 1 and 4 controlled by Vdd1 are kept on. This configuration is outlined in Table 1.

III. POST-LAYOUT SIMULATION RESULTS

A. S-Parameters results

This PA achieves promising RF performances and performs such good input and output matchings (Figure 4 and Figure 5). The values of S_{11} and S_{22} at 2.5 GHz are all around -20 dB for the four states. The small-signal gains of the PA are 36 dB for state 1A and 30.6 dB for state 2 as shown in Figure 5. Stability of the circuit is illustrated in Figure 4 . The stability factor μ, whose values are over 6 for the four states, guarantees unconditional stability of the proposed PA.

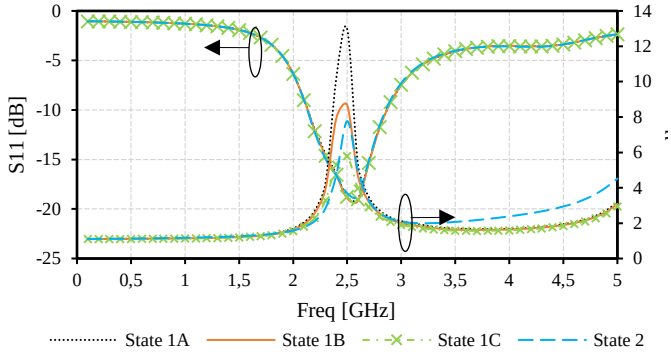

Figure 4. Input return loss $\mathbf{S_{11}}$ and the stability factor μ

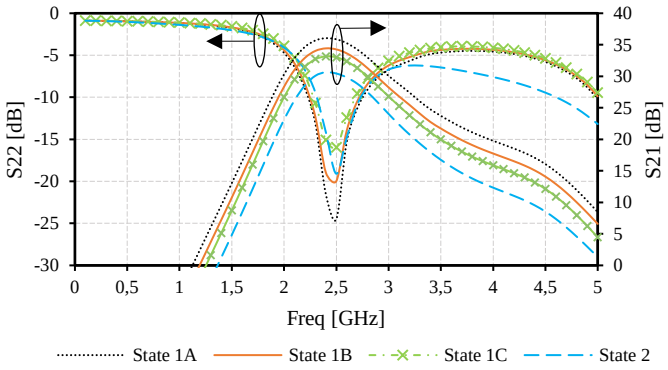

Figure 5. Small signal gain S_{21} and output return loss S_{22}

B. RF performances

The power added efficiency (PAE) is illustrated in Figure 6, the power gain and the output power with 2.5 GHz single-tone signals are shown in Figure 7. Both figures include the post-layout simulated data. Saturated output power P_{sat} of state 1A and state 2 are 29.8 dBm (high power) and 24.8 dBm (medium power), respectively. Maximum power gains of four stages are 35.6, 34.3, 32.8 and 30.1 dB, respectively. PAE at P_{sat} in state 1A is 27.2 % and PAE at 6dB of OBO in state 2 (Pout = 23.8 dBm) is 18 %, improved by 11%. State 2 improves significantly back-off efficiency at the MP region. To fulfill the requirement at 8dB of PAPR, this PA is reconfigured until 8 dB of OBO and reaches 11.8 % of PAE. With the SB technique, DC power consumption is reduced to 2.53 W for state 1B and 1.2 W for state 2 in Figure 8.

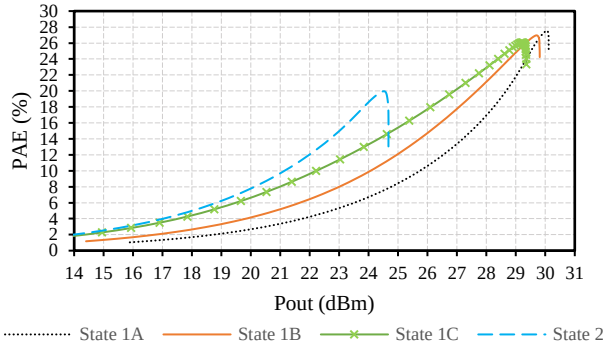

Figure 6. Simulated PAE versus output power

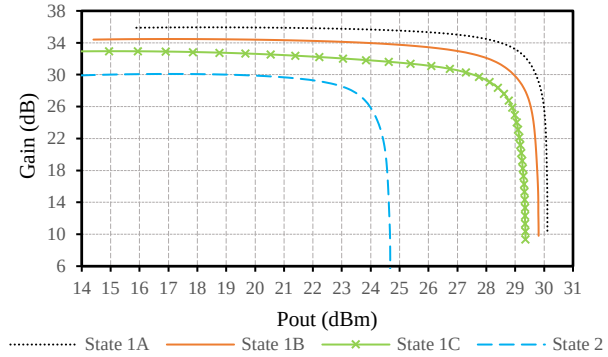

Figure 7. Simulated Gain versus output power

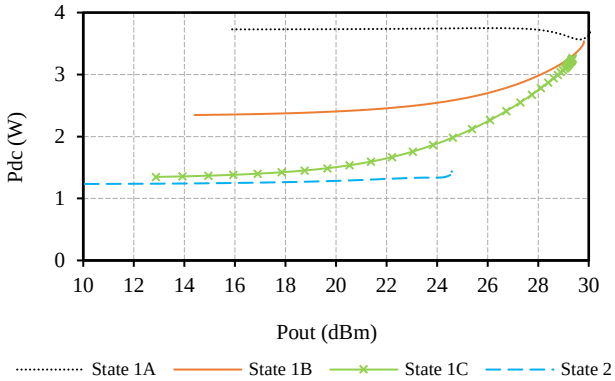

Figure 8. DC power consumption versus output power

TABLE 3. COMPARISON WITH RECENT 4G LTE MULTI-MODE CMOS PAs

Parameter		This work	[10]	[11]	[12]	[13]
Freq. [GHz]		2.5	1.95	0.7 – 1.0	1.7 - 2.0	1.9
Technology		65nm	130nm	180nm	180nm	40nm
PAPR [dB]		8	7	7	7.5	12
Size [mm^2]		2.98	4.48	2.52	1.56	2.94
Supply [V]		3.3	3.3	2	3.5	1.5
Psat [dBm]		29.8	29.3	> 13.6 (P_{-1dB})	26	28
Gain [dB]		35.6	29.3	19.6	15	22
PAE [%]	@Psat	27.2	31	25.5	31.6	34
	@OBO = 3dB	21	23.4	15.4	22.5	28.3
	@OBO = 6dB	19	20.5	-	18	25.5

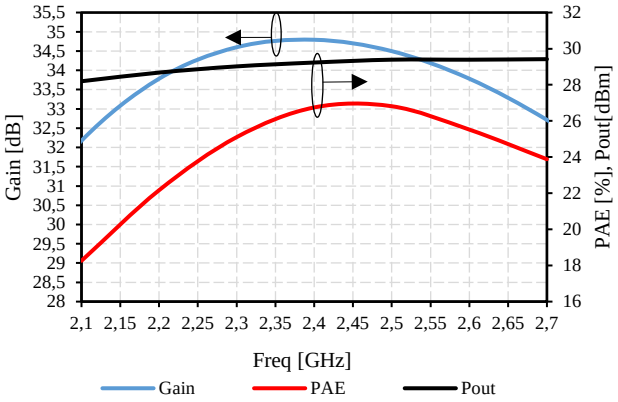

Figure 9. Simulated gain, PAE and output power versus frequency

The 3-dB bandwidth of this PA is 700 MHz from 2.05 GHz to 2.75 GHz, as illustrated in Figure 9.

Figure 10 is the layout of the 65-nm CMOS multi-mode reconfigurable PA. The estimated size of the entire circuit is 1.89 mm x 1.575 mm, including the pads. This layout is the version used for the incoming tape-out.

TABLE 2. CHOSEN STATE ACCORDING TO DESIRED PARAMETER

Desired parameter		State	Values
Max. Gain		1A	36 dB
Max. PAE			27.2%
Max. P_{sat}			29.8 dBm
High linearity P_{-1dB}			26 dBm
PAE in power back-off	High power (HP)	1C	↑ 6.8% @3dB OBO
	Medium power (MP)	2	↑ 8.2% @8dB OBO
Best trade-off	HP	1B	-
	MP	2	-

Table 2 compares this work with other state-of-the-art 4G LTE multi-mode CMOS PAs. This PA achieves a good trade-off between linearity and efficiency. Gain is significantly higher than previous CMOS integrated PAs.

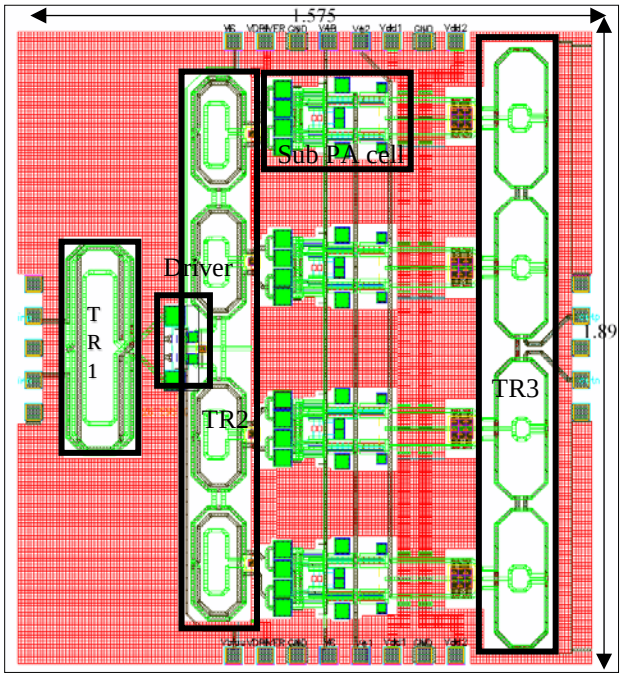

Figure 10. Layout of the reconfigurable power amplifier

Table 3 outlines the operation of this reconfigurable multi-mode PA. States of the PA are selected according to desired parameters. Therefore, the PA's efficiency is notably augmented in back-off power region. Furthermore, this PA is capable of being the best trade-off between efficiency and linearity in state 1B and state 2 for the high and medium power regions, respectively, as shown in this table.

IV. CONCLUSION

In this paper, a fully integrated 4G LTE reconfigurable CMOS PA is discussed and implemented. This PA achieves a maximum output power of +29.8 dBm and a maximum PAE of 27.2 % at 2.5 GHz. Using the segmented bias technique, this PA allows a PAE of over 10 % to be maintained in the output power's 8 dB back-off zone as required by LTE's PAPR specifications. The operation mode of the PA is controlled by two bias voltages of each sub-PA cell in order to trade-off between high linearity and high efficiency.

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Moreover, for the purpose of preserving high back-off PAE, two sub PA cells can be turned off to keep the PAE over 14 % in back-off power zone of 5dB to 7dB.

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