Software Defined Radio Transceiver Front−ends in the Beginning of the Internet Era

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***Abstract*— A mobile terminal today embeds a large number of technologies that maximize its interconnection capabilities. Regardless it is long or short range communication, the wireless terminal is definitely enabled to communicate efficiently over a large number of wireless standards. Nonetheless, the ideal candidate for such a mobile terminal radio front-end is the Software Defined Radio (SDR). This paper overlooks the key features required for a SDR in the beginning of the internet era and brings light on what is the best way to approach the SDR receiver design.**

Keywords-Software defined radio transceiver; multi-standard radio receiver

I. INTRODUCTION

Communication is an intrinsic part of the human nature. Through communication information is conveyed. Today's communication is driven by the Internet.

The Internet foundations were laid in 1960s by the USA military research projects aimed at building distributed computer networks. The internet mass global spread was delayed due to lack of networking infrastructure and limited number of PC users. But, in mid 1980s the PC market boomed due to IBMs Personal Computer based on Intel 80286 microprocessor and operated by Microsoft's Disk Operating System (MS-DOS). This combination formed the template for all PC developers and vendors.

Hence, during the 1990s, it was estimated that the number of Internet users doubled each year, with a brief period of explosive growth in 1996 and 1997. By end of 2011, the Internet reached 32.5 users per 100 inhabitants worldwide, see Fig. 1, [1].

In order to show the strong relation between the IT industry and the communication sector, Fig. 1 plots the number of worldwide subscribers of fixed and mobile telephone networks and Internet users. The Internet access connects the two sectors.

The Internet was initially developed as a "wired" network. Nevertheless, as Fig. 1 reveals the latest trends show the communication sector is strongly going mobile, as today the mobile subscribers number surpasses the fixed telephony ones by a factor of five.

Therefore, radio circuits designers need to account this trend and focus on the development of efficient solutions that maximize the mobile's terminal wireless interconnectivity.

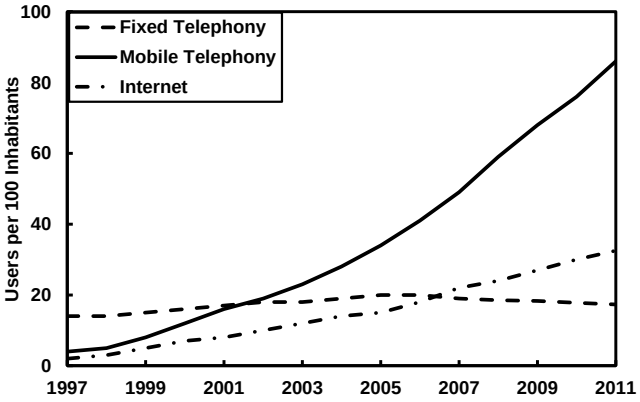

Figure 1. Internet usage – the driving force behind the need for SDRs

Section II overviews the historical development of wireless transceivers and defines the need for SDRs as the next step in the optimization process of wireless front-ends.

Section III overviews the generic SDR structure that is implemented in today's Systems on a Chip (SoCs), while in Section IV a designed receipt is proposed for the SDR receiver (SDRR) front-end.

Finally, the paper is concluded by Section V, which also overlooks the future developments.

II. THE NEED FOR SOFTWARE DEFINED RADIOS

A basic modern communication system is comprised by a large array of mobile equipment connected into wireless networks.

The communication between all these equipment is regulated by various communication standards, depending on the type of wireless network in which they operate.

Our lives today are bounded by the Internet. As presented in Section I, Internet access is possible over a wide array of wireless standards.

Hence, purely on the communication side, the present mobile equipment requires compatibility with all the standards maximizing its interaction capabilities: GSM/GPRS, UMTS, LTE, Bluetooth, Wireless LAN, LTE, WiMAX or DVBH.

Unifying the various communications standards is not a real possibility, given the huge number of users dedicated to a given wireless standard.

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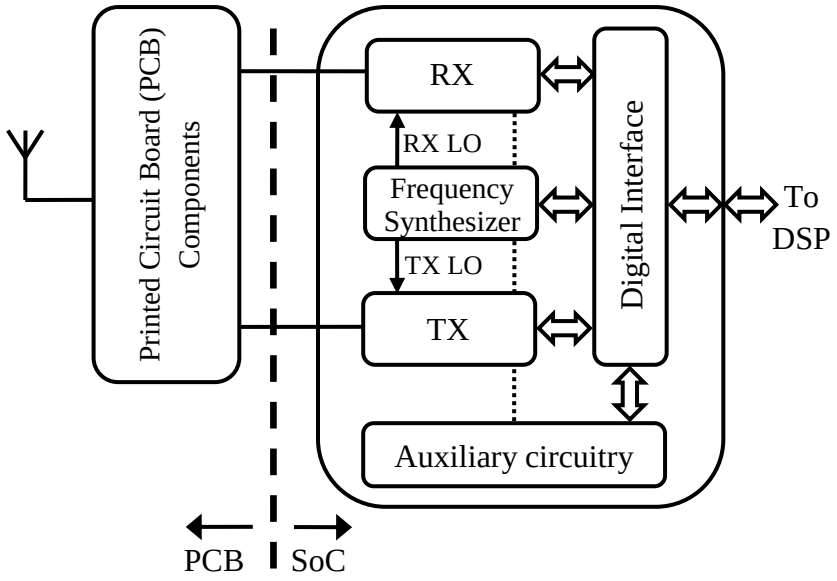

Figure 2. Software Defined Radio Transceiver Generic Block Schematic.

Therefore, there is a need of mobile equipment that enables wireless communication across the various wireless environments.

The first obvious solution was to incorporate for each standard a separate dedicated IC or Application Specific Integrated Circuit (ASIC) into the mobile device. One still has to have in mind the first Nokia mass production GSM mobile phone. The Nokia 1011 developed in the early '90s, was built from more than two dozen separate ICs and weighted about half a kilo [2]. By mid 2000's, solutions offering fully integrated quad-band GSM SoCs, [3] were already available.

A first step in reducing the cost for radio frequency (RF) front-end chips was enabled by the CMOS technology scaling. It opened the possibility of building "combo" ASICs, combining two or more SoCs on the same IC (e. g., BRCM2071 [4] that integrates Bluetooth, GPS and FM radio or BCM4325 [5] that incorporates W-LAN, Bluetooth and FM radio). However, these circuits still contain one RF front-end per communications standard.

Moving forward, the natural step in the development of multi-standard communication is building a reconfigurable ASIC, able to ensure compatibility with the wide array of communication standards in use today. Such and approach is efficient from two main reasons [6]:

- One "universal" design is required; thus design, packaging and testing costs are minimized, and
- As the "universal" ASIC is compatible with a wide array of wireless communication standards the previous various ASICs can be merged; thus the overall area of ASICs comprised in a mobile terminal is minimized.

In the "digital" realm the first step on this path is the development of the new multi-core Digital Signal Processor (DSP) architectures [7]. Such processors optimally leverage the power consumption with the IC cost, or equivalently its die area.

The idea behind it is to enforce as much parallel processing as possible to maintain a maximum "usage" of the chip die area during operation.

In this context, it is required to develop an RF transceiver capable to interface such a DSP. This RF transceiver is the Software Defined Radio (SDR).

III. TODAY'S SOFTWARE DEFINED RADIO TRANSCEIVER FRONT-ENDS

The RF transceiver SDR must employ a versatile architecture, able to change its characteristics dynamically given the particularities of each wireless standard and communication burst it has to handle.

The software driven System-on-a-Chip (SoC) combining such a re-configurable RF front-end and a multi-core DSP represents the Software Defined Radio (SDR). The block schematic of such a system is depicted in Fig. 2.

The four main blocks comprising the SDR RF front-end of Fig. 2 are:

- the frequency synthesizer (FS),
- the receiver (RX),
- the transmitter (TX), and
- the auxiliary circuitry (AUX)

The transceiver acts as a signal conditioning block. It either prepares the received signal for digital demodulation or it shapes the digitally modulated signal for the wireless transmission.

The DSP drives the RF front-end via the digital interface. By dynamically changing the transceiver settings, its performance can be adjusted depending on the requirements (e. g., noise or linearity performance, output power level) of the particular communication burst.

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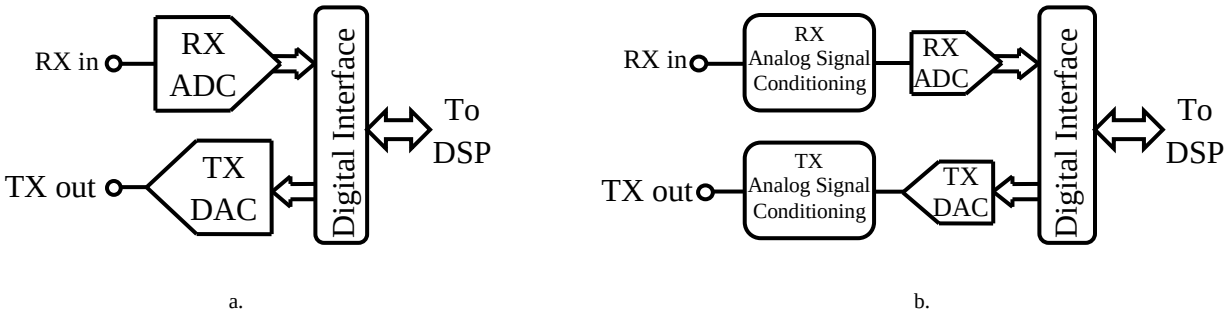

Figure 3. Software Defined Radio Simplified Block Schematic (FS and AUX not shown): a. Mitola's Concept; b. SDR embedding analog signal conditioning.

The FS is the RF transceiver "heart". Its beat is represented by the generation of the local oscillator (LO) signals which drive the receiver (RX LO), respectively the transmitter (TX LO).

The task of any wireless receiver is to condition the incoming wanted signal such as it can be properly demodulated.

Oppositely to the RX, the TX chain must ensure the up conversion on the RF frequency of the digitally modulated baseband signal. In the transmitter case the accent is placed on avoiding the disturbance of adjacent radio frequencies and maintaining a good signal integrity.

The auxiliary circuitry is mainly formed by the front-end's biasing block.

Fig. 6.a reveals the optimal choice from system level perspective for the TX and RX implementation. This multi-standard RF transceiver concept was coined by Mitola in [8]. Basically the RX is only an Analog-to-Digital Converter (ADC) and the TX is a Digital-to-Analog Converter (DAC). Of course, the transceiver requires a FS system to generate the ADC and DAC clocks.

In reality, due to practical implementation constrains, today's SDRs require analog signal conditioning blocks in between the antenna and the ADC and in between the DAC and the antenna (e. g., [6],. [9-11]). The SDR concept shown in Fig. 6.b relaxes the ADC and DAC electrical specifications by ensuring for the wanted signal the frequency translation and additional selectivity and amplification.

IV. A DESIGN RECEIPT: THE SOFTWARE DEFINED RADIO RECEIVER FRONT-END

In order to enhance the wireless system robustness and maximize the link budget, the latest wireless standards are very flexible (e. g, the IEEE 802.11g W-LAN uses BPSK, QPSK, QAM-16 and QAM-64 modulations on OFDMA carrier support).

Considering the abovementioned trend, as previously discussed it results the SDR is the natural solution for the radio front-end. For the receive side, the software re-configurable hardware solution is the Software Defined Radio Receiver (SDRR).

As in-depth analyzed in [12], given the huge amount of information the SDRR designer(s) need to handle, a *structured approach* of the design process is the enabling factor in finding and implementing the optimal circuit design.

First the most suited architecture for the SDRR front-end needs to be identified. The homodyne architecture stemmed out as the best choice that matches very well the high level of integration of the current deep sub-micron CMOS processes [13, 14]. Fig. 4 presents the re-configurable homodyne radio receiver [6].

The incoming RF signal is picked-up by the receiver's antenna and is amplified by one of its LNAs. Multiple LNAs can be integrated, depending on the envisaged use. The amplified RF signal is then converted to current in the mixer input gm-stage and down-converted directly to baseband by mixing with a local oscillator signal of equal frequency. Hence, at the mixing stage output the signal has a spectrum spanning from DC to a maximum frequency that is dependent on the wireless communication standard [15].

After mixing, the signal is conditioned by a low pass filter (LPF) and a variable gain amplifier (VGA), before its conversion to digital spectrum by an analog-to-digital converter (ADC).

Second the designer has to be enabled to handle efficiently the large amount of information comprised in the wireless standards. The most effective way to do so is based on simple and efficient models suited for manual analysis.

In [16], the author introduces the SDRR *generic blockers diagram* as a very efficient tool in evaluating, in a standard independent approach, the filter partitioning for channel selection in multi-standard radio receivers. By mapping all blockers and interferers arriving at the receiver's antenna, the *generic blockers diagram* enables the designer to evaluate proficiently the trade-off between the analog low pass filter order and the ADC specifications of resolution and speed, or equivalently the trade-off between its area and power consumption. Thus the optimal analog low pass filter order is determined.

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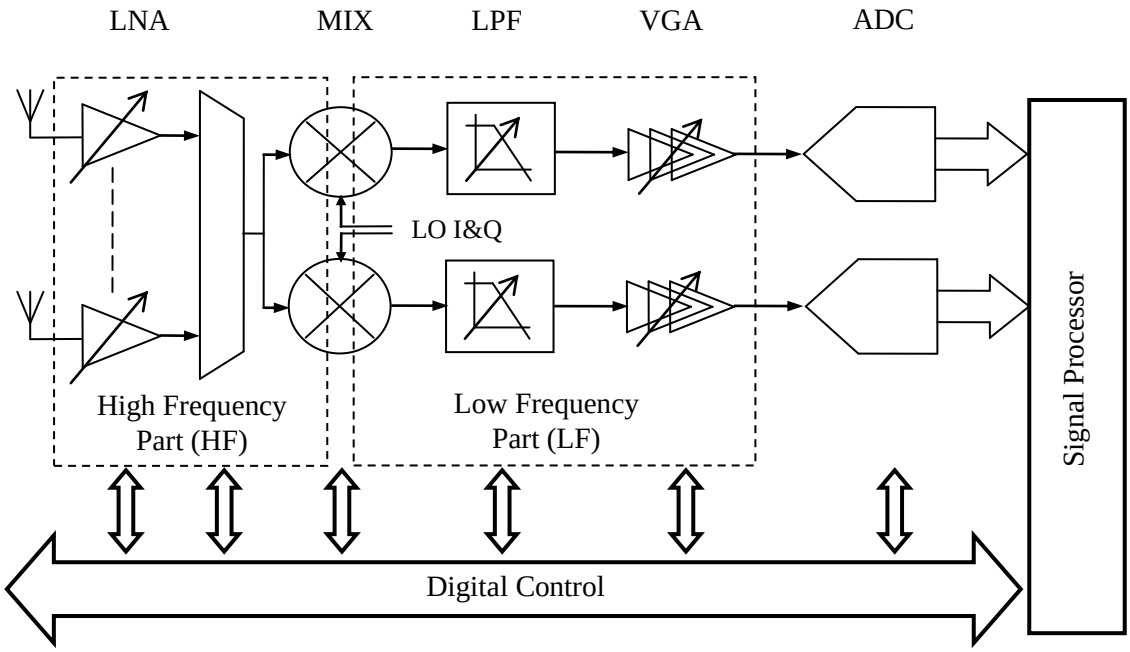

Figure 4. Software Defined Radio Transceiver Block Schematic [6].

In [17], the author introduces the *smart gain partitioning strategy* for multi-standard radio receivers. The strategy aims to aid the designer in identifying the optimal leverage between the receiver noise and linearity performance. Depending on the received signal strength, the receiver can change its noise or linearity characteristics accordingly (e. g., for large signal inputs the receiver will require a highly linear response, while it can tolerate more noise).

In the analysis from [17], the receiver gain thresholds at which the changes are triggered are calculated for various commercial standards. Thus, the designer is enabled to optimally handle the gain-noise-linearity partitioning. Of course, in order to enhance the model accuracy all these results should subsequently be completed by CAD simulations.

Third the designer needs to develop the SDRR front-end design strategy from both the system level and transistor level perspectives and to use this strategy to design the front-end's building blocks. As described in [18], the strategy needs to ensure the SDRR building blocks have the following characteristics:

- high linearity and low noise,
- immunity to particular technology characteristics and
- easiness of the design porting.

Basically, these targets are achieved by building *modular* RF, respectively baseband *circuits*, based on differential or pseudo-differential transistor pairs [18], respectively low power feedback amplifiers [19, 20].

V. CONCLUSIONS AND FUTURE TRENDS

This paper presented an overview of the key feature of software defined radio transceivers front−ends in the beginning of the internet era. The need for mobile equipment able to maximize its interconnection capabilities in conjunction with the VLSI integration have open the door for the SDR approach. Multi-core digital signal processors interfaced by flexible analog front-ends represent today's SDR.

Their transceiver front-ends employ a versatile architecture, able to change its key parameters dynamically (i. e., gain, noise, linearity performance and power consumption) based on the particular characteristics of the radio burst it handles.

Today's SDR front-ends are embedding analog signal conditioning blocks. Nevertheless, looking into the future and considering the rate at which the CMOS technology scales down, more and more signal processing is translated from the analog into the digital domain.

By making use of the relative inexpensive digital gates the modern transceivers analog circuits content is reduced [21]. This will impact the architecture of choice for all of the three key functional building blocks of the Fig. 5 SDR.

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