

Next Generation Power Distribution System Architecture: The Future Renewable Electric Energy Delivery and Management (FREEDM) System

Alex Huang, Xu She, Xunwei Yu, Fei Wang, and Gangyao Wang
 Future Renewable Electrical Energy Delivery and Management Systems Center
 North Carolina State University
 Raleigh, NC, US
 {aquang, xshe, xyu8, fwang5, gwang3} @ncsu.edu

Abstract—This paper presents the envisioned next generation power distribution system architecture, the so called FREEDM system. The presented system enables the plug-and-play of distributed renewable energy resources and distributed energy storage devices, therefore functions as the “energy internet”. The recent technical developments are summarized in this paper, with emphasis on the distributed grid intelligence, solid state transformer, DC microgrid, and fault isolation device. It is demonstrated that the FREEDM system is a highly attractive candidate for the future power distribution system.

Keywords-Smart grid; Microgrid; distributed generation; energy storage; DNP 3; Solid State Transformer.

I. INTRODUCTION

The future renewable electric energy delivery and management (FREEDM) system center is a US National Science Foundation (NSF) generation-III Engineering Research Center (ERC) established in 2008 headquarters at North Carolina State University, US. The mission of the center is to develop the fundamental and enabling technologies for future power distribution system, which is called the FREEDM system [1].

Figure 1 shows the one-line diagram of the proposed FREEDM system, which integrates the advanced power semiconductor devices technology, power electronics technology, and information technology. The FREEDM system achieves seamless integration of distributed renewable energy generation and storage, therefore enables highly intelligent and distributed power grid architecture. Some key features of this innovative power grid are:

1. Plug and play of distributed renewable energy resources (DRER) and distributed energy storage devices (DESD).
2. Intelligent energy management (IEM) system through the revolutionary solid state transformer (SST) concept with direct interface to the distribution system.
3. Intelligent fault management (IFM) system with fast fault isolation capability by adopting the solid state fault isolation device (FID).
4. Distributed grid intelligence software embedded into the IEM and IFM.
5. Reliable and secured communication infrastructure to enable real time monitoring and control of all the nodes in the system.

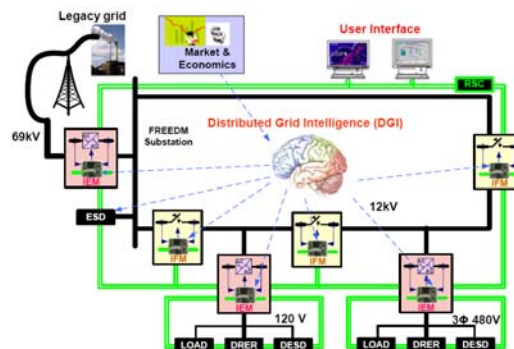


Figure 1. Electric grid diagram of the FREEDM system

In order to demonstrate the envisioned FREEDM system, recent efforts are made towards the living demonstration of a future home in the FREEDM system [2], as depicted in Figure 2. In this diagram, the DGI and SST are integrated to function as IEM. SST delivers 380V DC to the plug-and-play DC microgrid as well as 120/240V AC to the traditional AC load. FID is installed in the 12KV distribution line to isolate the fault current. Digital communication infrastructure based on DNP3 is also designed to enable the power management and condition monitoring of the whole system. Some breakthroughs have been achieved for the key components of such a system, including DGI, SST, DC microgrid, FID, and IEM.

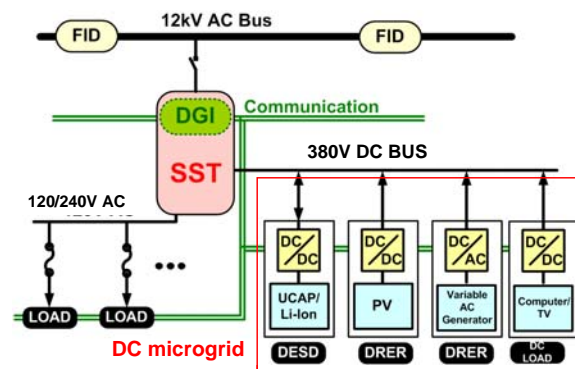


Figure 2. Electric grid diagram showing the interface of a future home in the FREEDM system

This paper summarizes and reports our newest progress in these areas. The hardware and software development of distributed grid intelligence was introduced in section II. In section III, two generations of solid state transformer are

presented with their characteristics highlighted. In section IV, the plug-and-play DC microgrid platform is illustrated. In section V, the development of Si based generation-I FID is presented. Lastly, the paper is concluded in section VI.

II. DISTRIBUTED GRID INTELLIGENCE

The DGI acts as the brain of the proposed FREEDM system. The diagram of DGI is shown in Figure.2, where green line represents the communication link, while black lines the electricity path. The main function of DGI is to collect information and manage power flow within a FREEDM hub or among multiple FREEDM systems over a wide area. Therefore, the hub is inherently distributed with components of the DGI algorithm executed on independent hardware within IEMs and IFMs. The DGI hardware is then required not only for localized control within each IEM and IFM, but also to implement control functions that must be handled collectively by groups of IEMs and IFMs. For DGI software, the main intelligence implemented is based on the multiple levels of control and time scales. The key challenge is to partition and distribute these controls as cooperating agents over multiple microprocessors within each IEM [3].

The distributed controller consists of a customized local controller that directly interacts with power converters and a commercial ARM board for communication implementation [4]. The division of hard real time and soft real time are therefore realized based on this hardware partitioning. A web based human machine interface (HMI) is also developed for system monitoring over the communication links. System operator can intervene the operation of SST by dispatching command through this HMI.

A. DGI Hardware Platform

The DGI hardware platform consists of three major components, namely, interface board, local controller board and ARM communication board, as shown in Figure 3. These three components can be stacked on top of each other to form a compact and reliable structure [4].

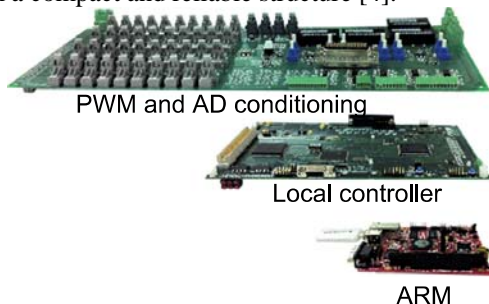


Figure 3. DGI hardware platform

The interface board (the top one in Figure. 3) is equipped with PWM output, analog conditioning circuit and fault protection. On the left side, there are 40 channels of optical fiber output to transmit switching signal to power devices.

These PWM signals are tied with fault protection signals in order to quickly turn off the power stage during fault situation. There are also 16 channels of analog conditioning circuit that has an output range of $-10V$ to $+10V$. Fault signals are generated using voltage comparators to compare the outputs of the conditioning circuit with tuned threshold values. The number of these channels is adequately designed for most of our converter applications in FREEDM, which means this hardware platform is universal and little modification is needed for new deployment.

Converter control is executed in local controller board (the middle one in Figure.3), which is able to work under both standalone and network modes. The circuit structure is based on combination of DSP and two FPGAs, as shown in Figure 4. With development of the IC technology, FPGAs have become the main stream in complex logic circuit design due to its flexibility, ease of use, and short time to market. In this structure, the major function of FPGA #1 is to implements PWM generation and interrupt the DSP periodically to evoke control loop. Once the DSP receives this external interrupt, an interrupt service route program is called and the control algorithm is executed. First step of the control algorithm is to sample converter voltage and current, this is done using FPGA #2 to generate AD control logic and pass the sampled value to DSP on data bus.

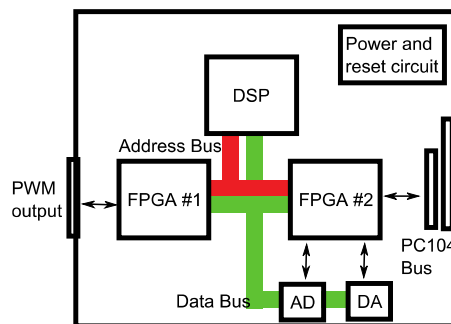


Figure 4. Functional diagram of Controller board

In order to transmit data to the ARM communication board, FPGA #2 is also implemented with a PC104 bus interface that can achieve fast and reliable data transmission. With the high performance bus access, the local controller is able to deliver measurement to and receive reference from the ARM communication board TS-7800 (bottom in Figure.3). The TS-7800 board features a Marvell 500MHz ARM9 SBC, which provides high end peripherals including gigabit Ethernet. The ARM board runs Linux 2.6 kernel with a full Debian distribution in on-board flash. PC104 bus is one of its external memory/program peripherals.

B. Design and Implementation of SST Communication

The objective of the communication system is two-fold: (1) the SST can send acquired measurement to the control center; (2) the control center can also send control commands and reference to the SST. To achieve such bidirectional communications between the SST and the

control center, we designed a systematic architecture as shown in Figure 5 [5]-[6]. Based on the hardware structure, the SST communication system is composed of two domains: network domain and device domain. In the network domain, a control center is connected to the distributed controller via a Local Area Network (LAN) over a DNP3 protocol stack. Thereby, the collected data and dispatched control commands can be delivered via DNP3 packets between devices. In terms of the device domain, it features aforementioned PC104 bus as data path to exchange data between the local controller and the ARM board.

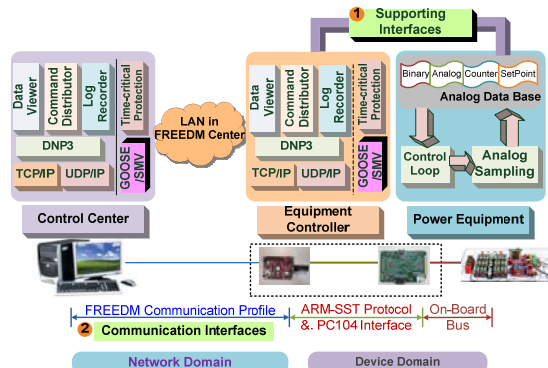


Figure 5. Communication schemes implemented at local DGI node

Since DNP3 over TCP/IP is employed as the underlying communication protocol, the design principal of network applications is to leverage basic DNP3 functions for the SST monitoring. We then introduce the network applications setup in a top-down manner. Left block in Figure. 5 depicts the application design in the network domain. Since DNP3 commonly works in a master/slave mode, the applications setup is correspondingly divided into two parts for the master and the slave. We envision three basic tasks on the master, including data query, command distribution and log collection, which are mapped into three modules, data viewer, command distributor and log recorder respectively. To support data query and modification in Data Viewer and Command Distributor, a database is programmed to store data from the device or issued by the Command Distributor. Two data channels are furnished under the database to retrieve data updates from the DNP3 function blocks, or dispatch commands to function blocks. As DNP3 is overlaid over TCP/IP in the communication layer model, the generated DNP3 packet will be fed to the slave via a TCP/IP channel. On the slave side, the application design is the same with that on the master.

III. SOLID STATE TRANSFORMER

The SST is a power electronic device that replaces the traditional 50/60 Hz power transformer by means of high frequency transformer isolated AC-AC conversion technique, which is represented in Figure. 1 [7]. The basic operation of the SST is firstly to change the 50/60 Hz AC voltage to a high frequency one (normally in the range of

several to tens of kilohertz), then this high frequency voltage is stepped up/down by a high frequency transformer with significantly decreased volume and weight, and finally shaped back into the desired 50/60 Hz voltage to feed the load. In this sense, the first advantage that the SST may offer is its reduced volume and weight compared with traditional transformers.

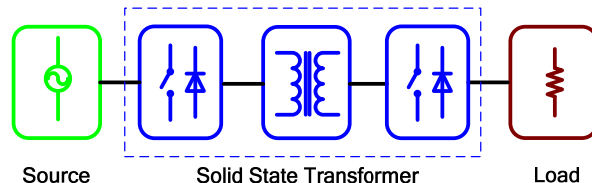


Figure 6. Solid state transformer configuration

It is further seen from the configuration of the SST that some other potential functionalities that are not owned by the traditional transformer may be obtained. First, the use of solid state semiconductor devices and circuits makes the voltage and current regulation a possibility; similarly to FACTS devices. This brings promising advantages such as power flow control, voltage sag compensation, fault current limitation, and others, which are not possible for traditional transformers. Therefore, the SST can enhance the stability and controllability of the power distribution grid. Second, voltage source converters connected from the secondary terminal of the SST could readily support a regulated DC bus, which could be connected to DC microgrids enabling the new microgrid architecture.

As a benchmark, a laboratory prototype of a 7.2 kV, 20 kVA single-phase, three-stage SST was built, which is named Generation-I (Gen-I) SST [8]. The topology of the Gen-I SST is illustrated in Figure 7.

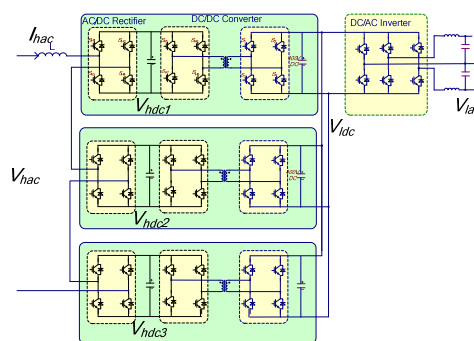


Figure 7. Topology of Gen-I SST based in Si IGBT

Cascaded multilevel rectifier with three H-bridges is adopted as the front-end stage. Three dual active bridge (DAB) converters are connected to each DC link with secondary side parallel as the DC/DC step down stage. In the last stage, the split phase inverter is adopted to provide both 120 and 240V AC.

The hardware prototype is shown in Figure .8. 6.5kV, 25A silicon based dual insulated gate bipolar transistor (IGBT) were customized and adopted for the rectifier and primary side of the DAB stages. It was packaged by POWEREX with chips supplied by ABB. 600V

commercial intelligent power modules (IPM) were adopted for the secondary side of the DAB and inverter stage. Based on the chosen power device, the switching frequency for the high voltage side rectifier, medium voltage DC/DC stage, and low voltage inverter stage was 1.2 kHz, 3.6 kHz, and 10.8 kHz respectively. A Metglas AMCC 1000 core was paralleled and used for the high voltage and high frequency transformer at an operating frequency of 3 kHz. The transformer was naturally cooled with the maximum temperature around 45 °C. Based on the detailed test results of the power device used in the power stage, PLECS simulations were used to estimate the efficiency of the converter, and the efficiency for this prototype at full power rating was close to 88 %.

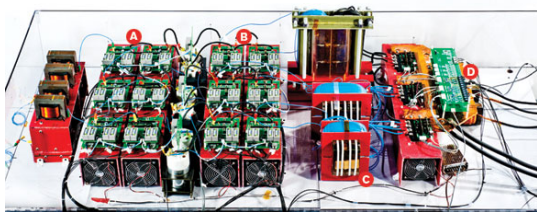


Figure 8. 20KVA three-stage SST based on 6.5KV Si IGBT

In order to realize the remote control and monitoring of the SST, the designed DGI hardware shown in Figure .3 is adopted. In this condition, this unit can be utilized as the IEM in the FREEDM systems. A HMI is developed for the whole FREEDM system, and Figure 9 shows the page for the SST control and monitoring. In this condition, all the data, including the command and the operating status information, can be transmitted between the DGI imbedded in the SST and the central controller server.

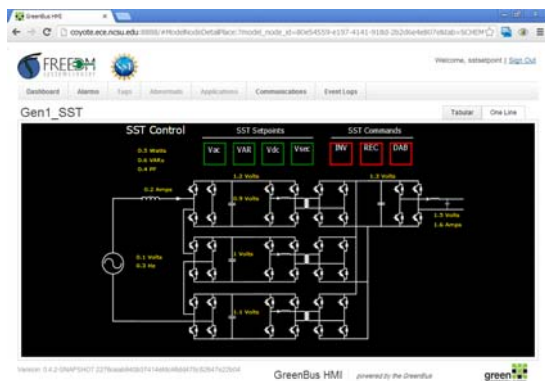


Figure 9. Control center webpage

Test result of the Gen-I SST is shown in Figure .10. The input AC voltage is 1.2KV, high voltage DC is 2.28KV, low voltage DC is 380V, and low voltage AC is 240V. The power rating is about 4KVA. The delivered 380V DC bus is readily for use to the plug-and-play DC microgrid.

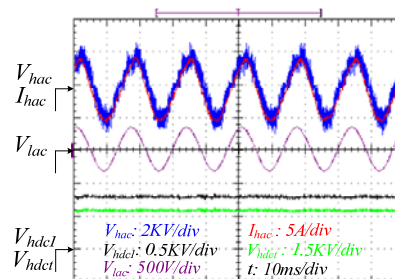


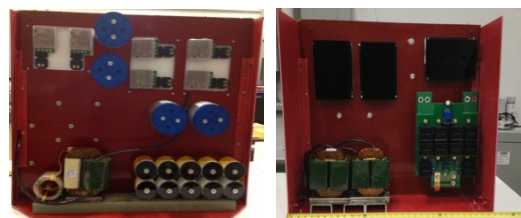
Figure 10. Test waveforms of Gen-I SST

The efficiency achieved was low mainly because of the relatively low power rating [9]. For MVA level design, the expected efficiency is higher than 95 %. In addition, the volume and weight of the SST was not effectively reduced compared with traditional transformers due to the relatively low operating frequency and large volume of power devices, heatsinks, and capacitors.

The performance improvement of the SST could be carried out in the following aspects:

1. Use of the SiC devices to increase the switching frequency as well as control the losses.
2. Use of nanocrystalline core to operate the transformer at a higher switching frequency.

Based on these considerations, another three-stage solid state transformer based on 15 kV SiC MOSFET was built, which was named Generation-II SST, as shown in Figure. 11.



(a) Front side: High voltage side; (b) Back side: Low voltage side
Figure 11. 20KVA SST based on 15KV SiC MOSFET

The newly developed 15 kV SiC MOSFET was adopted in the high voltage side and several low $R_{ds(on)}$ MOSFETs were paralleled to be used in the low voltage side [9]-[10]. A nanocrystalline core was used to assemble the 20 kVA high voltage transformer, which operates at 20 kHz. A certain soft-switching technique for the high voltage rectifier stage was adopted to solve the problem of high dv/dt introduced by the high switching speed. By using the measured loss data of the power devices, the estimated efficiency for the new Generation-II SST is close to 97 % [10]. In addition, its volume is about one third of the Generation-I SST. Therefore, the performance can be potential improved.

IV. PLUG-AND-PLAY DC MICROGRID

The plug-and-play DC microgrid is one of the most attractive solution for future residential application due to its good scalability. As shown in Figure 12, the envisioned DC microgrid system is constructed. It includes: two DRERs (PVs) and DESDs (batteries), which are used to simulate multiple DRERs and DESDs, local loads and a SST, where the arrows show the modules power flow directions. Two unidirectional DC/DC converters are used for PVs to transfer power generated by PVs into the system, and two bidirectional DC/DC converters are used for batteries to balance the power differences between loads and the power supplied by PVs in islanding mode. The local load and the SST share a common 380V dc bus. The DC bus voltage can be enabled by the SST's output or be regulated by the battery's DC/DC converters. Correspondingly, when the SST disconnects from the microgrid system, the dc microgrid operates in the islanding mode; while the SST connects to the system, the microgrid enters into the SST-enabled mode. In SST-enabled mode, the batteries can be charged or discharged through their converters automatically based on their control algorithms.

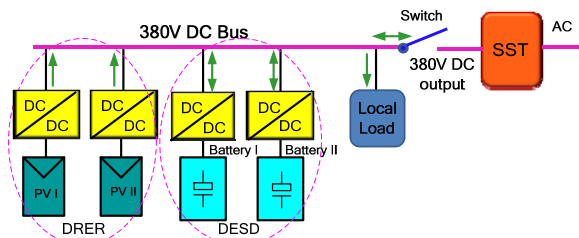


Figure 12. Diagram of plug-and-play DC microgrid

In the following discussion, the system's power management strategy is presented based on the Figure .11, including PV module control algorithm, battery control algorithm and plug and play function [11].

A. PV module control algorithm

The Maximum Power Point Track (MPPT) [12] control algorithm is shown in Figure 13.

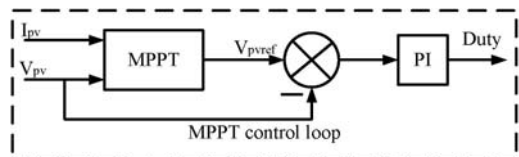


Figure 13. PV control algorithm.

V_{pv} is the PV panel's actual output voltage and V_{pvref} is the voltage reference, which is based on the MPPT curve. The difference of the two values as input to a PI controller is used to control the PV DC/DC converter.

B. Battery module control algorithm

To control each module distributed, integrate more DESDs into the system conveniently and implement the

plug and play function without the communication ports involves, the droop control [13] for the battery is adopted. Comparing to the other methods, the droop control has its own advantages when it applies to microgrid system, either in islanding mode, SST-enable mode or transient mode, because the module can be controlled independently based on its local information (its output voltage and current) and no need to be aware of other modules' or system's information. Their droop curves are shown in Figure 14 (a). 380V is a critical value. When the DC bus voltage is greater than 380V, batteries are in charging mode; otherwise they are in discharging mode. 400V and 360V are the upper-limit and lower-limit values for the DC bus voltage. In islanding mode, all battery modules share the current to balance the power difference between the PV generation and load, and regulate the DC bus voltage according to their droop curves. Generally, the bigger rating battery, which has smaller slope will share more current than the smaller one. In SST-enabled mode, the DC bus is regulated by the SST and the batteries can be still in droop control. Battery modules are in charging or discharging mode, which are determined by the bus voltage enabled by SST. As a result, when system is in transient mode, whether the system switches from the islanding mode to SST-enabled mode or on the other way, there is no need to change the batteries control algorithm. The droop control diagrams for batteries are shown in Figure 14 (b).

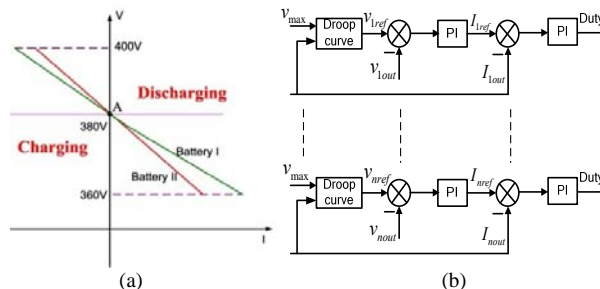


Figure 14. (a) Batteries droop curve; (b) Batteries control algorithm

C. Database

To supervise the operation of the whole system, a control center is constructed and the communication architecture is shown in Figure.15. Considering the DESD and DRER might be far from the control center, wire communication is unrealistic, thus a wireless communication port is adopted. The communication board (TS7800) [14] is interfaced with the each DSP board and transforms the SCI signals into WIFI signals, then the WIFI signals are transited to the control center. As a result, the control center of the DC microgrid collects the whole system information and a database is built to store all information. On the front-end of control center, Java Server Pages (JSP) are used to build up the webpage, which shows the real time data from each device and module's plug or unplug status, as shown in Figure 16(a). On the back-end of control center, a database is set up by Mosel to save all system history information in control center, as shown in Figure 16(b). This database can query the TS7800 board for the data based on the

customer’s required period and then display the history data on the webpage. Furthermore, these data will automatically store into the database in the specified space, because each device has its own space to save data in database according to their IDs. In addition, since each device has its own ID in the control center, when the device re-plugged into the system, it can be recognized by the control center then its data can be saved into the corresponding space. Furthermore, the dynamic arrows are added on the webpage to show the module power flow direction and the battery arrow direction are bidirectional since it operates bidirectional as discussed in section III. The webpage of control center is shown as followings.

In order to verify the proposed power management strategy, experimental tests have been carried out on an experimental setup in a laboratory. A 380V DC microgrid is constructed, which consists of two PV panel modules, two batteries modules and one local resistor load bank, which share a common dc bus. A DC power supply is used to supply the DC bus voltage to emulate SST-enabled mode.

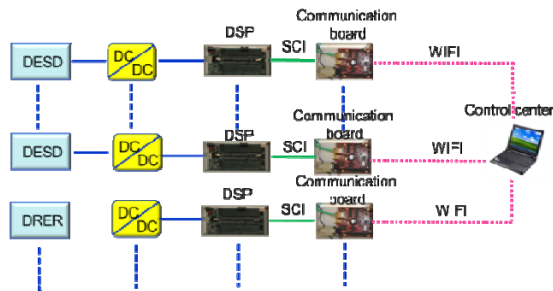


Figure 15. Communication architecture for DC microgrid

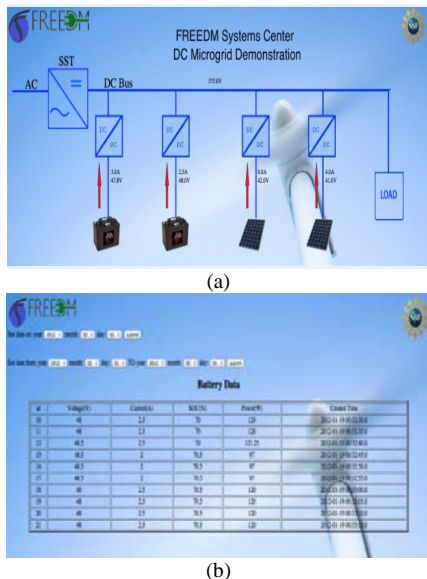


Figure 16. (a) Control center webpage; (b) system database.

Case I: islanding mode to DC source-enabled mode

Experimental results of the transition from islanding mode to DC source-enabled mode are shown in Figure 17.

(a) and Figure 17.(b). Initially the system is in the islanding mode and the DC bus voltage is regulated by the batteries. Based on the Figure 17 (b), the PV panels’ output power is almost equal to the load needed, so the bus voltage is 380V and the average values of batteries output currents are almost zeros. When the system connects to the DC source, there is no obvious change of the DC bus voltage, but the batteries output current have a very small drops because the DC source output voltage has a small oscillation.

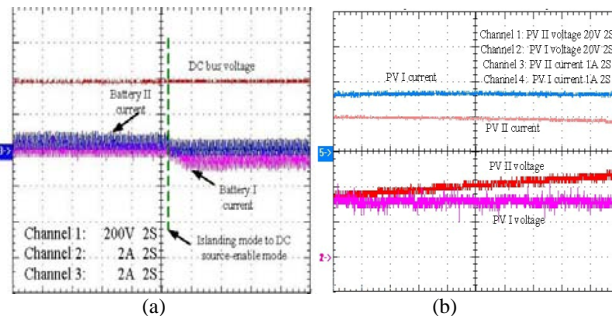


Figure 17. (a) Battery currents and bus voltage; (b) PV currents and voltages

Case II: DC source-enabled mode to islanding mode

Figure 18(a) and Figure 18(b) show the experimental results of the transition from DC source-enabled mode to islanding mode.

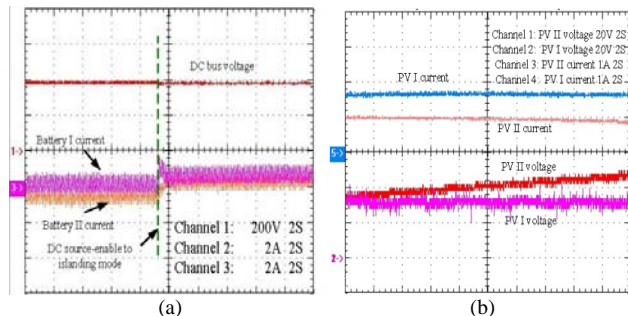


Figure 18. (a) Battery currents and bus voltage; (b) PV currents and voltages

When system is in the DC source-enabled mode, the DC bus voltage is regulated by the DC source. Since the DC source’s output voltage is 380V so the batteries are almost in stand-by status (output current average value is zero). When the system goes into the islanding mode, batteries are responsible to regulate the bus voltage. Since the power generated by PVs is less than the load needed, the DC bus voltage is a little bit smaller than 380V and the batteries output very small current.

V. SOLID STATE FAULT ISOLATION DEVICE

FID is an indispensable part of FREEDM system. The FID must provide ultra-fast isolation to fast restore the system voltage and therefore to minimize the required ride through capability of the system. It requires for a very fast operation (faults clearing within a few μS) in this power electronics based system. In the developed hardware test

bed, the FID is in series with a 12 KV distribution system. Considering the limitation of the available high voltage IGBT (6.5KV rating), the adopted topology consists of three IGBT modules connected in series, with each module containing two emitter-connected 6.5KV, 200A IGBTs together with free-wheeling diodes [14]. To absorb the over voltage caused by high di/dt in the turn-off process, metal oxide varistor (MOV) is adopted shown in Figure 19.

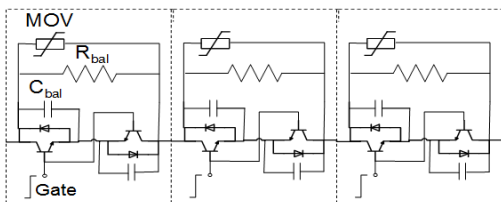


Figure 19. Gen-I FID with series connected IGBT

Test results of the developed FID prototype interrupting a 4A (peak) current in a single phase 7.2KV system is demonstrated in Figure 20. Figure 20 (a) shows the fast turn off process of the current and figure 20 (b) shows the recloser of the FID when the fault is cleared. It is shown that the developed FID can interrupt the fault current in a short time.

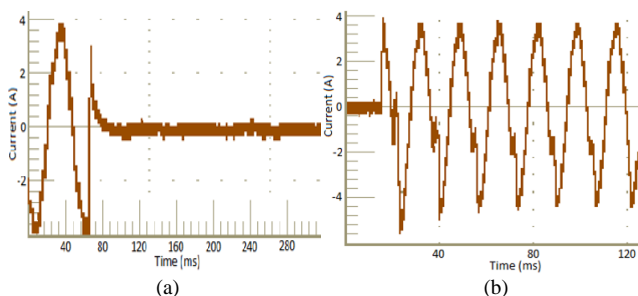


Figure 20. Test results of FID in the single phase 7.2 KV line

The Gen-II FID in FREEDM system will be focused on adoption of SiC power devices, such as SiC Emitter Turn-off Thyristor (ETO), together with hybrid switch concept to future reduce the on-state voltage, and therefore minimize the losses of the FID in the normal operation.

VI. CONCLUSION

This paper presents the promising future power distribution system architecture: the FREEDM system. As a major step towards the envisioned FREEDM system, this paper summarizes the recent development of some key technologies, including distributed grid intelligence, solid state transformer, plug-and-play DC microgrid, and fault isolation device. The proposed FREEDM system is an efficient electric power grid integrating highly distributed and scalable alternative generating sources and storage with existing power systems. Therefore, to facilitate a green and sustainable energy based society, mitigate the growing energy crisis, and reduce the impact of carbon emissions on the environment.

ACKNOWLEDGMENT

This work is supported by the National Science Foundation under the Award Number EEC-0812121.

REFERENCES

- [1] A. Q. Huang., M. L. Crow, G. T. Heydt, J. P. Zheng, and S. J. Dale, "The Future Renewable Electric Energy Delivery and Management system: The Energy Internet," in Proc. IEEE, vol.99, no.1, Jan. 2011, pp. 133-148.
- [2] X.She, A.Q.Huang, S. Lukic, and M. Baran, "On integration of solid state transformer with zonal DC microgrid," IEEE Trans. Smart grid, vol.3, no.2, June 2012, pp.975-985.
- [3] M.L.Crow, B.Mcmillin, W.Y.Wang, and S.Bhattacharya, "Intelligent energy management system of FREEDM system," in Proc.IEEE.PES general meeting, 2010, pp.1-4.
- [4] F.Wang, X.Lu, W.Y.Wang, and A.Q.Huang, "Development of Distributed Grid Intelligence Platform for Solid State Transformer," in Proc.IEEE Smart Grid Comm., 2012, pp.481-485.
- [5] X.Lu, W.Y.Wang, A.Juneja, and A.Dean, "Talk to transformer: An empirical study of device communications for the FREEDM system," in Proc.IEEE.Smart Grid Comm., 2011, pp. 303-308.
- [6] X.Lu, Z.Lu, W.Y.Wang, and J.F.Ma, "On network performance evaluation toward the smart grid: A case study of DNP3 over TCP/IP," in Proc.IEEE. Global Comm., 2011, pp.1-6.
- [7] X.She, R.Burgos, G.Y.Wang, F.Wang, and A.Q.Huang, "Review of solid state transformer in the distribution system: from implementation to filed application," in Proc.IEEE.ECCE, 2012, pp.4077-4084.
- [8] G.Y.Wang, S.Baek, J.Elliott, A.Kadavelugu, F.Wang, X.She, and A.Q. Huang, "Design and Hardware Implementation of Gen-I Silicon Based Solid State Transformer," in Proc.IEEE.APEC. 2011, pp.1344-1349.
- [9] G.Y.Wang, A.Q.Huang, and C.S.Li, "ZVS range extension of 10A 15KV SiC MOSFET based 20KW Dual Active Half Bridge (DHB) DC-DC converter," in Proc.IEEE ECCE 2012, pp. 1533-1539.
- [10] Annual report of Future Renewable Electrical Energy Delivery and Management system center, US, 2012.
- [11] X.W.Yu, F.wang, and A.Q.Huang, "Power management strategy for plug and play DC microgrid," in Proc. IEEE.PES.ISGT., 2012, pp.1-6.
- [12] N. Femia, G. Petrone, G. Spagnuolo and M. Vitelli, "Optimization of Perturb and Observe Maximum Power Point Tracking Method," IEEE Trans. Power Electron., vol. 20, no. 4, 2005, pp. 963-973.