# Built-In Self-Testing Infrastructure and Methodology for an EMG Signal Capture Module

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***Abstract*— Wearable technologies introduce a refinement to personal monitoring by permitting a long-term on-person approach to physiological signals capture. Sensors, textile integration, electronics miniaturization and other technological developments are directly responsible for advancements in this domain; however, in spite of the present progress there are still a number of obstacles to overcome for truly achieving seamless wearable monitoring technology. That concerns, namely, the increase of system's reliability at the design stage, including the adoption of built-in self-test features able to detect functional failures. Biopotential monitoring has been part of medicine and rehabilitation protocols for decades now, thus its integration within wearable systems is a natural progression, however a number of factors can affect acquisition reliability such as, electrode-skin impedance fluctuations and data-acquisition circuits' malfunction. This article presents a built-in self-testing approach for an EMG unit, part of a wearable gait monitoring system. The approach utilizes a mixed-signal test infrastructure managed through a dual purpose digital bus, which serves for communication (I2C) and stimuli propagation.**

***Keywords - BIST; EMG module; electrode-skin impedance; sigma-delta; I2C.***

## I. INTRODUCTION

Until recently, most research involving the capture and analysis of biometric and physiological signals has been limited to a laboratory or otherwise controlled environment, making use of cumbersome and costly equipment, which requires specialized facilities and trained personnel. Such research, although useful in its own right, fails to consider real life scenarios and their impact on the subject. The fast paced developments of body sensor networks (BSN) and wearable technologies (including the so called smart textiles) allowed for the next stage in human behaviour analysis tools, and introduces a new understanding of the interaction of individuals with their surrounding environment [1].

Although, wearable and portable biomedical monitoring devices are rapidly becoming a recognized alternative, little attention has been paid to field testing protocols in order to insure measurement reliability, especially when considering long-term scenarios. Testing and design for testability (DfT) have become a crucial aspect of most electronic designs, moreover considering the structural complexities involved in modern packaging technologies.

During biological signals capture, modules' faults (either catastrophic or parametric) can occur in both sensors and signal conditioning circuitry (SCC). This is even more acute when these modules are integrated within wearable systems, due to the harsh conditions they are subject to. In order to improve wearable systems reliability, built-in testing and calibration functionalities are required, which permit faults detection and diagnosis prior data is erroneously captured.

Although significant advances in the last decades have been made on the development and use of standard test infrastructures for digital circuits, such is not the case for analogue or mixed signal scenarios, in spite of the availability of the IEEE 1149.4 test bus [2] [3]. Nevertheless, a number of *ad hoc* contributions and strategies exist, where the general idea is the evaluation of an analog response to controlled stimuli, in order to verify expected response behavior and correlating deviations to specific faults in certain cases [4] [5].

In contrast, the electrode-skin interface, as well as its effect on biosignals measurements, has been well studied [6] [7] [8]. A number of strategies exist for the electrode-skin impedance characterization [9] [10], but the introduction of new electrodes types (textile and capacitive for example) present novel challenges, especially in the case of electromyographic (EMG) signals acquisition [11]. The traditional approach for insuring quality electrode based bioelectric monitoring is through a thorough skin preparation of the target area, verified with a portable skin-impedance meter or utilizing a test signal of the acquisition system. Methods such as the ones presented in [12] [13] provide a continuos monitoring of electrode-skin interface through the inclusion of additional hardware such as signal generators, current sources, filters, used in parallel with the target signal acquisition components.

This article presents a BIST solution for an EMG module of a wearable system intended for gait analysis. The strategy focuses on resource reutilization and component count minimization, through the reuse of an inter-integrated circuit (I2C) bus as a stimuli/response transport, managed through a novel protocol. Section 2 provides an overview of the wearable acquisition system for gait analysis design on which the present work was based. Section 3 presents the BIST strategies implemented, as well as the management framework. Section 4 summarized the experimental test results, and section 5 states the conclusions of the work.

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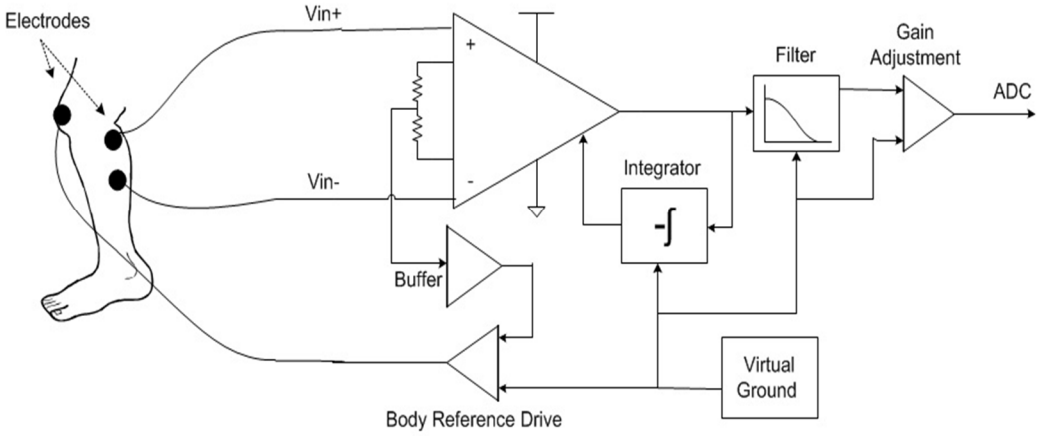


Figure 1. EMG signal conditioning module structure.

## II. WEARABLE DATA ACQUISITION SYSTEM FOR GAIT ANALYSIS

Current instrumentation and methods for gait analysis are still expensive and complex, difficult to setup by healthcare staff, hard to operate and uncomfortable for the patient, while requiring a very high level of expertise for data gathering, analysis and interpretation. A new instrument infrastructure specifically dedicated to capturing locomotion data is being developed [14]. The objective is to produce a patient friendly product, capable of providing reliable data for clinicians. It consists of a legwear with customized textile-embedded sensing electronic devices, interconnected by a wired body sensor network that captures inertial and EMG signals, which sends aggregated information to a personal computer through a wireless link.

### A. EMG Module

The EMG module contained within each sensor node, shown in Figure 1, can be divided in two main sections: the electrodes and the signal conditioning circuitry. The electrodes are sewn directly on the fabric using conductive yarns made of a polymeric filament covered by a very thin layer of silver, and grouped in sets of two acquisition electrodes and a reference electrode. The SCC comprises the following stages: a differential amplifier, drift removal, filtering, gain adjustment, and a body reference drive feedback. These stages have a predictable behavior established by their configuration and/or combination of elements such as resistors and capacitors, which show an acceptable dispersion of values among them, maintaining the proper functioning of the system. However, variations in the components' manufacturing process, different life-time degradations, electrical faults (shorts and open circuits), or environmental issues such as, humidity, pressure or temperature, can alter such balance of values. Therefore, it is important to ensure that the system is operating within the defined limits before and during its usage, in order to insure the reliability of the captured data.

## III. BUILT-IN SELF-TESTING

Built-in self-testing/calibration (BISTC) strategies have traditionally focused on performing detection, diagnosis and repair actions of a specific module, section, component, or IP core [15] [16]. The increasing complexity of modern wearable monitoring technology (WMT) can seldom benefit from strategies that are either too centralized, external data/equipment dependent, or component focused. Communication overhead, increased complexity and resources, or energy expenditure, are just a few factors that limit traditional approaches.

In order to address some of the before mentioned limitations, a BISTC method was proposed, which reduces implementation overhead through the reuse of the I2C bus for testing management purposes, all within a proprietary I2C compliant testing framework named SCPS (setup, capture, process and scan) [17]; making use of the already existing I2C bus for communication purposes, resource management and stimuli-response propagation. Figure 2 illustrates an overview of the infrastructure when applied in an embedded electrodes test instrument.

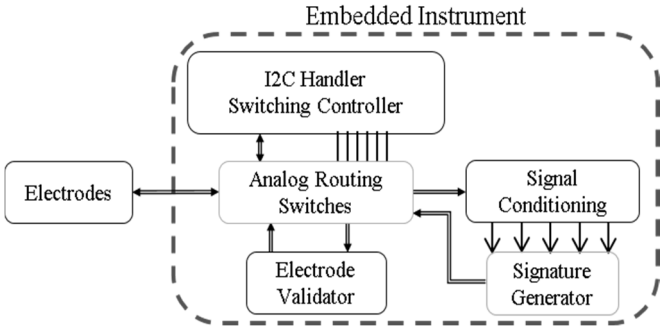


Figure 2. EMG module BISTC structure.

### A. Electrode-skin Verification

Electrodes are probably the most widely used sensors for capturing different biosignals within WMT. The contact impedance achieved in the electrode-skin interface affects

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biosignals measurements (as stated earlier), a matter of concern, traditionally resolved through, namely, skin preparation procedures, equipment checking, and electrode replacement. Even under such controlled conditions, variations of the electrode-skin contact impedance are to be expected. However, in most of the applications, such as athlete's performance and daily activities monitoring, or other scenarios where the individuals will have to position the electrodes themselves or the electrodes are integrated within a garment, careful positioning and skin preparation cannot be guaranteed.

In the case of textile electrodes the problems are exacerbated, due to their sensitivity to pressure, fabric stretching, and motion artifacts [18] [19]. In addition, textile electrodes and wires (Figure 3) are relatively new technologies and strong behavioral models have not been well established (when compared to pre-gel electrodes).

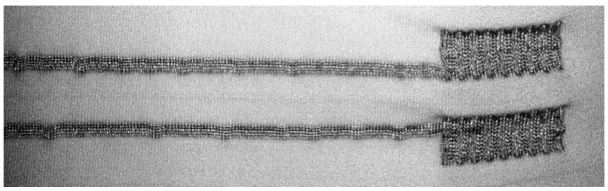

Figure 3. Embedded textile EMG electrodes.

A simple electrode-skin impedance verification circuit was developed following a straight forward approach, by injection of a small current in order to ascertain an electrode pair target load. Individual electrode-skin interface strategies generally utilize a three electrodes approach (one electrode-skin contact target and two others for sinking and voltage reference respectively); however, an electrode pair-wise verification was preferred in this case, in order to maintain approach simplicity. A single supply current to voltage converter is used (Figure 4), which includes a calibration resistor in parallel with the target load in order to control threshold limits and avoid open feedback scenarios. The stimulating current being introduced to the body is a paramount consideration, in order to comply with IEC60601-1 standards, thus the presence of a limiting reference resistor. A local DC reference can be applied as stimulus, in addition to a virtual ground compensated square wave signal sent through the I2C bus.

### *B. Signal condition circuitry verification*

Common-mode rejection, amplification and filtering are regular stages of any electrode based signal conditioning circuit [20]. Such conditioning is performed in order to reduce the effects of common-mode potentials, random noise, motion and power-line artifacts, as well as to effectively retrieving the components of interest of the measured signal. Amplification factors and cut-off frequencies are dependent on the signal type [20], and deviation can cause unwanted elements to be introduced into the conditioned signal.

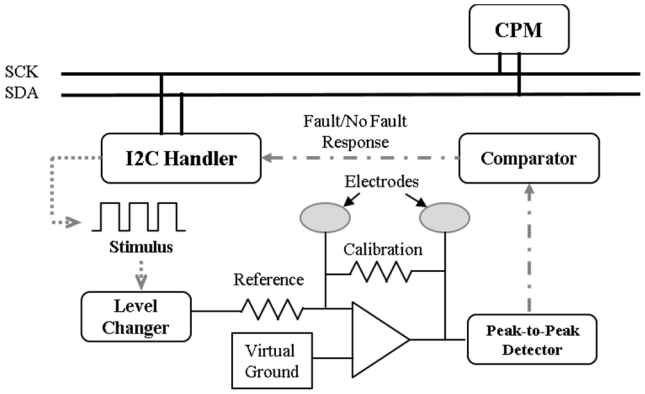


Figure 4. Electrode-skin verification structure.

The test of the SCC is achieved by means of the injection of a square stimulus at the input and the collection of its response in the form of a digital signature that can be compared to a pre-determined golden response. This response actually consists of a set of signatures corresponding to the tolerance determined by acceptable components variations. Initially a Built-In Logic Block Observer (BILBO)-like [21] based approach was attempted in which the stimulus was provided by an LFSR (Linear Feedback Shift Register), and the response of the SCC was collected by a Multiple Input Signature Register (MISR). However, such solution proved to be ineffective, since large variations of some components of the SCC module rendered signatures not so different from those considered valid values, thus providing unreliable and ambiguous error detecting methods for this specific purpose.

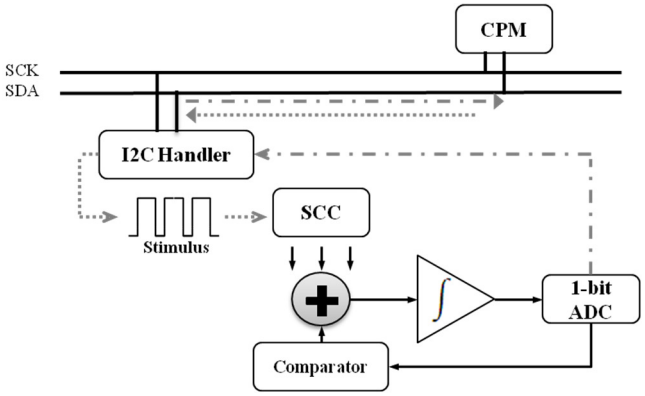


Figure 5. SCC test infrastructure.

Alternatively, a different testing approach was attempted, relying on the I2C Bus for stimuli generation and response capture purposes (Figure 5). An I2C Bus driven stimulus was preferred over a locally generated one, in order to reduce local sources of noise (such as clocks), gain increased stimulus shaped flexibility, and reuse of existing resources. The SCC is tested after capturing its transient response to an impulse designed in order to stimulate the

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SCC frequency bandwidth and amplitude full range. This transient, as well as that observed in another internal node of the SCC are then converted to a single digital bit stream by means of a delta-sigma modulator. The observation of different analog nodes and their compression in a single bit stream improves observability and saves test response resources and time. This way the need for an analog test bus line, the inclusion of a complex analogue to digital converter and the multiplexing test response acquisition are avoided.

In order to reduce noise along the communication lines, complexity and total area of the test circuit, it was decided to differ from traditional delta-sigma modulators, by eliminating the flip-flops generally present between comparators. The resulting signature is transported through the I2C lines to a local processing module, which applies a Ziv-Lempel based lossless compression algorithm [22]. This algorithm replaces repetitive bit sequences by a shorter code, as described in the following pseudo-code:

```
array = ΣΔ output
foreach segment from array
   if segment ∈ dictionary
      then signature + = segment
foreach segment from signature
   if segment ∈ 2nd dictionary
      then final signature += segment
```

Figure 6. Pseudo-code for compression algorithm.

The use of this compression algorithm is twofold. In the one hand, compression allows reducing the length of data to be transmitted along the wired network from the sensor node to the central processing module (CPM), thus reducing communication time and power, and on the other hand it permits for the analog response external recovery, using the corresponding decompressing algorithm.

### C. SCPS and the I2C Handler

A testing and/or calibration strategy for WMT benefits from a group or multi-sensor approach. Such approach could seek to maintain data reliability through recognition of deviating degradation patterns on sensors that could provide insight into system problems due to improper sensor positioning, induced electrical effects due to movement (turboelectric and piezoelectric effects), structural flaws and other factors that require the coverage provided by a group and/or multi-sensor approach. In order to manage the previously mentioned approach a testing framework was designed based on a protocol named SCPS. The SCPS protocol seeks to standardize the command sequence for sensor acquisition/testing access. An I2C based implementation was designed with broadcast, multicast and unicast commands set in order to address modules as groups.

In the present case the command set is utilized for routing elements configuration, and in the case of on-the-fly stimuli configurability, a sequence compatible with I2C communication is used for transporting stimuli and responses to and from the target module as described in Figure 7.

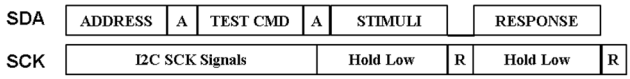


Figure 7. I2C compatible sequence for Stimulus/Response transport.

The sequence sets up the appropriate routing configuration through acknowledgement of a test command and uses the next two SCK low from stimulus and response transport. In order to avoid start/stop events from occurring, the master element insures a low state of the SDA prior to SCK high. A re-start or stop event can then be used at the event of the sequence to finalize the action.

## IV. RESULTS

The electrode verification circuit was simulated on Multisim 11.0.775 with database version 11.0.b. Preliminary experiments were performed on an Agar based gel for performance verification prior to testing on human volunteers. A number of signals were used for behavior confirmation, as can be seen in Figure 8, Figure 9, and Figure 10.

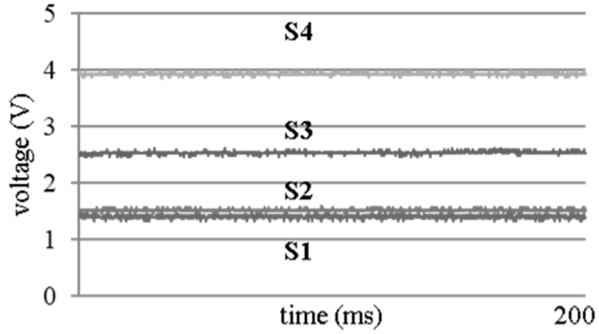


Figure 8. DC Stimuli response for varying conditions, where S1 is the stimuli, S2 is low impedance response, S3 is an expected impedance response and S4 is a high impedance response.

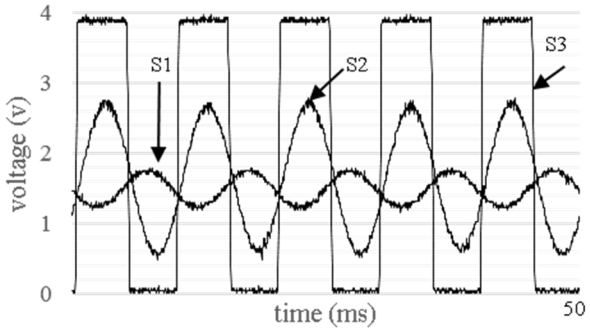


Figure 9. Sine wave of 100 Hz stimuli response for varying conditions, where S1 is the stimuli, S2 is a normal impedance response and S3 is a high impedance response.

The electrode-skin impedance was controlled through variations of the contact surface between the electrode and the skin. Figure 8 presents the behaviour response of the

circuit to such variations for a 10 µA DC stimulus, proving its compatibility with a threshold fault determination approach. Figure 9 and Figure 10 present corresponding responses to a sinewave and squarewave stimuli of matching peak to peak amplitude, respectively (limited to 50 µA). Such responses reveal their sensitivity to the reactive component of the electrode-skin impedance (through phase and time response effects).

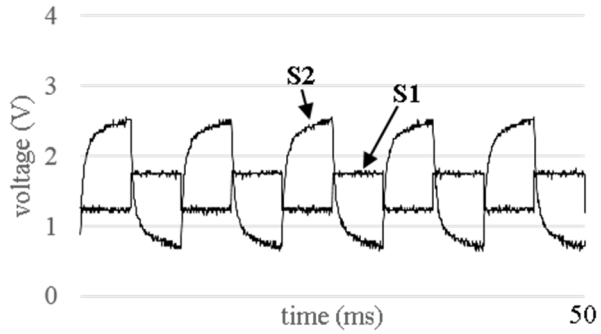


Figure 10. Square wave of 100 Hz stimuli, where S1 is the stimuli, and S2 is an expected impedance response.

### A. *Signature generation results*

The SCC and the delta-sigma circuits were simulated within a SPICE like simulator, using manufacturers' models for the operational amplifiers, comparators and analog switches. Figures 11 to 14 show the waveforms obtained in response to an impulse, for golden and faulty cases. The input pulse stimulus was designed considering the circuit time constants and the I2C time specifications – I2C's fast-mode and fast-mode plus specifications impose minimum durations of 0.6 and 0.26 µs high periods, respectively [23].

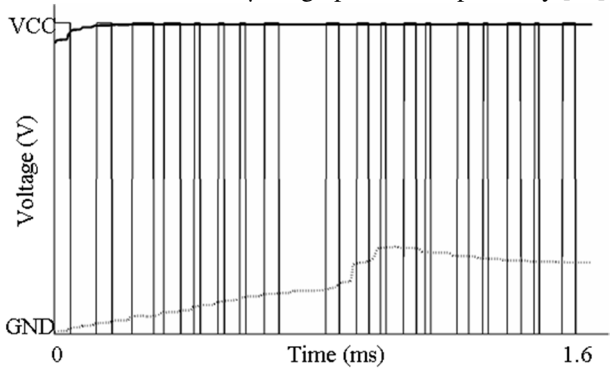


Figure 11. SCC golden response; SCC output (—), internal node (…), sigma-delta output (pulses).

Figures 12, 13 and 14 present faulty responses in the cases of, respectively: a 5% reduction of the filter's gain, a 30% reduction of the low-pass filter's capacitor, and an open connection at the instrumentation amplifier's gain. The sequences of pulses presented in each case are the corresponding outputs of the delta-sigma modulator. It can be seen that, after comparing these sequences with the golden case, the three faults are detectable. The comparison is actually done after capturing them with the I2C controlled infrastructure. This direct capture is possible because the I2C sampling frequency allows doing it with an adequate resolution, i.e., no pulses are lost.

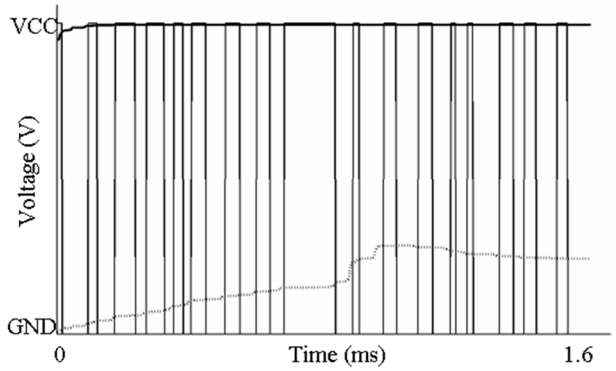


Figure 12. 5% reduction of filter's gain; SCC output (—), internal node (…), sigma-delta output (pulses).

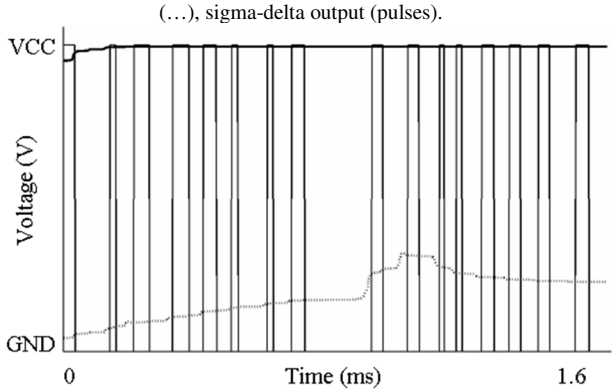


Figure 13. 30% reduction of low-pass-filter´s capacitor; SCC output (—), internal node (…), sigma-delta output (pulses).

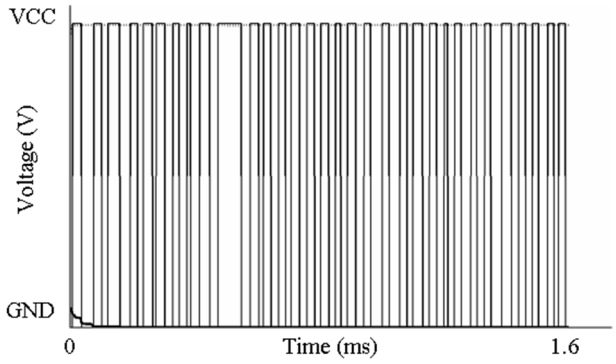


Figure 14. Open connection in instrumentation amplifier's output; SCC output (—), internal node (…), sigma-delta output (pulses).

The bit-stream that is then obtained presents duration of 1.4 ms, or a length of 140 bits. The Ziv-Lempel compression implemented in the local processing unit allows reducing this length in order to transmit a shorter number of bits.

## V. CONCLUSION

A mixed-signal built-in self-test infrastructure and methodology is presented that covers the need to address the in-situ verification of the electrode-skin interface, as well as

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the functional response of the associated signal conditioning circuitry, for a EMG module of a wearable data acquisition system for gait analysis purposes. The approach being proposed uses an I2C bus for test event management, as well as, stimuli/response transport through a protocol meant for resource optimization and sensor group testing strategies. The electrode-skin interface is evaluated after the measure of the differential impedance and the signal conditioning circuitry is tested after comparing its pulse response with the expected golden response. A Ziv-Lempel compression algorithm is used to allow transferring a shorter version of the captured bit stream, thus saving communication time and power, while preserving the possibility of reconstructing the circuit's pulse response. The simulations and circuit implementation results confirm the validation of the approaches being proposed and reveal their compatibility to the target system and available resources. Significance

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