

Sequential Symbol Synchronizers based on Pulse Comparison at Quarter Rate

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Abstract- This work presents the synchronizer based on pulse comparison, between variable and fixed pulses. This synchronizer has two variants, one operating by both transitions at the bit rate and other operating by both transitions at quarter rate. Each variant has two versions which are the manual and the automatic. The objective is to study the four synchronizers and evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal Noise Ratio).

Keywords - Prefilter; Synchronizers; Communication systems.

I. INTRODUCTION

This work studies the sequential symbol synchronizer, with a phase comparator based on a pulse comparison, between a variable pulse P_v and a fixed reference pulse P_f .

The synchronizer has four types supported in two variants, one operating by both transitions at rate and other operating by both transitions at quarter rate. The variant at the rate has two versions namely the manual (b-m) and the automatic (b-a). The variant at quarter rate has also two versions, namely the manual (b-m/4) and the automatic (b-a/4) [1, 2, 3, 4, 5].

The difference between them is only in the phase comparator since the other blocks are equal [6, 7, 8].

The error pulse P_e ($P_v - P_f$) controls the VCO (Voltage Controlled Oscillator) to synchronize with the input data.

The variable pulse P_v is common to manual and automatic versions but the fixed pulse P_f is different [9, 10].

The VCO output is the clock, with good quality, that samples the input data at the maximum opening eye diagram and retimes its bit duration [11, 12].

Fig. 1 shows the blocks diagram of the synchronizer.

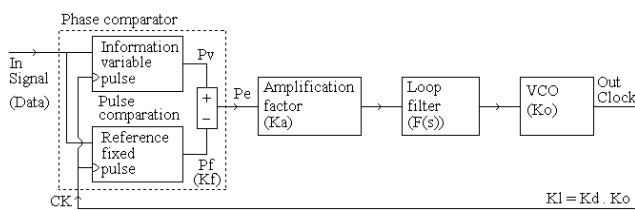


Fig. 1 Synchronizer based on pulse comparison

K_f is the phase comparator gain, $F(s)$ is the loop filter, K_o is the VCO gain and K_a is the loop amplification factor that controls the root locus and then the loop characteristics.

Following, we present the variant at bit rate with their manual and automatic versions. Next, we present the variant at the half bit rate with their manual and automatic versions.

After, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

II. STATE OF THE ART, PROBLEM AND SOLUTION

In priori and actual-art state, were developed various synchronizers operating, initially, at the bit rate. After, we developed synchronizers operating at half rate. Now, we present synchronizers operating at a quarter rate. This contribution increases the know-how about synchronizers.

Our motivation is to create new synchronizers and evaluate their performance. The problem is that the synchronizers have speed limitations. One solution proposes internal low frequency operation, but external high speed rate [1, 2, 3, 4].

III. SYNCHRONIZERS OPERATING AT THE RATE

The synchronizer with its VCO operates, here, at the data transmission rate.

This variant has the manual and the automatic versions, the difference is only in the phase comparator. The variable pulse P_v consists of first flip flop with exor and is equal in the two versions, but the fixed pulse P_f is different [1, 2].

A. Operation at the rate and manual version

The manual version has a phase comparator, where the fixed pulse P_f is produced by an exor with a delay $\Delta t = T/2$, that needs a previous manual adjustment (Fig. 2)

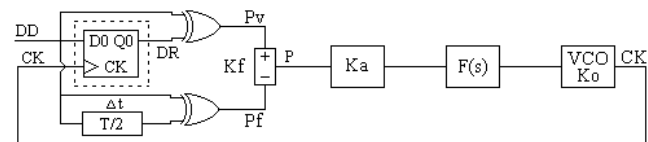


Fig. 2 Synchronizer at the rate and manual (b-m)

The variable pulse P_v minus the fixed pulse P_f ($P_v - P_f$) determines the error phase that controls the VCO.

Fig. 3 shows the waveforms of the synchronizer operating at the rate and manual version.

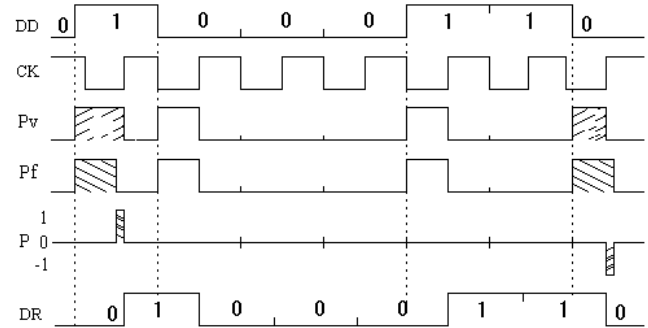


Fig. 3 Waveforms of the synchronizer at the rate and manual

The error pulse P_e diminishes and disappear at the equilibrium point.

B. Operation at the rate and automatic version

The automatic version has a phase comparator where the fixed pulse Pf is produced automatically by the second flip flop with exor, without previous adjustment (Fig. 4).

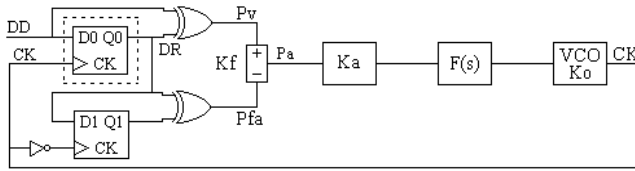


Fig. 4 Synchronizer at the rate and automatic (b-a)

The variable pulse Pv minus the fixed pulse Pf (Pv-Pf) determines the error phase that controls the VCO.

Fig. 5 shows the waveforms of the synchronizer operating at the rate and automatic version.

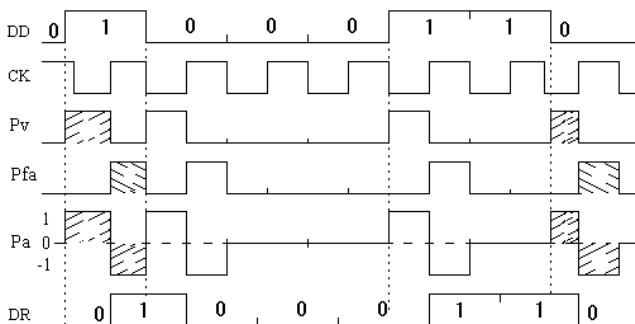


Fig. 5 Waveforms of the synchronizer at the rate and automatic

The error pulse Pe don't disappear, but the variable area Pv is equal to the fixed one Pf at the equilibrium point.

IV. SYNCHRONIZERS OPERATING AT QUARTER RATE

The synchronizer with its phase comparator operates, here, by both transitions at quarter data transmission rate.

This variant has the manual (b-m/4) and the automatic (b-a/4) versions, the difference is only in the phase comparator. The variable pulse Pv, based in the four first flip flops with multiplexer and exor, is equal in the two versions, but the fixed pulse Pf is produced from a different way [3, 4].

A. Operation at quarter rate and manual version

The manual version has a phase comparator, where the fixed pulse Pf is produced by an exor with a delay $\Delta t = T/2$, that needs a previous manual adjustment (Fig. 6).

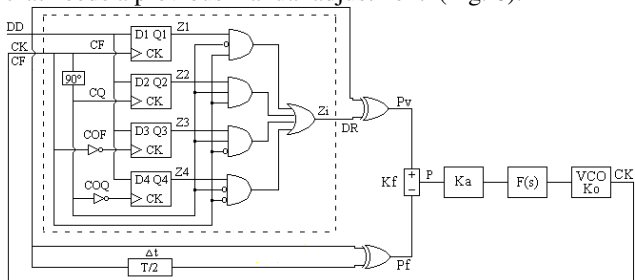


Fig. 6 Synchronizer at quarter rate and manual (b-m/4)

The variable pulse Pv minus the fixed pulse Pf (Pv-Pf) determines the error phase that controls the VCO.

Fig. 7 shows the waveforms of the synchronizer operating at quarter rate and manual version.

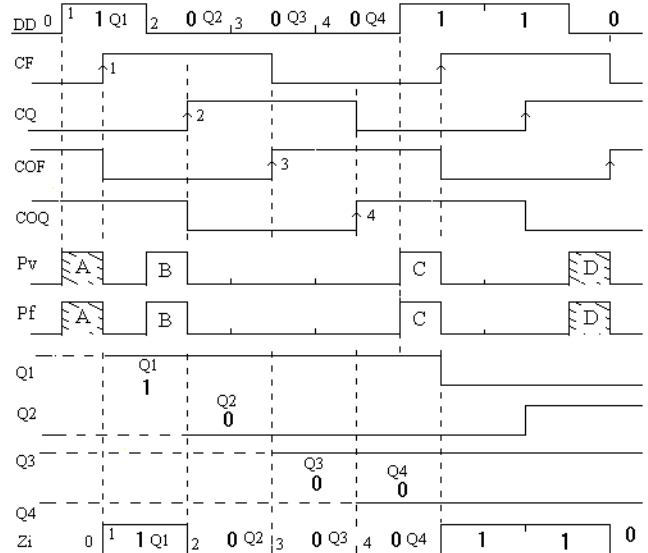


Fig. 7 Waveforms of the synchronizer at quarter rate and manual

The error pulse Pe diminishes and disappear at the equilibrium point

B. Operation at quarter rate and automatic version

The automatic version has a phase comparator, where the fixed pulse Pf is produced automatically by the seconds flip flops and multiplexer with exor, without previous adjustment (Fig. 8).

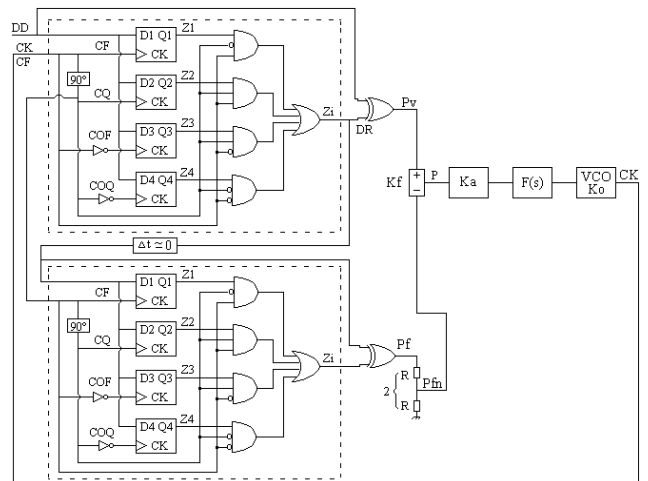


Fig. 8 Synchronizer at quarter rate and automatic (b-a/4)

The variable pulse Pv minus the fixed pulse Pf (Pv-Pf) determines the error phase that controls the VCO.

Fig. 9 shows the waveforms of the synchronizer at quarter rate and automatic version.

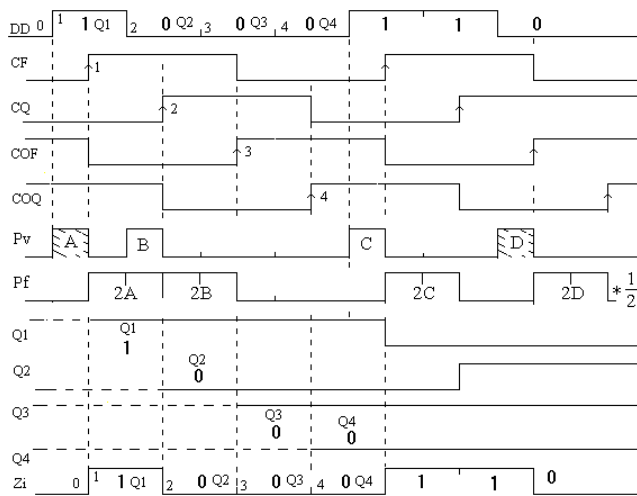


Fig. 9 Waveforms of the synchronizer at quarter rate and automatic

The error pulse P_e don't disappear but the positive area P_v is equal to the negative P_f at the equilibrium point.

V. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [5].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is $Kl=Kd.Ko=Ka.Kf.Ko$ where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplifier factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate $t_x=1$ baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is $f_{CK}=1$ Hz.

We choose a normalized external noise bandwidth $B_n = 5$ Hz and a normalized loop noise bandwidth $B_l = 0.02$ Hz. Later, we can disnormalize these values to the appropriated transmission rate t_x .

Now, we will apply a signal with noise ratio SNR given by the signal amplitude A_{ef} , noise spectral density N_o and external noise bandwidth B_n , so the $SNR = A_{ef}^2/(N_o.B_n)$. But, N_o can be related with the noise variance σ_n and inverse sampling $\Delta\tau=1/Samp$, then $N_o=2\sigma_n^2.\Delta\tau$, so $SNR=A_{ef}^2/(2\sigma_n^2.\Delta\tau.B_n) = 0.5^2/(2\sigma_n^2*10^{-3}*5) = 25/\sigma_n^2$.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter $F(s)=1$ with cutoff frequency 0.5 Hz ($B_p=0.5$ Hz is 25 times bigger than $B_l=0.02$ Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s) = \frac{G(s)}{1+G(s)} = \frac{KdKoF(s)}{s+KdKoF(s)} = \frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$B_l = \frac{KdKo}{4} = Ka \frac{KfKo}{4} = 0.02\text{Hz} \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is

$$B_l=0.02=(Ka.Kf.Ko)/4 \text{ with } (K_m=1, A=1/2, B=1/2; K_o=2\pi) \\ (Ka.K_m.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2/\pi \quad (3)$$

For the hybrid synchronizers, the loop bandwidth is

$$B_l=0.02=(Ka.Kf.Ko)/4 \text{ with } (K_m=1, A=1/2, B=0.45; K_o=2\pi) \\ (Ka.K_m.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2.2/\pi \quad (4)$$

For the combinational synchronizers, the loop bandwidth is

$$B_l=0.02=(Ka.Kf.Ko)/4 \text{ with } (K_f=1/\pi; K_o=2\pi) \\ (Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.04 \quad (5)$$

For the sequential synchronizers, the loop bandwidth is

$$B_l=0.02=(Ka.Kf.Ko)/4 \text{ with } (K_f=1/2\pi; K_o=2\pi) \\ (Ka*1/2\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.08 \quad (6)$$

The jitter depends on the RMS signal A_{ef} , on the power spectral density N_o and on the loop noise bandwidth B_l .

For analog PLL the jitter is

$$\sigma_{\phi}^2 = B_l.N_o/A_{ef}^2 = B_l.2.\sigma_n^2.\Delta\tau = 0.02*10^{-3}*2\sigma_n^2/0.5^2 = 16*10^{-5}.\sigma_n^2$$

For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

The following figure (Fig. 10) shows the setup that was used to test the various synchronizers.

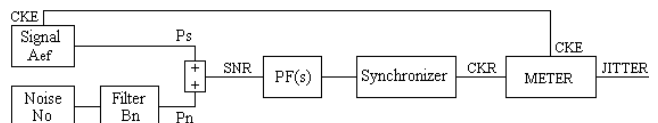


Fig. 10 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig. 11).

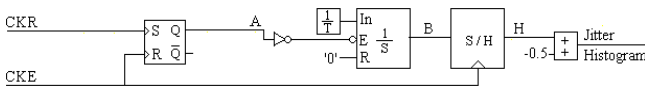


Fig. 11 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present the four synchronizer results in terms of output jitter UIRMS versus input SNR.

Fig. 12 shows the jitter-SNR curves of the four synchronizers with both transitions, at rate manual version (b-m), at rate automatic version (b-a), at quarter rate manual version (b-m/4) and at quarter rate automatic version (b-a/4).

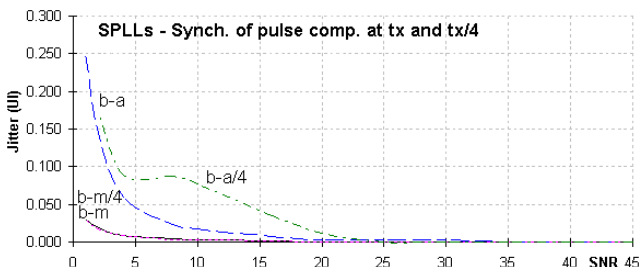


Fig. 12 Jitter-SNR curves of the 4 synchronizers(b-m,b-a,b-m/4,b-a/4)

We see that, in general, the output jitter UIRMS decreases gradually with the input SNR increasing. However, the both quarter rate automatic (b-a/4) has some irregularities.

For high SNR, the four synchronizer jitter curves tend to be similar. However, for low SNR, the manual versions (b-m, b-m/4) are significantly better than the automatic versions (b-a, b-a/4), the both transition at rate manual (b-m) is slightly the best. Also, for an intermediate SNR (SNR≅10), the both transitions quarter rate automatic (b-a/4) has a significant jitter perturbation, due to some losses of synchronism.

V. CONCLUSION AND FUTURE WORK

We studied four synchronizers using both transitions, with two variants, one operating at the rate that has two versions namely the manual (b-m) and the automatic (b-a) and other variant operating at quarter rate that has also two versions namely the manual (b-m/4) and the automatic (b-a/4). Then, we tested their jitter - noise curves.

We observed that, in general, the output jitter curves decreases gradually with the input SNR increasing. However, the quarter rate automatic (b-a/4) has some irregularities.

We verified that, for high SNR, the four synchronizers jitter curves tend to be similar, this is comprehensible since the synchronizers are digital and have similar noise margin.

However, for low SNR, the manual versions (b-m, b-m/4) are significantly better than the automatic versions (b-a, b-a/4), this is comprehensible since the automatic versions have more digital states than the manual versions, then the error state propagation effects is aggravated.

The version at rate manual (b-m) is slightly the best because has less digital states. On the other hand, the version at quarter rate automatic (b-a/4) has a significant jitter perturbation (SNR≅10) due to some losses of synchronism.

In the future, we are planning to extend the present study to other types of synchronizers.

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REFERENCES

- [1] Jean C. Imbeaux, "performance of the delay-line multiplier circuit for clock and carrier synchronization in Digital Satellite Communications". IEEE Journal on Selected Areas in Communications pp.82-95 Jan. 1983.
- [2] Werner Rosenkranz, "Phase Locked Loops with limiter phase detectors in the presence of noise", IEEE Transactions on Communications com-30 N°10 pp.2297-2304. Oct 1982.
- [3] Hans H. Witte, "A Simple Clock Extraction Circuit Using a Self Sustaining Monostable Multivibrator Output Signal", Electronics Letters, Vol.19, Is.21, pp.897-898, Oct 1983.
- [4] Charles R. Hogge, "A Self Correcting Clock Recovery Circuit", IEEE Transactions on Electron Devices pp.2704-2706 Dec 1985.
- [5] Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro and Jose P. Carvalho "A New Technique to Measure the Jitter", Proc. III Conf. on Telecommunications pp.64-67 Ffoz-PT 23-24 Apr 2001.
- [6] Marvin K. Simon and William C. Lindsey, "Tracking Performance of Symbol Synchronizers for Manchester Coded Data", IEEE Transactions on Communications Vol. com-2.5 N°4, pp.393-408, April 1977.
- [7] Jeffrey B. Carruthers, D. D. Falconer, H. M. Sandler and L. Strawczynski, "Bit Synchronization in the Presence of Co-Channel Interference", Proc. Conf. on Electrical and Computer Engineering pp.4.1.1-4.1.7, Ottawa-CA 3-6 Sep. 1990.
- [8] Johannes Huber and Weilin Liu "Data-Aided Synchronization of Coherent CPM-Receiver" IEEE Transactions on Communications Vol.40 N°1, pp.178-189, Jan. 1992.
- [9] Antonio A. D'Amico, Aldo N. D'Andrea and Ruggero Reggianni, "Efficient Non-Data-Aided Carrier and Clock Recovery for Satellite DVB at Very Low SNR", IEEE Jou. on Sattelite Areas in Comm. Vol.19 N°12 pp.2320-2330, Dec. 2001.
- [10] Rostislav Dobkin, Ran Ginosar and Christos P. Sotiriou "Data Synchronization Issues in GALS SoCs", Proc. 10th International Symposium on Asynchronous Circuits and Systems, pp.CD-Ed., Crete-Greece 19-23 Apr. 2004.
- [11] N. Noels, H. Steendam and M. Moeneclaey, "Effectiveness Study of Code-Aided and Non-Code-Aided ML-Based Feedback Phase Synchronizers", Proc. IEEE Intern. Conference on Communications (ICC'06) pp.2946-2951, Istambul-TK, 11-15 Jun 2006.
- [12] Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro and Jose P. Carvalho "Effects of the Prefilter Type on Digital Symbol Synchronizers", Proc. VII Symposium on Enabling Optical Network and Sensors (SEONs 2009) pp.35-36, Lisbon-PT 26-26 June 2009.