Power Consumption of Packet Processing Engines and Interfaces of Edge Router: Measurements and Modeling

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***Abstract*—Power management is a key feature in today's Internet Protocol/ Multi-Protocol Label Switching (IP/MPLS) network across all market segments. With the aim of controlling the power consumption in core networks, we consider energy aware devices that are able to reduce their energy requirements by adapting their performance. We focus on packet processing engines, and router interfaces, which generally represent the most energy consumption components of network devices data plane. Our goal is to control both the power configuration of pipelines, as well as to study the effect of the packet size onto the power consumption of an edge router. The results show that the packet size is closely related to the power consumption of the edge router. It is also shown that there is a tradeoff between power consumption and packet latency times. Based on these results, we model the formal power consumption equation of the edge router.**

Keywords-power consumption; green networking; packet processing engine; packet size; edge router; interface power; packet processing power.

I. INTRODUCTION

By the continuous growth of customers, broadband access, and number of services being offered by telecom operators and Internet Service Providers (ISPs), the energy efficiency issue has become a high priority objective, and a significant concern for network infrastructure and next-generation network devices. The rapid growth of traffic has resulted in a related increase in energy consumption. ISPs, and telecom operators reported alarming statistics of network energy requirements and of the related carbon footprint [1]. The Global e-Sustainability Initiative (GeSI) estimated the overall carbon footprint of European network devices and infrastructure to be about 349 MtCO2e (Million Metric Tons of Carbon) in 2020, with a 131% increase with respect to 2007 if no green network technologies (GNTs) would be adopted [2]. In order to support this rapid increase in energy consumption, ISPs need a larger number of devices with architectures able to perform more complex operations in a scalable way. The majority of current network devices operate at their maximum capacity and have a constant power consumption independent of the actual traffic load, and thus the most of the energy consumed in networks is wasted. It is well known that network links and devices are generally provisioned for busy or rush-hour load, which typically exceeds their average utilization by a wide margin [3]. Although this margin is seldom reached, network devices are designed on its basis so their power consumption remains more or less constant even in the presence of fluctuating traffic load.

The data plane certainly represents the most energy consuming and critical element in the largest part of network device architectures since it is generally composed by special purpose hardware (HW) elements (packet processing engines, network interfaces, etc.) that have to perform per-packet forwarding operations at very high speeds. Certain studies estimated that the power required at the data plane weighs for 54% on the overall device architectures, versus 11% for the control plane and 35% for power and heat management. Internal packet processing engines require about 60% of the power consumption at the data plane of a high end router, network interfaces weigh for 13%, switching fabric for 18.5%, and buffer management for 8.5 [4][5]. Starting from these data, we decided to focus on the power consumption of packet processing engines and the power consumption of the router interface trying to study the effect of the packet size variation onto the power consumption of an edge router. After that, we analyze the measurement results from numerous cases and show that the packet size is closely related to the power consumption of the edge router. Through the analysis, it is possible to draw a power consumption function of the edge router against the packet size.

In this paper, our main objective is to consolidate two factors of power consumption (packet processing engines and router interfaces) and find a closed relation between them, and provide an analytical model able to capture the trade-off between energy consumption and network performance (delay) by controlling the power state configurations according to the actual traffic load to minimize the power consumption while meeting the performance constraints.

The paper is organized as follows. Section II introduces literature review and related work. Then we describe the power consumption of the packet processing engines in section III, and the power consumption of the router interface in section IV. Section V shows the analytical model, while measurements

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and analysis are shown in section VI. Finally, the conclusions are in section VII.

II. LITERATURE REVIEW AND RELATED WORK

Most of the approaches that study the power consumption of data plane of the edge router are directed to study the effect of one separate factor from the previous discussed aspects in section I, and show the effect of it on the total power consumption of the data plane, assuming no variation for the other factors. Bolla et al. [6] provide an up-to-date survey on the current state-of-the-art in energy efficiency for fixed telecommunication networks, and improvements that can be introduced in today's networking equipment. Bolla et al. [7] aimed at studying the power consumption of packet processing engines by proposing an analytical model able to capture the impact of power management of the packet processing engines, and tried to optimize it by dynamic adaptation of network device resources. Ahn et al. [8] provide measurement of the power consumption of a router interface and draw an analytical model against the packet sizes. Nedevschi et al. [3] present the design of two forms of power management schemes, that reduce the energy consumption of network. The first form is based on putting network components to sleep during idle times, reducing energy consumed in the absence of packets. The second form is based on adapting the rate of network operation to the offered workload, reducing the energy consumed when actively processing packets. Zouaoui et al. [9] achieve to adapt the router queue-length by dynamic buffer management in such a way, that reduced the energy. In this paper, our objective is to consolidate two merged factors of power consumption (packet processing engines and router interfaces) and find a closed relation between them to study the best suitable power configuration of pipelines in both high traffic volume (rush hours) and low traffic volume, and achieve the best way to optimize the tradeoff between energy consumption and network performance indexes (delay) using different packet sizes. By merging both contributions [7][8], we proposed an analytical model able to capture the impact of packet size on the link utilization factor and the packet processing capacity, which will affect the power consumption of packet processing inside the data plane. The obtained results show that for low traffic volumes, it is recommended to use a power state corresponds to the minimization of energy consumption constrained to low packet latency with high packet size. For high traffic volumes, it is recommended to use power state corresponds to the maximization of energy consumption constrained to low packet latency with high packet size.

III. POWER CONSUMPTION OF PACKET PROCESSING ENGINES

In order to reduce the energy requirements of the packet processing engine, there are two basic techniques. Firstly, Adaptive rate (AR) that allows dynamically modulating the capacity of a processing engine (or single pipeline) in order to meet traffic loads and service requirements. Secondly, Low power idle (LPI) that forces processing engines to enter low-power states when not sending/processing packets. As previously evaluated and sketched in preliminary studies [6][7], LPI and AR have different impacts on packet forwarding performance. Figure 1 illustrates the effect of AR and LPI on packet forwarding performance. We can tune AR and LPI mechanisms for each parallel pipeline (interaction between AR and LPI). Figure 1(c) shows how AR causes a stretching of packet service times, while the sole adoption of LPI Figure 1(b) introduces an additional delay in packet service, due to the wake-up times.

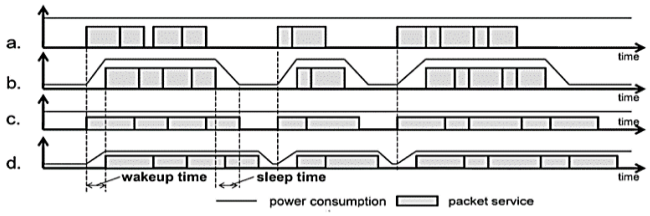

Figure 1. Packet service times and power consumptions in the cases with (a) no power- ware optimizations, (b) only LPI, (c) only AR, and (d) AR and LPI [6][7].

As sketched LPI and AR have different impacts on packet forwarding performance. AR causes a stretching of packet service times, while LPI introduces an additional delay in packet service, due to the wake-up times. Our goal is to dynamically manage the engine configuration in order to balance its energy consumption with respect to its network performance. Now, we will introduce the Advanced Configuration and Power Interface (ACPI) specification and how it makes AR and LPI capabilities accessible. In general computing systems, the ACPI specification provides an open standard for device configuration and power management by the operating system. This standard models the AR and LPI functionalities by introducing two sets of energy-aware states, (P) performance and (C) power states. Regarding the C-States, C_0 indicates the operating state where the central processing unit (CPU) executes instructions, while C_1 to C_x is processor LPI states. As (X) value becomes higher, less power is consumed, because the pipeline will be in sleeping state. But the transition between active and sleeping states requires longer time and more power consumption during transition process. i.e., C_0 is active mode and C ($_{1...\ X}$) are sleep modes. In particular, C_1 is a state where the processor is not executing instructions, but can return to the C_0 state essentially instantaneously. All processors must support this power states. The number of LPI states is considered optional excluding C_0. In addition, the transition times and the power consumption compared to C_0 depend on the specific platform implementation [7]. Regarding the P-states, they allow modifying the operating energy of a processor by altering the working frequency or voltage. So by using P-states, processor can consume different amounts of power while providing different processing performance at the C_0 state. P_0 is the highest performance state with P_1 to P_Y being successive lower performance [7]. The higher index of P and C, the less power will be consumed. Transition between different P-states is generally very slow with respect to packet processing times.

IV. POWER CONSUMPTION OF ROUTER INTERFACE

We begin our investigation of power consumption of the router interface caused by packet sizes with the increment of link utilization. We analyze the power consumption of router interfaces with each L2 frame size 64, 256, 512, and 1518 bytes as the increase of the link utilization. We empirically found that the power consumption of the router interface is directly proportional to the link utilization, as well as reverse

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proportional with the packet sizes. The power consumption increases dramatically when the traffic with 64 bytes L2 frame size [8]. The power consumption of the router interface increases more than 5 watts and this value can't be ignored because a router which has n interfaces consumes more than 5n watts caused by just router interfaces. It is because the router utilizes electricity for processing packets pass through the router. The more the frames passing through the router; the more the power used in the router [8].

V. ANALYTICAL MODEL

In this section, a relation between the packet size, the packet processing power and interface power is proposed in our study based on the adaption of two models presented in [7][8]. The case of single pipeline is chosen in this research. For simplicity, we adopt the ACPI representation of power management primitives and refer to AR and LPI configurations in terms of P and C states. Most of the previous studies presented in the literature didn't take into account the relation between the internal packet processing power and router interfaces power. There are some researches to measure power consumption of packet processing engines. We adopted the model in [7], because the model evaluation shows an acceptable accuracy. Service rate μ represents the device capacity in terms of packet headers that can be processed per second. Moreover, we assume all packet headers requiring a constant service time. The selection of different P and C states is supposed to impact on the forwarding engine performance in terms of both packet service capacity and wake-up times of the servers. The model notation is introduced in Table I. The overall power equation for packet processing driven in [7] is illustrated in (1)

$$\tilde{\phi} = \left[1 + \frac{(\rho - 1)\,(1 + \lambda\,\tau_{on})}{1 + \beta\,\lambda\,\tau_s}\right]\phi_a + \frac{\lambda\,(1-\rho)\,\tau_{on}}{1 + \beta\,\lambda\,\tau_s}\phi_t + \frac{1-\rho}{1 + \beta\lambda\,\tau_s}\phi_{idle} \quad (1)$$

The average packet delay (latency) is defined as the average waiting time of the packet inside the processing engine and can be calculated according to [7] as in (2)

$$\bar{W} = \frac{\bar{L}}{\lambda\,\beta} = \frac{2\tau_s + \lambda\beta{\tau_s}^2 - \frac{1}{\lambda} + \frac{1}{\lambda\beta}\sum_{j=1}^{j_{max}} \beta_j\, j^2}{2(1 + \lambda\beta\tau_s)} + \frac{\rho^2 - \beta + \sum_{j=1}^{j_{max}} \beta_j\, j^2}{2\,\lambda\beta(1-\rho)} \quad (2)$$

In addition, as stated in [8], the power consumption of the router interface is directly proportional to the link utilization, as well as reverse proportional with the packet sizes. So, the power consumption of a router interface can be defined as the following equation:

$$P_{interface} = \left(E_{HP}\frac{\rho \times R}{s}\right) + E_{PT} \times \rho \times R = \rho \times R\left(\frac{E_{HP}}{s} + E_{PT}\right) \quad (3)$$

In order to obtain the total power consumption of the router, we will consider the switching fabric power and buffer management power are constants. The packet processing power and the interface power are presented in (1) and (2), respectively. So the total power equation will be,

$$\phi_{total} = \left[1 + \frac{(\rho - 1)\,(1 + \lambda\,\tau_{on})}{1 + \beta\,\lambda\,\tau_s}\right]\phi_a + \frac{\lambda\,(1-\rho)\,\tau_{on}}{1 + \beta\,\lambda\,\tau_s}\phi_t + \frac{1-\rho}{1+\beta\lambda\,\tau_s}\phi_{idle} + \rho \times R\left(\frac{E_{HP}}{s} + E_{PT}\right) \quad (4)$$

where ρ is the link utilization factor of the pipeline and can be calculated from (5)

$$\rho = \frac{\lambda\,\beta}{\mu} \quad (5)$$

TABLE I NOTATION

Symbol	Description
μ	Packet service rate of the pipeline in P_y state
β	Average number of packets in the incoming batch
ρ	Link utilization factor of the pipeline
λ	Rate of batch arrival to the pipeline
τ_{on}	Time needed to wake up the HW of the pipeline from C_x sleeping state
τ_{off}	Time needed to put the active HW of the pipeline into C_x sleeping state
τ_s	Setup time of the pipeline in the transition from C_x to P_y
ϕ_a	Power consumption when pipeline is active in P_y state
ϕ_{idle}	Power consumption when the pipeline is sleeping in C_x state
ϕ_t	Power consumption during τ_{on} and τ_{off}
$\tilde{\phi}$	Power consumption for packet processing
R	The maximum link utilization of the router interface (Const)
E_{HP}	Energy consumption for header processing
s	Packet size
E_{PT}	Energy consumption for packet transferring
$P_{interface}$	Power consumption for router interface
$\bar{L}$	Mean value of packets in one burst
j	Number of received packet groups
β_j	Probability that an incoming burst to the pipeline contains j packets
$\bar{W}$	Average packet delay inside the processing engine
ϕ_{total}	Total power consumption of the router

VI. MEASUREMENTS AND ANALYSIS

Firstly, we begin our investigation of power consumption of the router by measuring real world traffic traces between real ISPs in Egypt and Italy. First measurement was based on the inbound traffic profile of core gateway network router in TE Data (Egypt), which is peering with Telecom Italia Sparkle (Italy) and connecting together via STM-16 fiber link (2.4 Gbps). The edge router is Juniper M320 with switching capacity 320 Gbps, and the interface type is serial interface. As shown in Multi Router Traffic Grapher (MRTG) figures. Figure 2 (a) shows the daily traffic pattern, and Figure 2 (b) shows the weekly traffic pattern. The

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evolution of the incoming traffic load follows the classical night-and-day profile with high similarity between days.

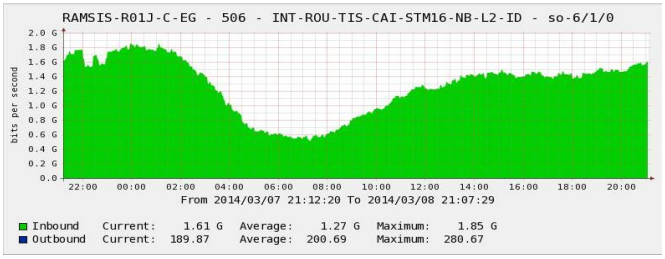

Figure 2. (a) Daily traffic profile of core TE Data network router peering with TIS.

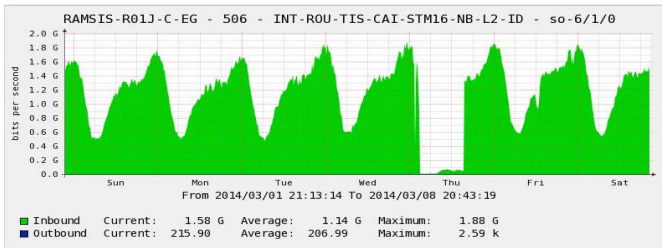

Figure 3. (b) Weekly traffic profile of core TE Data network router peering with TIS.

Second measurement was performed on the inbound traffic profile of other gateway network router in TE Data (Egypt), which is peering with Vodafone (Egypt) and connecting together via STM-16 fiber link. The edge router is also Juniper M320, and the interface type is Giga Ethernet (GE) interface. Figure 3 (a) shows the daily traffic pattern, and Figure 3 (b) shows the weekly traffic pattern.

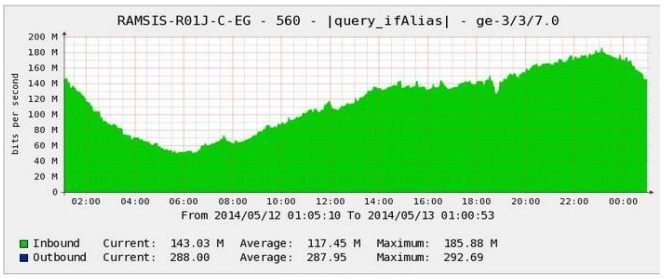

Figure 3. (a) Daily traffic profile of core TE Data network router peering with Vodafone.

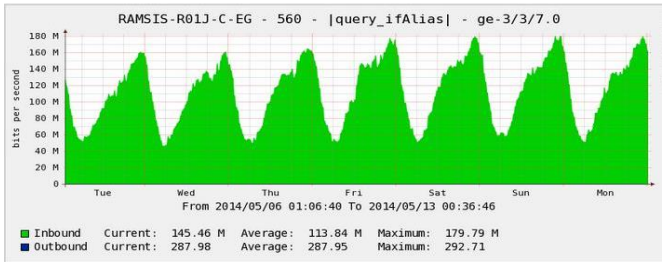

Figure 3. (b) Weekly traffic profile of core TE Data network router peering with Vodafone.

Other traffic distributions are described in Measurement and Analysis on the Wide Internet (MAWI), which is Japanese research group focuses on traffic measurement analysis for long term measurement on Internet, and its real-world traffic traces are publicly available [10] and part of "A Day in the Life of the Internet" [11]. In [7], the experimentations were based on multicore Linux SW Router (SR) and the proposed model estimation was validated by using real-world traffic traces [10][11], and the model evaluation shows an acceptable accuracy. The previous traffic profiles show the regular daily cyclic patterns with traffic dropping at night and growing during the day. In addition, we can figure out that the minimum of the traffic typically appears during the first hours of the morning, while rush hours are during the day. Hence, we can conclude that the traffic distributions are nearly identical regarding different types of edge router platforms, regardless the router architectures, edge router type and interface type.

Secondly, we begin our investigation of the power consumption of packet processing engines using the analytical model of [7], which is validated by the multi core Linux SW Router (SR). This choice is mainly due to the fact that current commercial routers do not include AR and LPI capabilities, and only their nominal and/or maximum power consumptions are reported in the datasheets [7]. By studying the power consumption of packet processing with various configurations of P and C states. The results in Figure 4 show that selecting too deep standby C-states may cause a rise in power consumption. This is simply caused by the wake up τ_s from the deepest C-state. We realized that for high P and C indexes, the packet processing capacity will decrease; also the power consumption of packet processing will be decreased. For low P-C indexes, the packet processing capacity will be increased and the power consumption of packet processing will be increased accordingly.

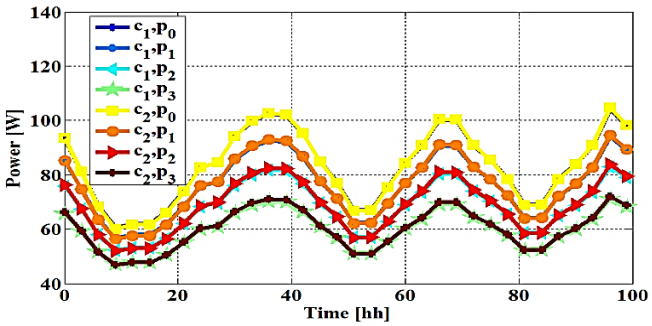

Figure 4. Power consumption of packet processing according to various configurations of P-and C-states.

To figure out the best suitable power states of the pipeline during normal traffic and rush hours, we have to measure the average absolute packet delay, i.e., the average waiting time of the packet inside the processing engine of the pipeline. As shown in Figure 4 and Figure 5, P_3-C_2 state indicates the minimum power consumption (lowest performance) with maximum delay during the minimum volume of traffic loads, while P_3-C_1 state indicates almost the same power consumption (P_3) but with minimum delay during the same minimum value of traffic loads. As a result of that, we suggest reducing the power consumption of the system with P_3 performance (power) state, while not using the deepest sleeping state C_1.

Accordingly, for the maximum traffic volume (rush hours), both P_0-C_1 and P_0-C_2 states indicate the maximum power consumption (highest performance) with minimum delay. As both states have almost the same performance which is P_0, so

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we suggest using P_0-C_1, as it will lead to a minimum delay in case of rush hours. Table II illustrates the power consumption and average packet delay using different P-C states during the maximum and minimum traffic load. By taking into consideration the effect of the power consumption of router interfaces, CISCO 7609 router is used. It is composed of a routing engine, a line card, and one power supply unit. Environment around the router is very important for the precise measurement of the power consumption. The router should be evaluated at temperature of 25℃ ± 3℃ and the relative humidity of 30% to 75%. In addition, the router should be evaluated at a barometric pressure between 1020 and 812 mbar. In the AC power configuration, the router should be evaluated at 230 VAC ± 1%, 50 or 60 Hz ± 1% [8]. We measure the power consumption of router interfaces with each L2 frame size 64, 256, 512 and 1518 bytes. Figure 6 shows the power consumption of the router when the generated traffic is injected to each router interface. We empirically found that the power consumption of the interface is in the direct proportional to the link utilization ρ, as well as in the reverse proportional to the packet sizes. The power consumption increases dramatically when the traffic with 64 bytes L2 frames size. In the other cases, it also increases considerably because the more frames passing through the router, the more power used in the router.

TABLE II POWER CONSUMPTIONS AND AVERAGE PACKET DELAY OF THE DEVICE'S P-C STATES DURING MAXIMUM AND MINIMUM TRAFFIC VOLUME

Value of traffic	Power / Delay	P-C states			
		P_0-C_1	P_0-C_2	P_3-C_1	P_3-C_2
Maximum (Rush Hours)	Power Consumption	Low	High	Low	High
	Average Packet Delay	Low	High	Low	High
Minimum	Power Consumption	High	Low	High	Low
	Average Packet Delay	High	Low	Low	High

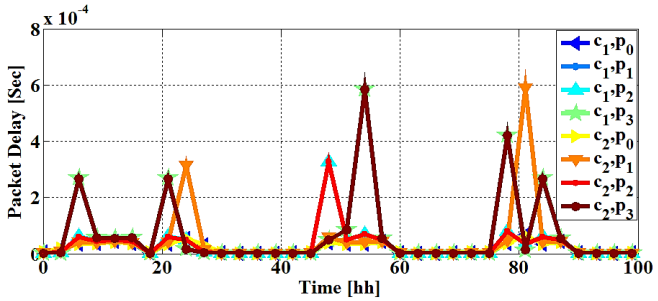

Figure 5. Average absolute packet delay according to various configurations of P-and C-states.

As stated in (5), the packet processing capacity μ is indirect relation to the link utilization ρ. As the packet processing capacity increases, the link utilization factor decreases. Also, as the packet size increases, the link utilization factor will be increases as recited in (3). So there is indirect relation between the packet size and the packet processing capacity as shown in Figure 7. As the packet size increases, the packet processing capacity decreases [12]. Accordingly, the power consumption of the packet processing will be decreased.

As a result, the total power consumption of the router will be decreased.

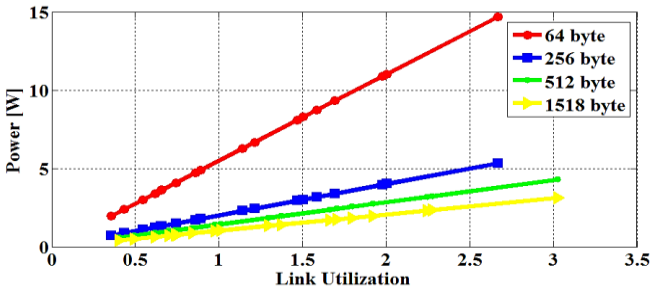

Figure 6. Power consumption of router interface with different packet size.

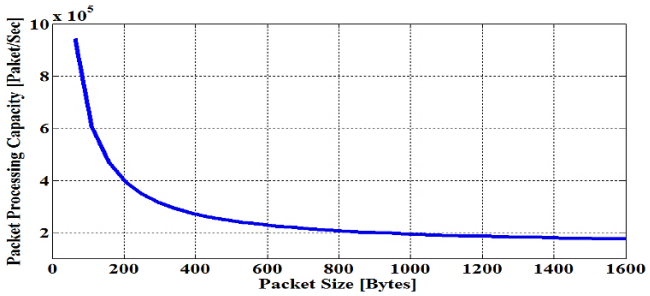

Figure 7. The relation between packet processing capacity and packet size.

Figure 8 and Figure 9 show the total power consumption of the router as stated in (4) for each P_0-C_1 and P_3-C_1 states respectively. As stated previously in section VI, it is obviously shown from Figure 8 that the chosen P_0-C_1 state will lead to high power consumption (highest performance) with minimum possible delay during the maximum volume of traffic loads (rush hour).

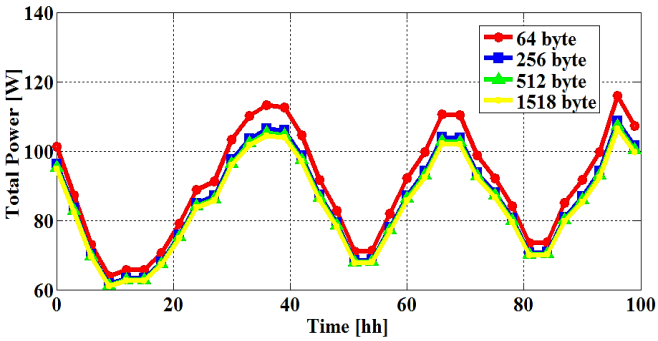

Figure 8. Total power consumption according to P_0-C_1 state.

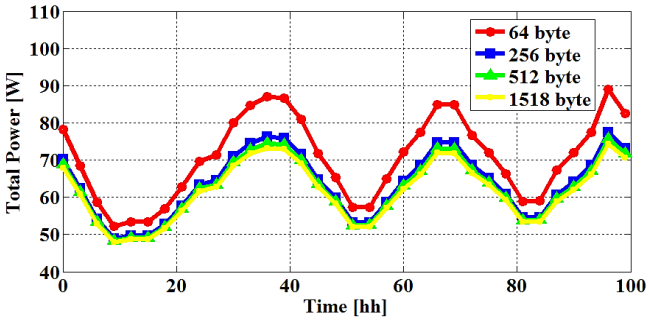

Figure 9. Total power consumption according to P_3-C_1 state.

On contrary for the case of P_3-C_1 state shown in Figure 9 the minimum power consumption (lowest performance) with maximum possible delay during the minimum volume of

traffic loads. The values of ϕ_{idle} , τ_{on}, ϕ_a and μ used for numerical calculation of the total power equation stated in (4) for different P-C states were adopted from [7][12], and are illustrated in Table III and IV.

TABLE III POWER CONSUMPTIONS AND TRANSITION TIMES OF THE DEVICE'S C-STATES

C_X state	ϕ_{idle}	τ_{on}
C_0	Active	Active
C_1	10 Watt	10 ns
C_2	8 Watt	100 ns

TABLE IV POWER CONSUMPTIONS AND FORWARDING CAPACITIES OF THE DEVICE'S P-STATES

P_y state	ϕ_a	μ
P_3	50 Watt	650 kpkts/s
P_2	60 Watt	770 kpkts/s
P_1	70 Watt	890 kpkts/s
P_0	80 Watt	1010 ts/s

VII. CONCLUSION

We proposed an analytical model able to capture the impact of packet size on the packet processing capacity, which will affect the total power consumption of edge router. We found also the best suitable power configuration of pipelines in both high traffic volume (rush hours) and low traffic volume, and achieve the best way to optimize the tradeoff between energy consumption and network performance indexes (delay) using different packet sizes.

Firstly, we considered energy aware network devices able to trade their energy consumption for packet forwarding. We proposed an analytical model able to capture the impact of power management capabilities on network performance. This study is based on the analytical models represented in [7][12]. We focused on the packet processing, which generally represents the most energy consuming components of network devices (60%), as well as the power consumed in router interfaces (13%). Our goal was to find the best suitable power configuration of pipelines in both high traffic volume (rush hours) and low traffic volume; and to achieve the best way to optimize the tradeoff between energy consumption and network performance indexes using different packet sizes.

Secondly, we analyzed and drawn an analytical power consumption model of a router interface. We analyzed it against the packet size. According to the results, we can find that the power consumption of the router interface is in the direct proportion to the link utilization as well as in the reverse proportion to the packet size. Also, we deduced that the packet size is in reverse proportion to the packet processing capacity, which will lead to decrease the power consumption of packet processing inside data plane as well. The obtained results show that for low traffic volumes, it is recommended to use a P-state corresponds to the minimization of energy consumption constrained to low packet latency with high packet size. For high traffic volumes, it is recommended to use a P-state corresponds to the maximization of energy consumption constrained to low packet latency with high packet size. Also, it is suggested not to select too deep standby C-state as it may cause a rise in power consumption to make the transition from the sleeping state C_x to the active C_0 state.

Our future work will study the power consumption of the router taking into consideration the buffer management which consumes 8.5% of the total power inside the data plane. Also, we will study the effect of different routing protocols on the total power consumption besides more practical results by setting a practical test bed to validate the analytical model using Network Performance Monitor (NPM) and edge routers support the energy wise feature.

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