Comparison of Receiver Architecture in Terms of Power Consumption and Noise Figure for Cochlear Implants Application

U. Cerasani, W. Tatinian
University Nice Sophia Antipolis
LEAT, Valbonne, France
umberto.cerasani@unice.fr
william.tatinian@unice.fr

P. Ndungidi, C. Dualibe, C. Valderrama
Université de Mons
Mons, Belgique
papy.ndungidi@umons.ac.be
Fortunato.Dualibe@umons.ac.be
Carlos.Valderrama@umons.ac.be

***Abstract*– Change in patients requirements has lead to new cochlear implants architecture specifications. In this paper, we proposed the receiver chain architecture study and design for new type of cochlear implants. Two receiver architectures were compared in terms of power consumption and Noise Figure, both of fundamental importance in biomedical embedded systems. SPICE simulations of the these architectures were carried out and transient results were presented for the solution retained. Furthermore optimization of the Low Noise Amplifier (LNA) using mathematical computations is presented, increasing the entire receiver performances.**

Keywords: SPICE Simulations, RF Receiver, LNA Optimization

I. INTRODUCTION

Cochlear implant is a device aiming to aid severely deaf people to partially recover hearing (electrical description of cochlear implant can be found in). A prototype aiming to make the implant less noticeable is presented in. In this new cochlear implant prototype, the transmitter is inserted inside the auditory canal, sending Radio Frequency (RF) waves (allowing reduced antenna size) to the receiver located inside the patient' s skull. As the auditory canal space is limited, the battery size and its charge are the main limiting factors for the emitter design, diminishing its performances.

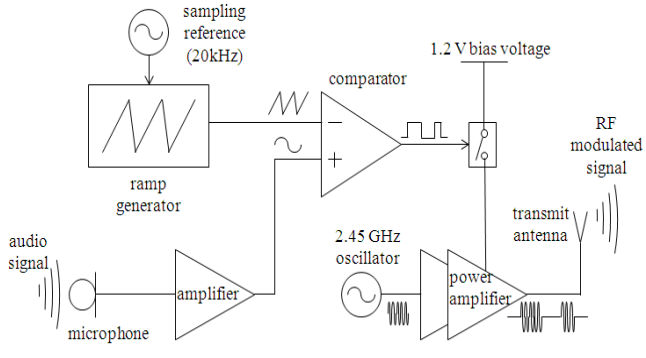

Figure 1: Transmitter architecture (redrawn from)

According to the work presented in, the Digital Signal Processor (DSP) that was previously located in the emitter, can be integrated on the receiver. This has the advantage of reducing the emitter consumption but on the other hand implies an electrical architecture reworking. The emitter has already been presented in and the architecture is recalled in Figure 1. The input signal coming from the microphone was compared with a ramp reference signal to create a Pulse Width Modulated (PWM) signal, then multiplied by a 2.45GHz oscillator to create the RF signal sent to the transmitter antenna.

The aim of this paper is to select the receiver architecture fitting the most with the cochlear implants specifications and then to optimize its critical block in terms of Noise Figure and power consumption as explained in Section III. The receiver architectures overview is presented in Section IV, followed by the mathematical optimization of the LNA. Two different types of receiver front end architectures are then discussed and compared in terms of added noise and power consumption (Section V.), before presenting our concluding remarks and preferences.

II. RECEIVER ARCHITECTURE

The communication channel between the transmit- and the receive antenna is presented in, leading to an estimated received power of -87dBm, and added noise in the propagation channel of -95dBm. Those values were computed from the maximal authorized emitted power in the ISM band (20dBm), the attenuation in human tissue with corresponding dielectric constants, the ISM bandwidth (80MHz) and assuming a white noise distribution. This fixes the LNA sensitivity and is used as basis for the receiver specifications and architecture selection.

The selected architecture for the receiver includes a low noise amplifier followed by an amplitude demodulation stage and a digital signal processing unit controlling the electrodes array, which is implanted inside the patient's cochlea.
Electrodes array are the most consuming part of the receiver (their power consumption estimation is around 50mW [*4*]) and this energy cannot be reduced for proper nerve fibers

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excitation. The total electronic consumption should be significantly lower than the electrodes array consumption to increase battery lifetime

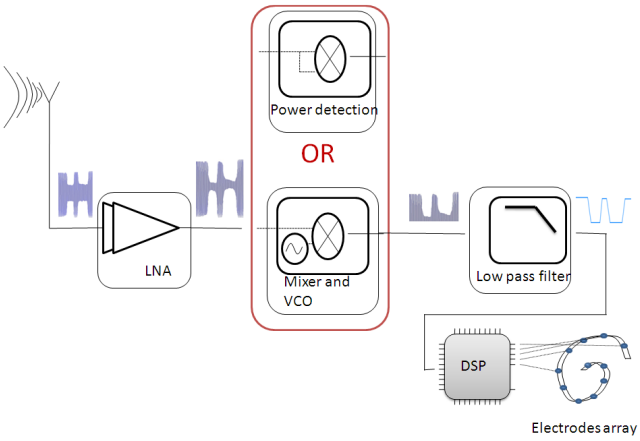

Figure 2 : Transmitter architecture overview, with signal outputs in color

Ultra low power processors currently available in market consume few µW at the 1MHz working frequency [5], [6]. Ultra-low-energy biomedical signal processors (BSPs) are nowadays being developed with overall energy consumption around 100 pJ/cycle with a working frequency of 1MHz (a state of the art review can be found in [7]). Therefore more constraints in term of power consumption are put in the RF/analog electronic devices of the receiver, which should not contain complex blocks for envelop detection.

Most particularly, a high consumption would lead to an increase of the battery reload frequency, which is inconvenient for the patients. Because of low power constraints, power repartition between blocks becomes fundamental. The unique block allowed to consume more power was the LNA in order to decrease the total Signal-to-Noise Ratio (SNR) of the entire receiver as explained in Section III.

As presented in Figure 2, two architectures are investigated for the AM demodulation: a power detection using a mixer with the RF and LO inputs connected together and a coherent demodulation composed of a mixer and a local oscillator at the same frequency as the input signal. The output signal is a PWM-like waveform and is low-pass filtered to recover the initial signal amplitude. Linearity is not significant as the PWM signal maximum frequency (around 2MHz) is substantially lower than the carrier frequency (2.45GHz).

III. LNA OPTIMIZATION

As a direct consequence of the Friss equation [8] (reminded in (1)) the Noise Factor of the entire receiver is greatly dependent on the LNA Noise Factor and gain. Consequently we decided to optimize the LNA design in terms of power consumption and noise figure.

$$F_{total} = F_{LNA} + \frac{F_{demod} - 1}{G_{LNA}} + \frac{F_{filter} - 1}{G_{LNA}\, G_{demod}} \qquad (1)$$

Where F_{LNA}, F_{demod} and F_{filter} are the Noise Factor of the LNA, the Noise Factor of the blocks composing each demodulating topology and the Noise Factor of the RC filter respectively. G_{LNA} and G_{demod} are the Power Gains with load of the LNA and the blocks composing each demodulating topology respectively.

TABLE I. : COMPONENT VALUES OF THE LNA OBTAINED BY MATHEMATICAL COMPUTATION

	Implemented values
Center Frequency	**2.475 GHz**
Voltage supply	**1.2 V**
Current Consumption	**10 mA**
L_L	**1.3 nH**
C_L	**3.18 pF**
$L_{M1,M2}$	**0.15 um**
$W_{M1,2}$	**165 um**
NF	**1. 4**
L_S	**0.14 nH**
L_G	**14.3 nH**

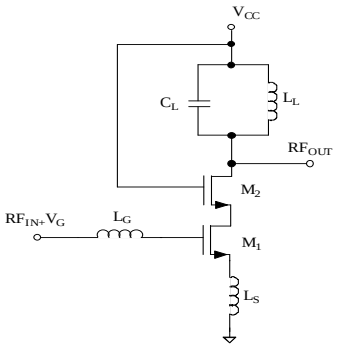

Figure 3: Circuit of the Low Noise Cascode Amplifier

Figure 3 shows the schematic of the implemented LNA. The cascode stage (M_2) is used to improve input-output isolation, reduce the Miller effect and, consequently, increase the bandwidth. The resonant circuit formed by L_L and C_L permits a high gain with a low voltage supply at the frequency of interest. With L_G and L_S a narrow band input impedance matching is obtained. The input transistor (M_1) is used in inductively degenerated common-source configuration.

TABLE II: PARAMETERS OBTAINED BY MATHEMATICAL COMPUTATION AND WITH CADENCE SIMULATION

	Mathematical computation	Cadence evaluation
RF Frequency	2.4GHz	**2.45GHz**
S21	>17dB	**24.7dB**
S11	-10dB	**-7.11dB**
S22	-10.1dB	**-1.5dB**
NF	<1.4 dB	**0.75dB**
Power Consumption	13.2 mW	**11.71mW**

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The width of the transistor and the other parameters of the circuit were mathematically computed using a similar development than the method presented by Thomas H. LEE [9], minimizing the Noise Figure while optimizing power consumption.

For both architecture, we evaluated the receiver performances using a 0.13µm RF CMOS technology. Table I shows the values obtained from calculations, after some minor modifications according to the target CMOS 130 nm process.The results of simulations are summarized in Table II.

In practice, equations used for this optimization were derived from first order modeling (SPICE level [10]) and provided general characterization of the LNA further refined by Cadence simulations (especially modifying the polarization of M1), explaining the improvements in Table II, especially in terms of NF and gain.

IV. RECEIVER ARCHITECTURES IMPLEMENTED

The two architectures presented in Figure 2 were implemented in SPICE and they were compared in terms of power requirements and noise addition. The LNA and the filter were common to both solutions. The polarizing circuitry is not shown in the figures.

A. Solution 1: LNA and Power Detector

The input signal is the one received by the antenna (2.4GHz carrier modulated in amplitude by a PWM signal) and the LNA output is connected to the Local Oscillator Input (LO +) as well as on the RF input of the Mixer. The Power Detector is therefore created using a mixer with its inputs connected to the same source. We designed a single balanced Mixer because of its low power consumption. However, as the DC offset is injected directly in the RF source, it degrades the mixer linearity [11], not of importance in our application.

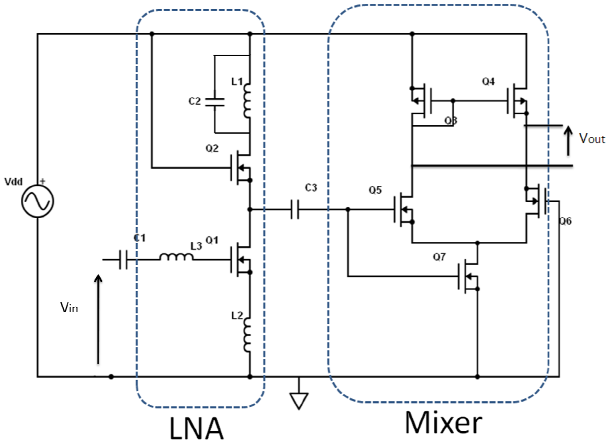

Figure 4: Receiver architecture solution 1 with a LNA and a power detector

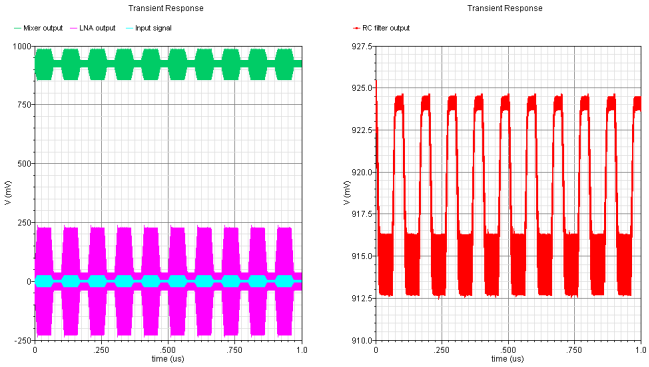

Figure 5: Transient simulations including the input signal, the LNA output, the mixer output (right) and the RC filter output (left)

The designed mixer has a NF of 20dB, and its output is directly connected to the RC filter. The simplified schematic of the Solution 1 is presented Figure 4 (with bias circuit removed for clarity reasons) and the associated transient simulations are presented in Figure 5.

For the test case, the PWM signal was created with a 1 kHz sine wave, which was sampled at 1MHz. The RF input signal is represented in light blue and the corresponding magnitude is low enough to make the LNA operate within the linear region. Removing the DC voltage, the output signal is represented in pink, where one can see that the ratio between the maximal and minimal magnitude is around 5, which is high enough for a further OOK demodulation. The effects of rising and falling times are also visible on the curve. As a result, after filtering, we obtained a signal that corresponds to the emitted signal, where the distortions and the low output magnitude are mainly due to the low power consumption of the mixer (100µA).

The main advantage of this architecture was the use of only two active devices (LNA and mixer) instead of three (in the other solution).

B. Solution 2: LNA, Mixer and VCO

The oscillator used is an L-C tank oscillator with a central frequency of 2.45GHz and frequency control (V_{tune}) to compensate the frequency shift due to temperature variations within the human body (presented in Figure 6).

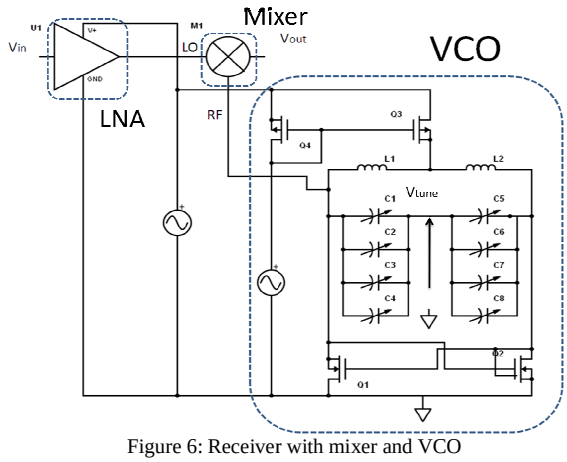

Figure 6: Receiver with mixer and VCO

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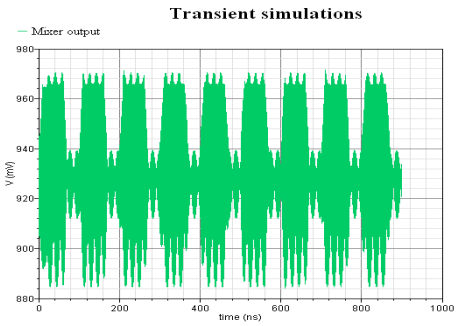

Figure 7: Transient simulation of the mixer output in the second architecture

The width of the NMOS of the differential pair is 210µm and the length is 150nm, which drives a current of 10mA. The Noise Figure of the cross coupled pair was obtained with SPICE simulations and was found equal to 7dB. Then, using Periodic Steady-State (PSS) analysis, we estimated the phase noise, which was around -120dBc/Hz at 1MHz from the carrier (PWM maximal frequency).

Transient simulation results are presented in Figure 7, where one can see that the output voltage magnitude of the mixer is much higher than in the previous architecture, at the cost of output oscillations due to the frequency shift between LO and RF. Indeed this shift is inevitable as low power constraints did not allow carrier recovery. Nevertheless, this distortion may be removed by subsequent Signal Processing.

V. ARCHITECTURE COMPARISON

The main requirements of our receiver was its low power consumption and a very reduced Noise Figure. Maximizing SNR at the receiver output (before DSP computation) is hence very relevant and consists on minimizing the total Noise Factor of the receiver.

TABLE III: NOISE FACTOR AND POWER COSUMPTION COMPARISON

	Power Detector	Mixer and VCO
Power Consumption (mW)	**11.91**	**21.4**
NF	**2.57**	**2.61**

Total Noise Factor computation is expressed by the Friss formula as previously stated in (1).

The Noise Factors comparison for each solution are shown in Table III, as well as their respective Power Consumption estimation.

The solution with VCO is consuming twice as much power as the solution with the Power Detector. This results in a total extra energy of about 100mA*h per day (assuming that the device is activated during 8 hours per day).

As discussed in Section II. the increase in power consumption of the RF front end represents between 20% to 40% of the power consumed by the electrodes array depending on the selected topology.

As stated in Section III.B., the effect of the VCO phase noise is not significant compared to the frequency shift associated with the absence of carrier recovery in the receiver. This may significantly corrupt the signal rectification as the signal translation into lower frequencies is followed by the RC filter.

In consequence, it is authors' belief that the first architecture should be preferred for this application. Optimization algorithms such as NSG2 presented in [12] are available and permits optimization of the overall architecture to maximize parameters of interest (still under work).

VI. CONCLUSION

This paper presented the study and design of the receiver front end architecture for new type of cochlear implants.

As the LNA block was compulsory in both the solutions and significantly impact the overall architecture Noise Figure, its optimization using mathematical computation was first performed before its implementation in Cadence and subsequent refinement.

Two receiver architectures were compared in terms of power consumption and Noise Figure, both of fundamental importance in biomedical embedded systems. The architecture with Power Detector was preferred for our application, as it consumed less and did not suffer of frequency shift, which could impact the signal demodulation.

The optimization of the overall LNA and Power detector architecture is ongoing, using a nonlinear multi-objective optimization, based on the Genetic Algorithm (GA) NSGA II.

This overall optimization may be necessary if the measured Noise Power inside the transmission channel would be greater that the estimated one, yet very close to the Signal Power received by the antenna.

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