Improved Linearity CMOS Active Resistor Structure Using Computational Circuits

Cosmin Popa
University Politehnica of Bucharest, Romania
1-3 Iuliu Maniu, Bucharest, Romania
email: cosmin_popa@yahoo.com

***Abstract*-A new low-power low-voltage active resistor structure with improved performances will be presented. The problem of circuit linearity is solved by implementing an original technique, using a proper current biasing of the differential core, while the existing solutions allow only a partial improvement of the circuit performances. The structures are implemented in $0.35\mu m$ CMOS technology and are supplied at $\pm 3V$. The circuits present a very good linearity (in the worst case, total order distortions $< 0.4\%$), correlated with an extended range of the input voltage (at least $\pm 0.5V$). The tuning range of the active resistors is about hundreds $k\Omega$ - $M\Omega$.**

Keywords-Linearity; active resistor circuit; computational circuits; VLSI design.

I. INTRODUCTION

CMOS (Complementary Metal Oxide Semiconductor) active resistors [1][2][3][4] are very important blocks in VLSI analog designs, mainly used for replacing the large value passive resistors, with the great advantage of a much smaller area occupied on silicon. Their utilisation domains include amplitude control in low distortion oscillators, voltage controlled amplifiers and active RC filters. These important applications for programmable floating resistors have motivated a significant research effort for linearising their current-voltage characteristic. The first generation of MOS active resistors [1] [2] used MOS transistors working in the linear region. The main disadvantage is that the realized active resistor is inherently nonlinear and the distortion components were complex functions on MOS technological parameters. A better design of CMOS active resistors is based on MOS transistors working in saturation. Because of the quadratic characteristic of the MOS transistor, some linearization techniques [3][4] were developed in order to minimize the nonlinear terms from the current-voltage characteristic of the active resistor. An important class of these circuits, referring to the active resistors with controllable negative equivalent resistance, covers a specific area of VLSI designs, finding very large domains of applications such as the cancelling of an operational amplifier load or the design of Deboo [5] integrators with improved performances.

The original idea proposed in this paper is to use a linear CMOS differential amplifier for obtaining (with minor changes in the design) two important functions:

- Simulation (in a first-order analysis) of a perfect linear resistor using exclusively MOS active devices, having the advantages of a very good controllability of the equivalent resistance and of an important reduction of the silicon occupied area, especially for large value of the simulated resistance;
- Simulation of a controllable negative resistance circuit with improved linearity;

A. State of the art

The paper contains a section describing the theoretical basis of the design methods, followed by a section presenting some important simulation results and, in the end, a conclusion.

II. THEORETICAL ANALYSIS

A. Improved linearity MOS differential structure

An improved linearity MOS differential structure represents the core of the original active resistor circuit with improved linearity (Figure 1). "SQ" block is a squaring circuit, having the original implementation presented in Figure 3.

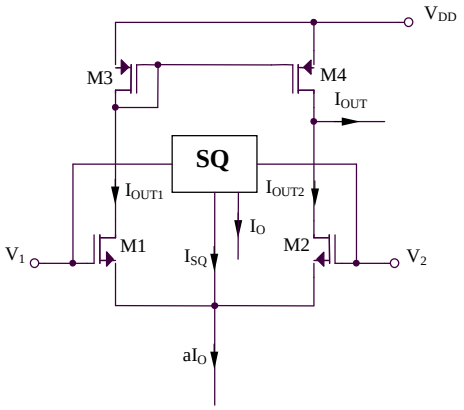

Figure 1. Improved linearity MOS differential structure

 ISBN: 978-1-61208-151-9

The differential output current for this circuit has the following expression:

$$I_{OUT} = (V_1 - V_2)\sqrt{K(aI_O - I_{SQ}) - \frac{K^2}{4}(V_1 - V_2)^2}\ . \quad (1)$$

In order to obtain a linear behavior of the proposed differential structure, the I_{SQ} output current of the squaring circuit "SQ" must be the sum of a constant term and a term proportional with the square of the differential input voltage:

$$I_{SQ} = bI_O - \frac{K}{4}(V_1 - V_2)^2, \quad (2)$$

b being a positive constant, depending on the particular implementation of the squaring circuit. Replacing (2) in (1), it results:

$$I_{OUT} = \sqrt{(a-b)KI_O}\,(V_1 - V_2) = G_m(V_1 - V_2), \quad (3)$$

$G_m = \sqrt{(a-b)KI_O}$ being the circuit equivalent transconductance.

The proposed method for designing the required voltage squaring circuit is based on a differential amplifier (Figure 3), having a controllable asymmetry between the geometries of its composing transistors. This difference between the aspect ratios of MOS transistors will introduce in the output currents of the differential amplifier a term proportional with the square of the differential input voltage.

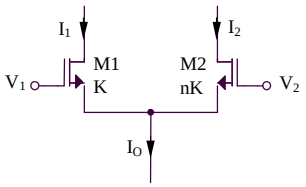

Figure 2. Asymmetrical differential structure

The differential input voltage, V, can be expressed as follows:

$$V = V_{GS1} - V_{GS2} = \sqrt{\frac{2I_1}{K}} - \sqrt{\frac{2(I_O - I_1)}{nK}}, \quad (4)$$

resulting:

$$\frac{K}{2}V^2 = I_1 + \frac{I_O - I_1}{n} - 2\sqrt{\frac{I_1(I_O - I_1)}{n}}. \quad (5)$$

The expression of I_1 current can be obtained solving the following second-order equation, derived from (5):

$$I_1^2\left[\left(\frac{n-1}{n}\right)^2 + \frac{4}{n}\right] + \left(\frac{I_O}{n} - \frac{KV^2}{2}\right)^2 + I_1\left[2\frac{n-1}{n}\left(\frac{I_O}{n} - \frac{KV^2}{2}\right) - \frac{4I_O}{n}\right] = 0 \quad (6)$$

So:

$$I_1 = \frac{I_O}{n+1} + \frac{n(n-1)}{2(n+1)^2}KV^2 + \frac{nV}{(n+1)^2}\sqrt{2KI_O(n+1) - K^2nV^2} \quad (7)$$

and:

$$I_2 = I_O - I_1 = \frac{nI_O}{n+1} - \frac{n(n-1)}{2(n+1)^2}KV^2 - \frac{nV}{(n+1)^2}\sqrt{2KI_O(n+1) - K^2nV^2}\ . \quad (8)$$

The complete realization of a voltage squaring circuit, based on the previous proposed method, uses a cross-coupling of two differential amplifiers having controllable asymmetries between their geometries, M1-M2 and M3-M4 (Figure 3).

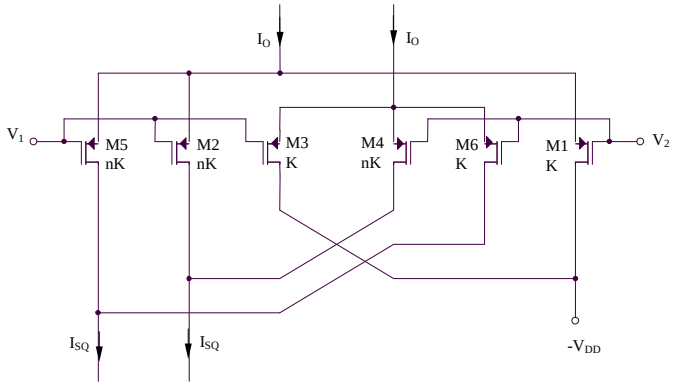

Figure 3. Squaring circuit

Using (7) and (8), it results:

$$I_{SQ} = I_{D2} + I_{D4} = \frac{nI_O}{n+1} - \frac{n(n-1)}{2(n+1)^2} KV^2 - \\ - \frac{nV}{(n+1)^2}\sqrt{2KI_O(n+1) - K^2nV^2} + \\ + \frac{nI_O}{n+1} - \frac{n(n-1)}{2(n+1)^2} KV^2 + \\ + \frac{nV}{(n+1)^2}\sqrt{2KI_O(n+1) - K^2nV^2} = \\ = \frac{2nI_O}{n+1} - \frac{n(n-1)}{(n+1)^2} KV^2 \quad . \quad (9)$$

B. Positive resistance active resistor circuit

The proposed active resistor circuit with positive equivalent resistance is presented in Figure 4.

The current passing between the input pins V_1 and V_2, $I_{OUT} = I_{OUT1} - I_{OUT2}$ has the following expression:

$$I_{OUT} = (V_1 - V_2)\sqrt{K\frac{aI_O - I_{SQ}}{2} - \frac{K^2}{4}(V_1 - V_2)^2} \quad , \quad (10)$$

because each differential amplifier M1-M4 and M2-M3 is biased at a current equal with:

$$I_{OUT1} + I_{OUT2} = \frac{aI_O - I_{SQ}}{2} \quad . \quad (11)$$

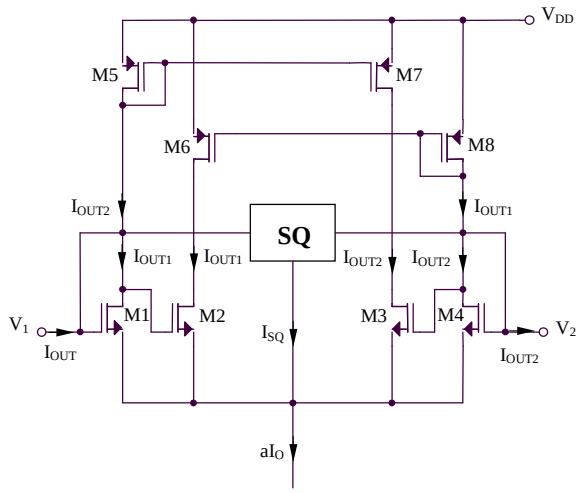

Figure 4. Positive resistance active resistor circuit

Using the expression (9) of I_{SQ} current, it results:

$$I_{OUT} = (V_1 - V_2)\sqrt{\frac{KI_O}{2}\left(a - \frac{2n}{n+1}\right) + \frac{K^2(V_1 - V_2)^2}{2}\left[\frac{n(n-1)}{(n+1)^2} - \frac{1}{2}\right]} \quad . \quad (12)$$

The conditions for obtaining a linear behavior of the circuit can be written as:

$$\frac{n(n-1)}{(n+1)^2} = \frac{1}{2}, \quad (13)$$

resulting:

$$n_{1,2} = 2 \pm \sqrt{5} \quad (14)$$

and:

$$I_{OUT} = (V_1 - V_2)\sqrt{\frac{KI_O}{2}\left(a - 2\frac{2 \pm \sqrt{5}}{3 \pm \sqrt{5}}\right)} \quad . \quad (15)$$

The equivalent resistance of the circuit presented in Figure 5 will be:

$$R_{ECH} = \frac{V_1 - V_2}{I_{OUT}} = \left[\frac{KI_O}{2}\left(a - 2\frac{2 \pm \sqrt{5}}{3 \pm \sqrt{5}}\right)\right]^{-1/2} \quad . \quad (16)$$

C. Negative resistance active resistor circuit

The proposed active resistor circuit with negative equivalent resistance is presented in Figure 5.

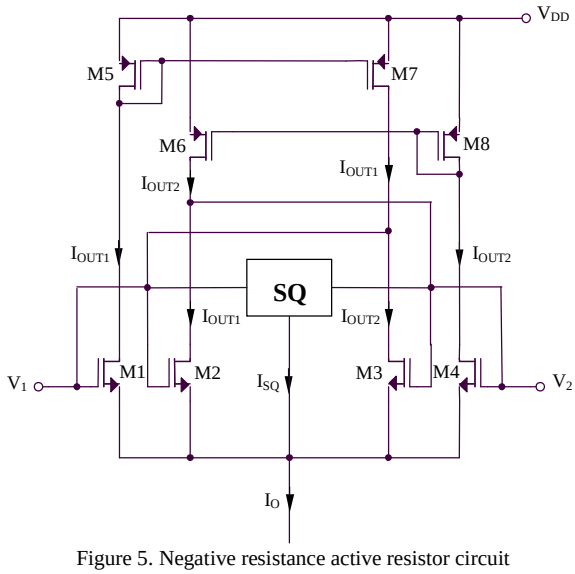

Figure 5. Negative resistance active resistor circuit

 ISBN: 978-1-61208-151-9

The equivalent resistance of the circuit presented in Figure 6 will be:

$$R_{ECH} = -\frac{V_1 - V_2}{I_{OUT}} = -\left[\frac{KI_O}{2}\left(a - 2\frac{2 \pm \sqrt{5}}{3 \pm \sqrt{5}}\right)\right]^{-1/2} . \quad (17)$$

III. SIMULATED RESULTS

The SPICE [6] simulation $I_{OUT1,2}(V)$ based on $0.35\ \mu m$ CMOS technology parameters for the original differential amplifier from Figure 1 (representing the core of the multifunctional structure) is presented in Figure 6, showing a very small linearity error. The supply voltage corresponds to low-power requirements, $V_{DD} = 3\ V$.

The simulation shows a very good linearity of the original differential structure.

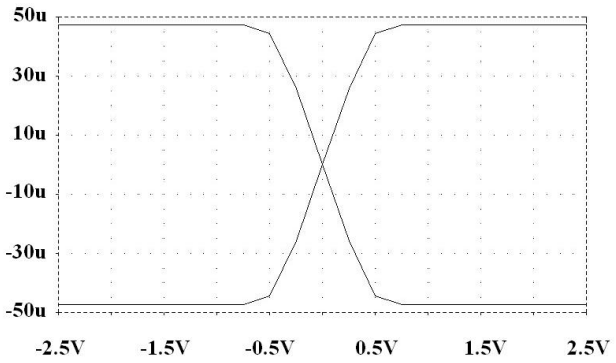

Figure 6. Simulation of the transfer characteristic for the original differential structure

IV. AKNOWLEDGMENTS

This work was supported by POSDRU/89/1.5/S/62557 project.

V. CONCLUSION

A new low-power low-voltage active resistor structure with improved performances has been presented. The linearity is strongly increased by implementing an original technique, using a proper current biasing of the differential core. The structures are implemented in $0.35\mu m$ CMOS technology and are supplied at $\pm 3V$. The circuits present a very good linearity (in the worst case, $THD < 0.4\%$), correlated with an extended range of the input voltage (at least $\pm 0.5V$). The tuning range of the active resistors is about hundreds $k\Omega$ - $M\Omega$.

REFERENCES

[1] Z. Wang, "Current-controlled Linear MOS Earthed and Floating Resistors and Application," *IEEE Proceedings on Circuits, Devices and Systems*, 1990, pp. 479-481

[2] L. Sellami, "Linear Bilateral CMOS Resistor for Neural-type Circuits," *Proceedings of the 40th Midwest Symposium on Circuits and Systems*, vol. 2, 1997, pp. 1330-1333.

[3] C. Muniz-Montero, R. Gonzalez-Carvajal, A. Diaz-Sanchez, and J.M. Rocha, "Low Frequency, Current Mode Programmable KHN Filters Using Large-Valued Active Resistors", Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on, 27-30 May 2007, pp. 3868 – 3871

[4] T. Sanchez-Rodriguez, C. Lujan-Martinez, R. Carvajal, J. Ramirez-Angulo, and A. Lopez-Martin, "CMOS Linear Programmable Transconductor Suitable for Adjustable Gm-C Filters", Electronics Letters, Volume 44, Issue 8, April 10 2008, pp. 505 – 506

[5] A.M. Soliman, M. Ismail, "Novel Passive and Active Compensated Deboo Integrators", Proceedings of the IEEE, Vol. 67, Issue 2, 1979, pp. 324-325

[6] http://bwrc.eecs.berkeley.edu/classes/icbook/spice/

 ISBN: 978-1-61208-151-9