

# Asynchronous Sequential Symbol Synchronizers based on Pulse Comparison by Positive Transitions at Bit Rate

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**Abstract-** This work studies the asynchronous sequential symbol synchronizers based on pulse comparison by positive transitions at rate (ap). Their performance will be compared with the reference asynchronous symbol synchronizers based on pulse comparison by both transitions at rate (ab). For the reference and proposed variants, we consider two versions which are the manual (m) and the automatic (a). The objective is to study the four synchronizers and evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal Noise Ratio).

**Keywords -** Synchronism; Digital Communications

## I. INTRODUCTION

This work studies the asynchronous sequential symbol synchronizer based on pulse comparison operating by positive transitions at rate (ap). Their jitter is compared with the reference asynchronous synchronizers operating by both transitions at rate (ab) [1, 2].

For both, reference and proposed variant, we consider the versions manual (m) and automatic (a) [3, 4, 5, 6, 7].

The difference between the reference and proposed synchronizer is in the symbol phase comparator since the others blocks are similar. The phase comparator compares the input variable pulse duration  $P_v$  with the intern reference fixed pulse duration  $P_f$  and the error pulse  $P_e$  synchronizes the VCO (Voltage Controlled Oscillator) [8, 9].

The synchronizer regenerates the data, recovering a clock (VCO) that samples and retimes the data [10, 11, 12, 13].

Fig. 1 shows the blocks of the general symbol synchronizer.

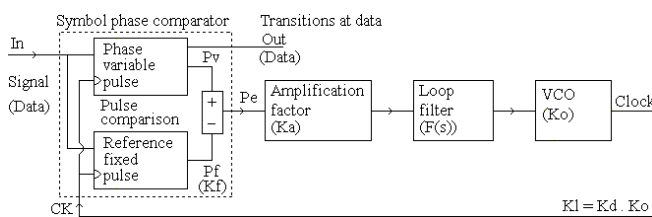


Figure 1. Synchronizer based on pulse comparison

Following, we present the reference variant, asynchronous sequential symbol synchronizers based on pulse comparison by both transitions at rate, with versions manual (ab-m) and automatic (ab-a). Next, we present the proposed variant, asynchronous sequential symbol synchronizer based on pulse comparison by positive transitions at rate, with versions manual (ap-m) and automatic (ap-a).

After, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

## II. ANTERIOR WORK AND NEW CONTRIBUTIONS

While various types of synchronizers were developed, very little has done on evaluating their quality.

The motivation of this work is to create new synchronizers and to evaluate their performance with noise. This contribution increases the knowledge about synchronizers.

Before, we presented various synchronous synchronizers, now, we will present the asynchronous synchronizers [1,2,3].

## III. REFERENCE BY BOTH AT RATE

The reference, asynchronous sequential symbol synchronizers based on pulse comparison operating by both transitions at bit rate has two versions which are the manual (ab-m) and the automatic (ab-a) [1, 2].

The versions difference is in the phase comparator, the variable pulse  $P_v$  is common but the fixed  $P_f$  is different.

### A. Reference by both at rate manual (ab-m)

The block  $P_v$ , shown below, produces a variable pulse  $P_v$  between the input bits and VCO. The manual adjustment delay with Exor produces a manual fixed pulse  $P_f$  (Fig. 2).

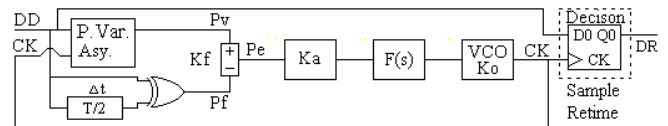


Figure 2 Asynchronous by both at rate and manual (ab-m)

The comparison between the pulses  $P_v$  and  $P_f$  provides the error pulse  $P_e$  that forces the VCO to synchronize the input. The block  $P_v$  is an asynchronous circuit (Fig. 3).

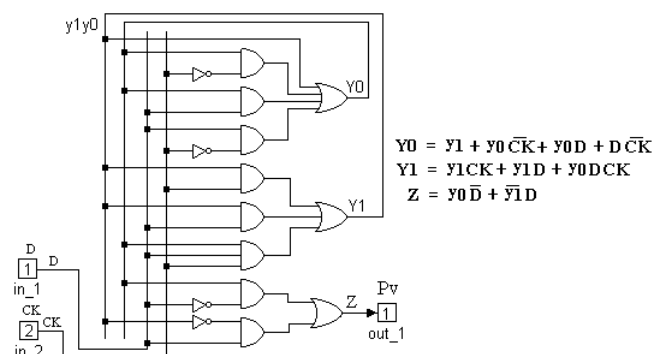


Figure 3. Intern aspect of the block  $P_v$

Fig. 4 shows the waveforms of the reference manual (equal to the corresponding synchronous by both at rate) [3].

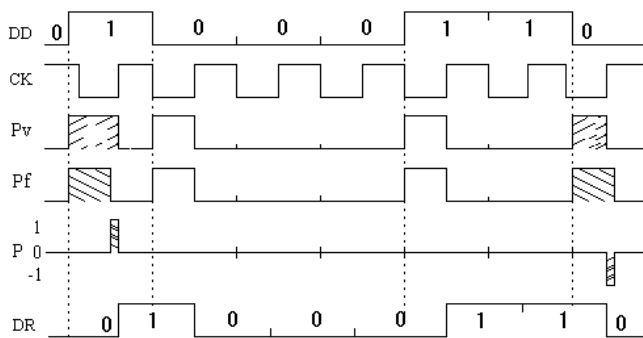


Figure 4. Waveforms of the asynchronous by both at rate manual

The error pulse  $P_e$  diminishes during the synchronization time and disappear at the equilibrium point.

**B. Reference by both at rate automatic (ab-a)**

The block  $P_v$ , common with anterior, produces the variable pulse  $P_v$  between input and VCO. The block  $P_f$ , shown below, produces the comparison fixed pulse  $P_f$  (Fig. 5).

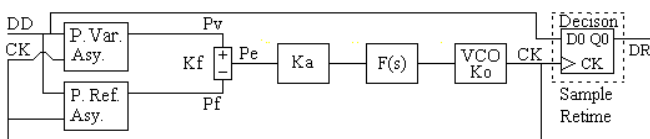


Figure 5. Asynchronous by both at rate and automatic (ab-a)

The comparison between the pulses  $P_v$  and  $P_f$  provides the error pulse  $P_e$  that forces the VCO to follow the input. The block  $P_f$  is an asynchronous circuit (Fig. 6).

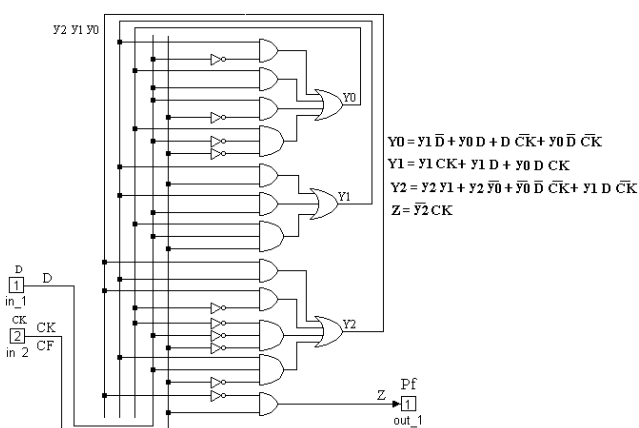


Figure 6. Intern aspect of the block Pf

Fig. 7 shows the waveforms of the reference automatic (equal to the corresponding synchronous by both at rate) [3].

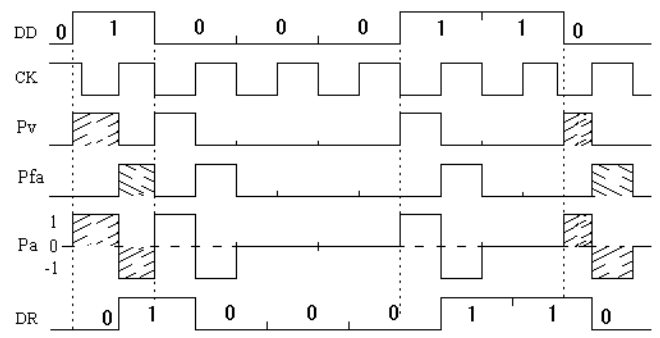


Figure 7. Waveforms of the asynchronous by both at rate automatic

The error pulse  $P_e$  does not disappear, but the variable area  $P_v$  is equal to the fixed  $P_f$  at the equilibrium point.

**IV. PROPOSED BY POSITIVE AT RATE**

The proposed, asynchronous sequential symbol synchronizers based on pulse comparison operating by positive transitions at bit rate has also two versions namely the manual (ap-m) and the automatic (ap-a) [3, 4].

The versions difference is in the phase comparator, the variable pulse  $P_{vp}$  is common but the fixed  $P_{fp}$  is different.

**A. Proposed by positive at rate manual (ap-m)**

The block  $P_{vp}$  produces the variable pulse  $P_{vp}$  between input positive transitions and VCO. The manual adjustment delay  $T/2$  with AND produces a fixed pulse  $P_{fp}$  (Fig. 8).

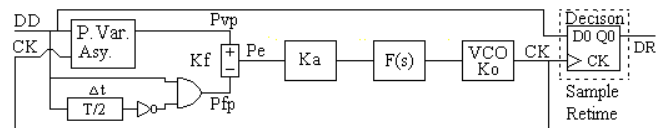


Figure 8. Asynchronous by positive at rate and manual (ap-m)

The comparison between pulses  $P_{vp}$  and  $P_{fp}$  provides the error pulse  $P_e$  that forces the VCO to synchronize the input. The block  $P_{vp}$  is an asynchronous circuit (Fig. 9).

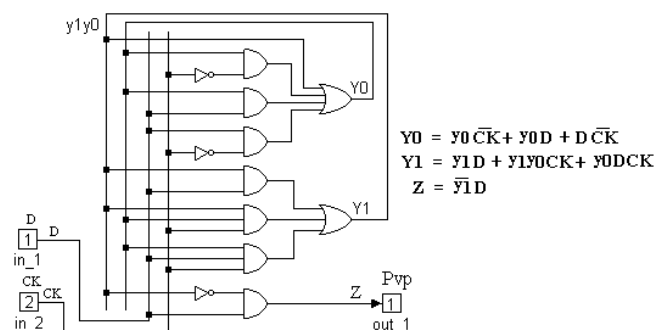


Figure 9. Intern aspect of the block Pvp

Fig. 10 shows the waveforms of the proposed manual (equal to the corresponding synchronous version) [3].

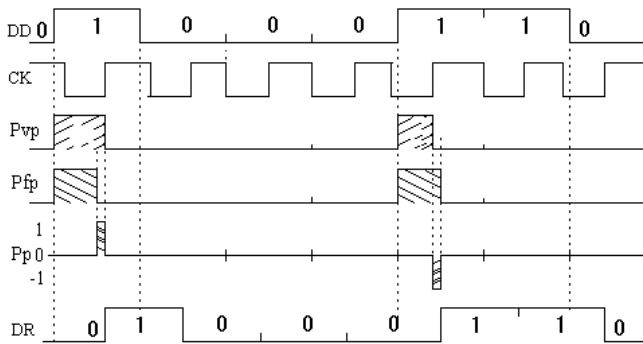


Figure 10. Waveforms of the asynchronous positive at rate manual

The error pulse  $P_e$  diminishes during the synchronization time and disappears at the equilibrium point.

**B. Proposed by positive at rate automatic (ap-a)**

The block  $P_{vp}$ , common, produces the variable pulse  $P_{vp}$  between input and VCO. The block  $P_{fp}$ , shown below, produces the comparison fixed pulse  $P_{fp}$  (Fig. 11).

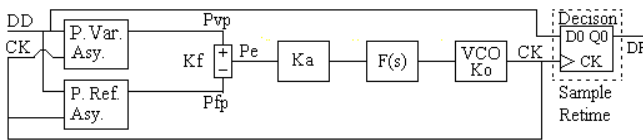


Figure 11. Asynchronous by positive at rate and automatic (ap-a)

The comparison between the pulses  $P_{vp}$  and  $P_{fp}$  provides the error pulse  $P_e$  that forces the VCO to follow the input. The block  $P_{fp}$  is an asynchronous circuit (Fig. 12).

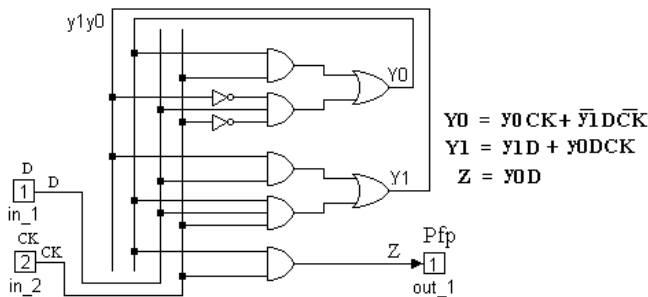


Figure 12. Intern aspect of the block Pfp

Fig. 13 shows the waveforms of the proposed automatic (equal to the corresponding synchronous version) [3].

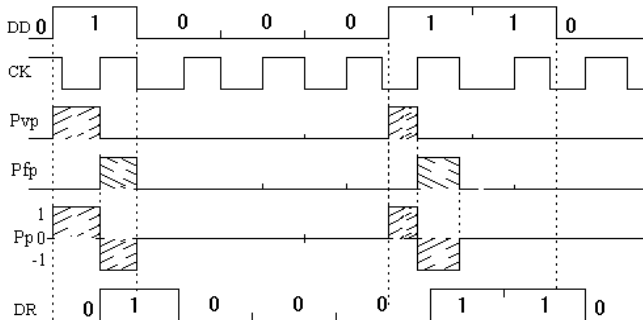


Figure 13. Waveforms of the asynchronous positive at rate automatic

The error pulse  $P_e$  does not disappear, but the variable area  $P_v$  is equal to the fixed  $P_f$  at the equilibrium point.

**V. DESIGN, TESTS AND RESULTS**

We present the design, tests and results of the various synchronizers [5].

**A. Design**

To have guaranteed results, is necessary to dimension all the synchronizers with equal conditions. Then, the loop gain  $K_l=K_dK_o=K_aK_fK_o$  must be equal in all the synchronizers. The phase detector gain  $K_f$  and the VCO gain  $K_o$  are fixed. Then, the loop gain amplification  $K_a$  controls the root locus and consequently the loop characteristics.

For analysis facilities, we use normalized values for the transmission rate  $t_x=1$ baud, clock frequency  $f_{CK}=1$ Hz, extern noise bandwidth  $B_n=5$ Hz and loop noise bandwidth  $B_l=0.002$ Hz. Then, we apply a signal power  $P_s= A_{ef}^2$  and a noise power  $P_n= N_o= 2\sigma_n^2 \Delta\tau$ , where  $\sigma_n$  is the noise standard deviation and  $\Delta\tau = 1/f_{Samp}$  is the sampling period. The relation between SNR and noise variance  $\sigma_n^2$  is

$$SNR= A_{ef}^2/(N_o.B_n) = 0.5^2/(2\sigma_n^2*10^{-3}*5)= 25/\sigma_n^2 \quad (1)$$

Now, for each synchronizer, is necessary to measure the output jitter  $U_{IRMS}$  versus the input SNR

- 1<sup>st</sup> order loop:

We use a cutoff loop filter  $F(s) = 0.5$ Hz, is 25 times greater than  $B_l= 0.002$ Hz, what eliminates the high frequency but maintain the loop characteristics. The transfer function is

$$H(s)= \frac{G(s)}{1+G(s)} = \frac{K_dK_oF(s)}{s+K_dK_oF(s)} = \frac{K_dK_o}{s+K_dK_o} \quad (2)$$

the loop noise bandwidth is

$$B_l = \frac{K_dK_o}{4} = K_a \frac{K_fK_o}{4} = 0.02Hz \quad (3)$$

So, with ( $K_m=1, A=1/2, B=1/2, K_o=2\pi$ ) and loop bandwidth  $B_l=0.002$ , we obtain respectively the  $K_a$ , for analog, hybrid, combinational and sequential synchronizers, then

$$B_l=(K_a.K_f.K_o)/4 = (K_a.K_m.A.B.K_o)/4 \rightarrow K_a=0.08*2/\pi \quad (4)$$

$$B_l=(K_a.K_f.K_o)/4 = (K_a.K_m.A.B.K_o)/4 \rightarrow K_a=0.08*2.2/\pi \quad (5)$$

$$B_l=(K_a.K_f.K_o)/4 = (K_a*1/\pi*2\pi)/4 \rightarrow K_a=0.04 \quad (6)$$

$$B_l=(K_a.K_f.K_o)/4 = (K_a*1/2\pi*2\pi)/4 \rightarrow K_a=0.08 \quad (7)$$

For the analog PLL, the jitter is

$$\sigma_\phi^2=B_l.N_o/A_{ef}^2=0.02*10^{-3}*2\sigma_n^2/0.5^2=16*10^{-5}.\sigma_n^2 \quad (8)$$

For the others PLLs, the jitter formula is more complicated.

- 2<sup>nd</sup> order loop:

Is not used here, but provides similar results.

**B. Tests**

We used the following setup to test synchronizers (Fig. 14)

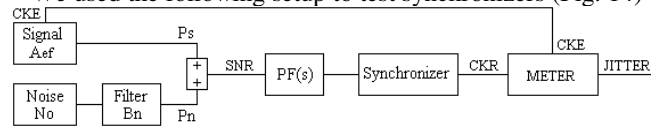


Figure 14. Blocks diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock, the difference is the jitter.

### C. Results

We present the results in terms of output jitter UIRMS versus input SNR. Fig. 15 shows the jitter - SNR curves of the four synchronizers which are the both manual (ab-m), the both automatic (ab-a), the positive manual (ap-m) and the positive automatic (ap-a).

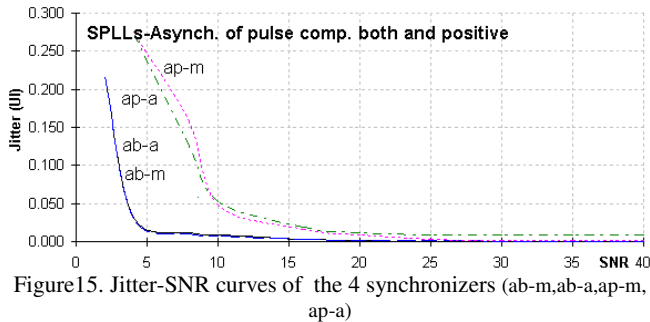


Figure 15. Jitter-SNR curves of the 4 synchronizers (ab-m, ab-a, ap-m, ap-a)

We observe that, in general, the output jitter UIRMS decreases gradually with the input SNR increasing.

We verify that, for high SNR, the four jitter curves tend to be similar. However, for low SNR, the variant asynchronous both at rate manual (ab-m) and automatic (ab-a) are better than the variant asynchronous positive at rate manual (ap-m) and automatic (ap-a).

### V. CONCLUSION AND FUTURE WORK

We studied four synchronizers involving the reference variant asynchronous by both transitions at rate with versions manual (ab-m) and automatic (ab-a) and the proposed variant asynchronous by positive transitions at rate with versions manual (ap-m) and automatic (ap-a). Then, we tested and compared their jitter - SNR curves.

We observed that, in general, the output UIRMS jitter curves decrease gradually with the input SNR increasing.

We verified that, for high SNR, the four synchronizers jitter curves tend to be similar, this is comprehensible since all the synchronizers are digital, with equal noise margin. However, for low SNR, the variant asynchronous by both at rate with its versions manual (ab-m) and automatic (ab-a) is better than the variant asynchronous by positive at rate with its versions manual (ap-m) and automatic (ap-a), this is comprehensible because the variant by both transitions has more transitions (double) than the variant by positive transitions and then, the going time from the error state to the correct state is lesser.

In the future, we are planning to extend the present study to other types of synchronizers.

### ACKNOWLEDGMENT

The authors are grateful to the program FCT (Foundation for sScience and Technology) / POCI2010.

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