Prefilter Bandwidth Effects in Asynchronous Sequential Symbol Synchronizers based on Pulse Comparison by Positive Transitions at Bit Rate

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***Abstract*- This work studies the prefilter bandwidth effects in four asynchronous sequential symbol synchronizers. We consider three prefilter bandwidths namely B1=∞, B2=2.tx and B3=1.tx, where tx is the bit rate. The synchronizer has two variants one asynchronous by both transitions at rate and other asynchronous by positive transitions at rate. Each variant has two versions namely the manual and the automatic. The objective is to study the prefilter with the four synchronizers and to evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal Noise Ratio).**

Keywords - Prefilter; Synchronizers; Communication systems.

I. INTRODUCTION

This work studies the prefilter bandwidth effects on the jitter-SNR behavior of four sequential symbol synchronizers.

The prefilter, applied before the synchronizer, switches their bandwidth between three values namely first B1=∞, after B2=2.tx and next B3=1.tx, where tx is the bit rate.

The synchronizer has four versions supported in two variants, one asynchronous by both transitions at rate with versions manual (ab-m) and automatic (ab-a) and other asynchronous by positive transitions at rate with versions manual (ap-m) and automatic (ap-a) [1, 2, 3, 4, 5, 6].

The difference between the four synchronizers is in the phase comparator. The clock is the VCO (Voltage Controlled Oscillator) that samples appropriately and retimes correctly the input data, guarantying good quality [7, 8, 9, 10, 11, 12].

Fig. 1 shows the prefilter followed of the synchronizer.

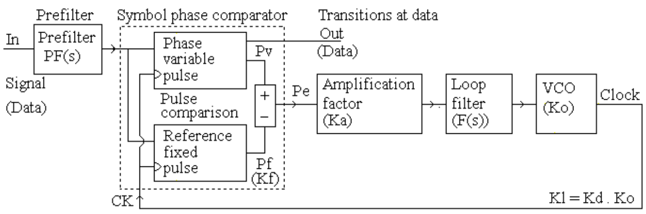

Figure 1. Prefilter with synchronizer based on pulse comparison

PF(s) is the prefilter (low pass). The synchronizer has various blocks, namely Kf is the phase detector gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the loop gain factor that controls the root locus and loop characteristics.

Following, we present the prefilter with their three different decreasing bandwidths (B1=∞, B2=2.tx, B3=1.tx).

After, we present the standard reference variant, asynchronous sequential symbol synchronizers based on pulse comparison by both transitions at rate, with versions manual (ab-m) and automatic (ab-a).

Next, we present the new proposed variant, asynchronous sequential symbol synchronizers based on pulse comparison by positive transitions at rate, with versions manual(ap-m) and automatic (ap-a). After, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

II. ART STATE, PROBLEMS AND SOLUTION

In the past art state was developed various synchronizers, but now is necessary to study their performance.

Previously, we studied the prefilter effects in synchronous synchronizers, the actual motivation is to study the prefilter but in asynchronous synchronizers [1, 2, 3, 4, 5].

The problem is that the jitter increases with the noise. So, to solve this problem, we propose a prefilter that attenuates the noise but however distorts slightly the signal [6, 7, 12].

II. PREFILTER BANDWIDTH EFFECTS

The prefilter, applied before the synchronizer, filters the noise but distorts slightly the signal. The prefilter bandwidth B switches between three values (B1=∞, B2=2.tx, B3=1.tx).

Fig. 2 shows the prefilter with their three bandwidths.

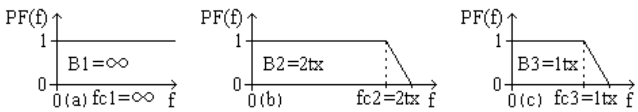

Figure 2. Three prefilter bandwidths: a) B1=∞; b) B2=2.tx; c) B3=1.tx

We will evaluate the three bandwidth effects (B1, B2, B3) on the jitter-SNR curves of the four symbol synchronizers.

a) Prefilter bandwidth equal infine (B1=∞): first (Fig.2a), we study this bandwidth effects.

b) Prefilter bandwidth equal two tx (B2=2.tx): second (Fig.2b), we study this bandwidth effects.

c) Prefilter bandwidth equal one tx (B3=1.tx): third (Fig.2c), we study this bandwidth effects.

III. REFERENCE BY BOTH AT RATE

The reference, asynchronous sequential symbol synchronizers based on pulse comparison operating by both transitions at bit rate has two versions which are the manual (ab-m) and the automatic (ab-a) [1, 2].

The versions difference is in the phase comparator, the variable pulse Pv is common but the fixed Pf is different.

A. Reference by both at rate manual (ab-m)

The block Pv, shown below, produces a variable pulse Pv between the input bits and VCO. The manual adjustment delay with Exor produces a manual fixed pulse Pf (Fig. 3).

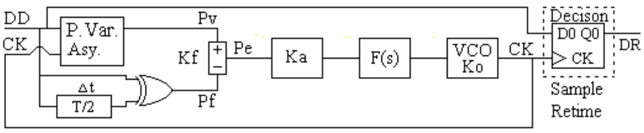

Figure 3. Asynchronous by both at rate and manual (ab-m)

The comparison between the pulses Pv and Pf provides the error pulse Pe that forces the VCO to synchronize the input. The block Pv is an asynchronous circuit (Fig.4).

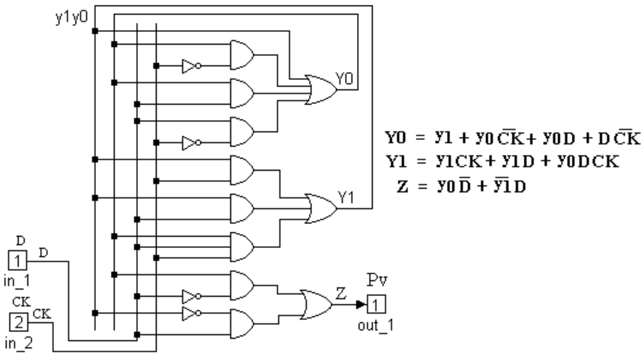

Figure 4. Intern aspect of the block Pv

The error pulse Pe diminishes during the synchronization time and disappear at the equilibrium point.

B. Reference by both at rate automatic (ab-a)

The block Pv, common with anterior, produces the variable pulse Pv between input and VCO. The block Pf, shown below, produces the comparison fixed pulse Pf (Fig. 5).

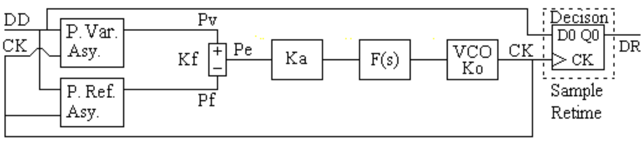

Figure 5. Asynchronous by both at rate and automatic (ab-a)

The comparison between the pulses Pv and Pf provides the error pulse Pe that forces the VCO to follow the input. The block Pf is an asynchronous circuit (Fig. 6).

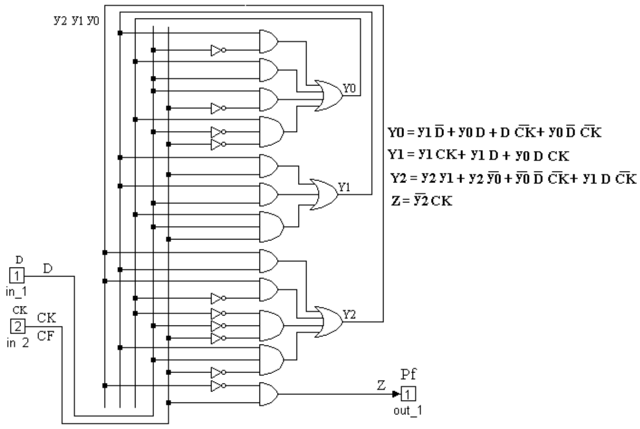

Figure 6. Intern aspect of the block Pf

The error pulse Pe does not disappear, but the variable area Pv is equal to the fixed Pf at the equilibrium point.

IV. PROPOSED BY POSITIVE AT RATE

The proposed, asynchronous sequential symbol synchronizers based on pulse comparison operating by positive transitions at bit rate has also two versions namely the manual (ap-m) and the automatic (ap-a) [3, 4].

The versions difference is in the phase comparator, the variable pulse Pvp is common but the fixed Pfp is different.

A. Proposed by positive at rate manual (ap-m)

The block Pvp produces the variable pulse Pvp between input positive transitions and VCO. The manual adjustment delay T/2 with AND produces a fixed pulse Pfp (Fig. 7).

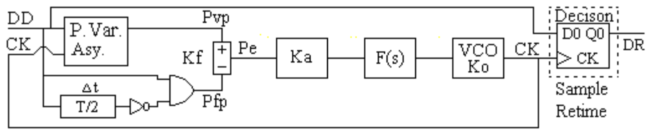

Figure7. Asynchronous by positive at rate and manual (ap-m)

The comparison between pulses Pvp and Pfp provides the error pulse Pe that forces the VCO to synchronize the input. The block Pvp is an asynchronous circuit (Fig. 8).

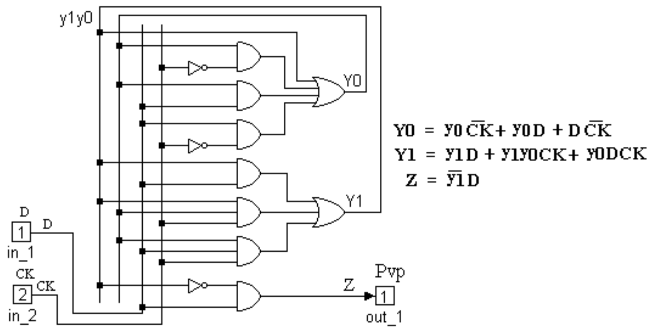

Figure 8. Intern aspect of the block Pvp

The error pulse Pe diminishes during the synchronization time and disappear at the equilibrium point.

B. Proposed by positive at rate automatic (ap-a)

The block Pvp, common, produces the variable pulse Pvp between input and VCO. The block Pfp, shown below, produces the comparison fixed pulse Pfp (Fig. 9).

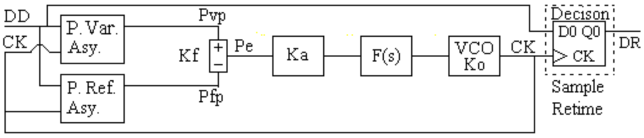

Figure 9 Asynchronous by positive at rate and automatic (ap-a)

The comparison between the pulses Pvp and Pfp provides the error pulse Pe that forces the VCO to follow the input. The block Pfp is an asynchronous circuit (Fig. 10).

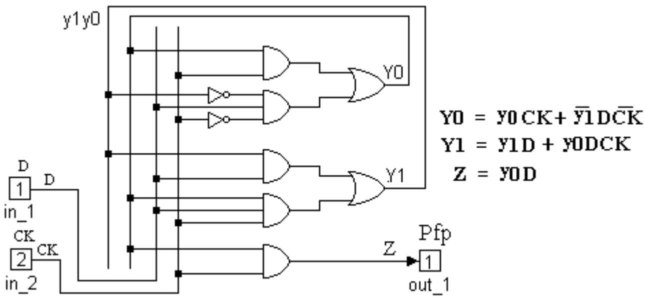

Figure 10. Intern aspect of the block Pfp

The error pulse Pe does not disappear at the equilibrium point, but the variable area Pv becomes equal to the fixed Pf.

V. DESIGN, TESTS AND RESULTS

We present the design, tests and results of the various synchronizers [5].

A. Design

To get guaranteed results, is necessary to dimension all the synchronizers with equal conditions. Then, the loop gain Kl=KdKo=KaKfKo must be equal in all the synchronizers. The phase detector gain Kf and the VCO gain Ko are fixed. Then, the loop gain amplification Ka controls the root locus and consequently the loop characteristics.

For analysis facilities, we use normalized values for the bit rate tx=1baud, clock frequency fCK=1Hz, extern noise bandwidth Bn=5Hz and loop noise bandwidth Bl=0.002Hz. Then, we apply a signal power Ps= A^2_{ef} and a noise power Pn= No= $2\sigma n^2.\Delta\tau$, where σn is the noise standard deviation and $\Delta\tau$ =1/fSamp is the sampling period. The relation between SNR and noise variance σn^2 is

$$SNR= A^2_{ef}/(No.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2 \quad (1)$$

Now, for each synchronizer, is necessary to measure the output jitter UIRMS versus input SNR

- 1^{st} order loop:

The used cutoff loop filter F(s)=0.5Hz, is 25 times greater than Bl= 0.002Hz, what eliminates the high frequency but maintain the loop characteristics. The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (2)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (3)$$

So, with (Km=1, A=1/2, B=1/2, Ko=2π) and loop bandwidth Bl=0.002, we obtain respectively the Ka, for analog, hybrid, combinational and sequential synchronizers, then

$$Bl=(Ka.Kf.Ko)/4 = (Ka.Km.A.B.Ko)/4 \to Ka=0.08*2/\pi \quad (4)$$

$$Bl=(Ka.Kf.Ko)/4 = (Ka.Km.A.B.Ko)/4 \to Ka=0.08*2.2/\pi \quad (5)$$

$$Bl=(Ka.Kf.Ko)/4 = (Ka*1/\pi*2\pi)/4 \to Ka=0.04 \quad (6)$$

$$Bl=(Ka.Kf.Ko)/4 = (Ka*1/2\pi*2\pi)/4 \to Ka=0.08 \quad (7)$$

For the analog PLL, the jitter is

$$\sigma_\phi^2=Bl.No/Aef^2=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2 \quad (8)$$

For the others PLLs, the jitter formula is more complicated.

- 2^{nd} order loop:

Is not used here, but provides similar results.

B. Tests

We used the following setup to test synchronizers (Fig. 11)

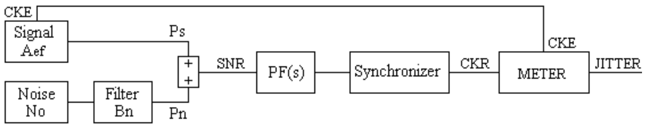

Figure 11. Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock, the difference is the jitter.

C. Results

We will present the results, in terms of jitter - SNR, for each prefilter bandwidth with the four synchronizers.

Fig. 12 shows the jitter-SNR curves for the prefilter bandwidth B1=∞ with the four synchronizers (ab-m, ab-a, ap-m, ap-a).

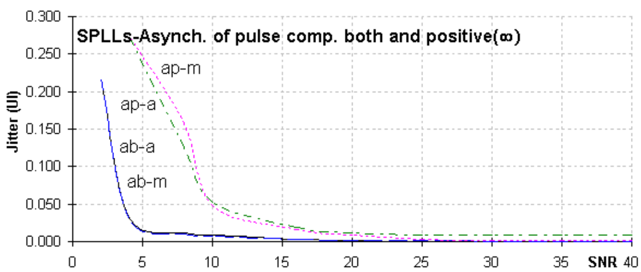

Figure 12. Jitter-SNR curves of B1+4synchronizers (ab-m, ab-a, ap-m, ap-a)

For prefilter B1=∞, we verify that, for high SNR, the four synchronizer jitter-SNR curves tend to be similar. However, for low SNR, the variant asynchronous by both at rate with versions manual (ab-m) and automatic (ab-a) are better than the variant asynchronous by positive at rate with versions manual (ap-m) and automatic (ap-a).

Fig. 13 shows the jitter-SNR curves for the prefilter bandwidth B2=2.tx with the four synchronizers (ab-m, ab-a, ap-m, ap-a).

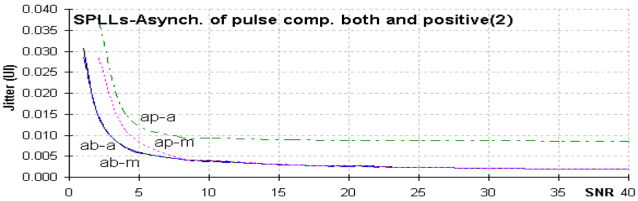

Figure 13. Jitter-SNR curves of B2+4synchronizers (ab-m, ab-a, ap-m, ap-a)

For prefilter B2=2.tx, we verify that, it becomes the jitter-SNR curves more similar between themselves. For high SNR, it degrades slightly the jitter-SNR curves. However, for low SNR it benefits significantly the jitter - SNR curves.

Fig. 14 shows the jitter-SNR curves for the prefilter bandwidth B3=1.tx with the four synchronizers (ab-m, ab-a, ap-m, ap-a).

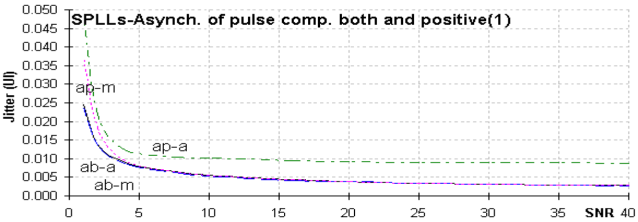

Figure 14. Jitter-SNR curves of B3+4synchronizers (ab-m, ab-a, ap-m, ap-a)

For prefilter B3=1.tx, we verify that, it becomes the jitter-SNR curves still more similar between themselves. For high SNR, it harms more the jitter-SNR curves. However, for low SNR, it benefits less the jitter-SNR curves.

VI. CONCLUSION AND FUTURE WORK

We studied three prefilter bandwidths (B1=∞, B2=2.tx, B3=1.tx) with four synchronizers, one variant asynchronous by both transitions at rate with versions manual (ab-m) and automatic (ab-a) and other variant asynchronous by positive at rate with versions manual (ap-m) and automatic (ap-a). Then, we measured their jitter - SNR curves.

We observed that, in general, the output jitter curves decreases gradually with the input SNR increasing.

For prefilter B1=∞ (greater), we verified that, for high SNR, the four synchronizers jitter curves tend to be similar, this is comprehensible since all the synchronizers are digital and have similar noise margin. However, for low SNR, the variant asynchronous by both at rate with its versions manual (ab-m) and automatic (ab-a) is better than the variant asynchronous by positive at rate with its versions manual (ap-m) and automatic (ap-a), this is comprehensible because the variant by both transitions has more transitions (double) than the variant by positive transitions and then, the going time from the error state to the correct state is lesser.

For prefilter B_2=2.tx(medium), we verified that, it becomes the jitter-SNR curves more similar between themselves. For high SNR, it degrades slightly the jitter-snr curves. However, for low SNR, it benefits significantly the jitter-SNR curves.

For prefilter B3=1.tx (minor), we verify that, it becomes the jitter-SNR curves still more similar between themselves. For high SNR, it degrades more the jitter-SNR curves. Also, for low SNR, it benefits less the jitter-SNR curves.

So, the prefilter, for high SNR, distorts the signal what is prejudicial, for low SNR, attenuates noise what is beneficial.

In the future, we are planning to extend the present study to other types of synchronizers.

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REFERENCES

[1] Jean C. Imbeaux, “performance of the delay-line multiplier circuit for clock and carrier synchronization in Digital Satellite Communications”, IEEE Journal on Selected Areas in Communications pp. 82-95 Jan. 1983.

[2] Werner Rosenkranz, “Phase Locked Loops with limiter phase detectors in the presence of noise”, IEEE Transactions on Communications com-30 Nº10 pp. 2297-2304. Oct 1982.

[3] Hans H. Witte, “A Simple Clock Extraction Circuit Using a Self Sustaining Monostable Multivibrator Output Signal”, Electronics Letters, Vol.19, Is.21, pp. 897-898, Oct 1983.

[4] Charles R. Hogge, “A Self Correcting Clock Recovery Circuit”, IEEE Transactions on Electron Devices pp. 2704-2706 Dec 1985.

[5] Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro and Jose P. Carvalho “A New Technique to Measure the Jitter”, Proc. III Conf. on Telecommunications pp. 64-67 FFoz-PT 23-24 Apr 2001.

[6] Marvin K. Simon and William C. Lindsey, “Tracking Performance of Symbol Synchronizers for Manchester Coded Data”, IEEE Transactions on Communications Vol. com-2.5 Nº4, pp. 393-408, April 1977.

[7] Jeffrey B. Carruthers, D. D. Falconer, H. M. Sandler and L. Strawczynski, “Bit Synchronization in the Presence of Co-Channel Interference”, Proc. Conf. on Electrical and Computer Engineering pp. 4.1.1-4.1.7, Ottawa-CA 3-6 Sep. 1990.

[8] Johannes Huber and Weilin Liu “Data-Aided Synchronization of Coherent CPM-Receivers” IEEE Transactions on Communications Vol.40 Nº1, pp. 178-189, Jan. 1992.

[9] Antonio A. D’Amico, Aldo N. D’Andrea and Ruggero Reggianni, “Efficient Non-Data-Aided Carrier and Clock Recovery for Satellite DVB at Very Low SNR”, IEEE Jou. on Sattelite Areas in Comm. Vol.19 Nº12 pp. 2320-2330, Dec. 2001.

[10] Rostislav Dobkin, Ran Ginosar and Christos P. Sotiriou “Data Synchronization Issues in GALS SoCs”, Proc. 10th International Symposium on Asynchronous Circuits and Systems, pp. CD-Ed., Crete-Greece 19-23 Apr. 2004.

[11] N. Noels, H. Steendam and M. Moeneclaey, “Effectiveness Study of Code-Aided and Non-Code-Aided ML-Based Feedback Phase Synchronizers”, Proc. IEEE Intern. Conference on Communications (ICC’06) pp. 2946-2951, Istambul-TK, 11-15 Jun 2006.

[12] Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro and Jose P. Carvalho “Carrier Phase Lock Loop and Bit Phase Lock Loop”, Proc. IX Symposium on Enabling Optical Network and Sensors (SEONs) pp. CD-Edited, Aveiro-PT 1-1 July 2011.