Design for a UWB Down-Conversion Mixer for Multi-Band Applications

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Abstract*—In this paper, a CMOS down-conversion mixer for UWB applications is presented. The mixer circuit is designed using a VIS 0.25µm RF CMOS technology, working at the 0.9GHz-10.6GHz frequency range; it will be used in applications such as IEEE WiFi, GSM and WiMAX. The core of the mixer has been designed based on double-balanced cell architecture, and uses the current bleeding method to increase the linearity and improve the conversion gain. We put a resistor on the drain of the MOS between two RF inputs, which will improve the flatness of conversion gain. Regarding the arrangement of the mixer, the RF frequency is set at 0.9GHz-10.6GHz, the LO frequency 0.8GHz-10.5GHz and the IF of 100MHz. The simulated conversion gain of the mixer is 7± 1dB. The 1dB compression point is higher than -11dBm at high frequency and -9dBm at low frequency. The RF input return loss is well below -11dB, and the LO input return loss is below -10dB. The noise figure is 12.93dB while IF is 100MHz, and the mixer core dissipates 9.8mW under a 1.8 V supply.

Keywords-UWB; Down Conversion; CMOS

I. INTRODUCTION

The requirements of wireless communication systems have been increasing rapidly over the last few decades. Higher speed transportation, lower power consumption, low cost and operating on multi-band have been very important considerations in wireless development [1]. The new design technique for ultra wide-band wireless communications must be carried out with future high-precision applications in mind. Wireless Fidelity (Wi-Fi), worldwide Interoperability for Microwave Access (WiMAX) [2-5] and Global Systems for Mobile Communications (GSM) are very common in modern life. A lot of mobile devices, like personal computers, mobile phones, and digital music players can be connected to Wi-Fi networks, but only within a limited area.

WiMAX is a form of wireless communication; its standard is known as IEEE 802.16x. The area of WiMAX is very large and can be used within entire residential districts, remote areas, or in SOHO internets. Its application will benefit the mobility of individuals, families and companies.

GSM is the most popular standard of mobile phones. By Q4 2012, over 3.2 billion people were using GSM technology [6] and the world market share of GSM is over 80% [7].

In this work, a 0.9GHz~10.6GHz ultra wide band (UWB) down conversion mixer was designed for use in a variety of applications, such as Wi-Fi, WiMAX and GSM. However, the linearity and noise figures of a mixer should be continuously improved for future high-sensitivity applications. In Section II, the circuit design aspect is described. Section III includes post-simulation results, and conclusions are presented in Section IV.

II. CIRCUIT DESIGN

This circuit uses the process of standard complementary metal oxide semiconductor (CMOS) 0.25µm 1P5M technology, and we used Advanced Design System (ADS) requirements to simulate the circuit. The Radio Frequency (RF) input frequency was between 0.9GHz and10.6GHz, and the Local Oscillator (LO) input frequency was set between 0.8GHz and 10.5GHz. The Intermediate Frequency (IF) output frequency was 100MHz. The Gilbert structure [8] was modified to complete this circuit, and improve it over a double-balanced mixer. Figure 1 shows the whole circuit diagram.

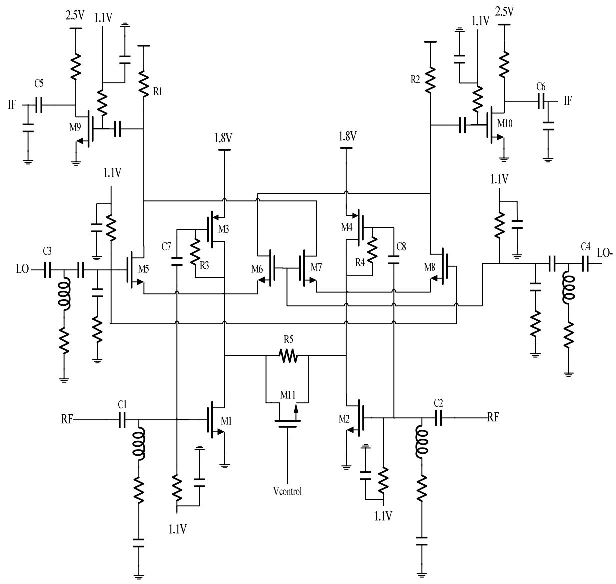


Figure 1. Down-Conversion Mixer

As shown in Figure 1, LO stages of transistors from M5 to M8 are designed using MOS switches. M1 and M2 are operated on the saturation region to act as conductors and to permit RF signals to go through the gate and become current signals. M3 and M4 act as the paths of current bleedings to make more current flow into M1 and M2, thereby increasing the conversion gain and reducing noise. R3 and R4 block the signals into M3 and M4, and can also act as the self-bias voltages of M3 and M4. C7 and C8 prevent the bias voltages and allow the signals to go through them to M3 and M4. If this is the case, M3 and M4 can not only provide the paths for current bleeding but can also amplify the signals. Capacitors from C1 to C6 act as DC blocks, and a common source amplifier is implemented to be the IF output buffer.

The flatness of conversion gain is also very important to the UWB mixer, so a resistor is embedded between the drains of M1 and M2. Figure 2 shows that C7, R3 and R5 combine to form a high pass filter, as shown in Figure 3. This decreases the gain of low frequency to improve the flatness of conversion gain, as shown in Figure 4. The conversion gain can be sacrificed to improve flatness.

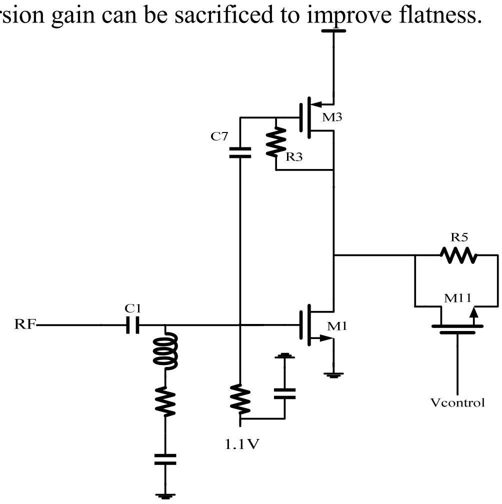


Figure 2. The Relationship among C7, R3, and R5

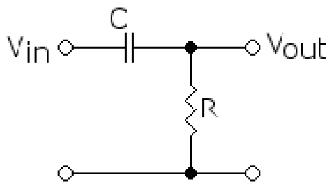


Figure 3: High-Pass Filter

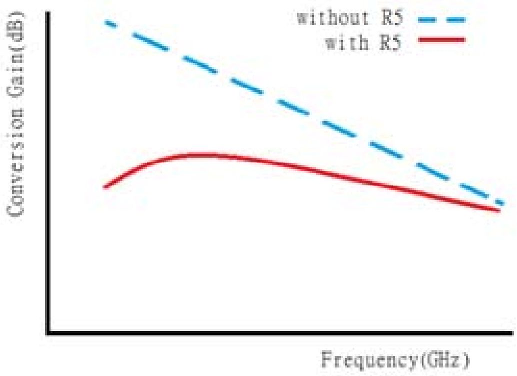


Figure 4. The Change in Flatness of Conversion Gain

III. SIMULATIONS AND RESULTS

Figures 5 to 11 depict the post-simulation result using ADS software. The supply voltage and power consumption are 1.8V and 18.3mW, respectively. The maximum conversion gain of the mixer was simulated at 8.8 dB at a frequency of 2.9 GHz, while the minimum was 5.7 dB at 10.6 GHz, and an average of 7.25 dB over the band. A plot of the conversion gain versus frequency is shown in Figure 5. Figures 6 and 7 show RF and LO input matching, since it is a UWB mixer and the return loss is less than 8dB. Figure 8 represents P-1dB, with three frequencies chosen for simulation. The results range from about -8.5 to -11dBm.

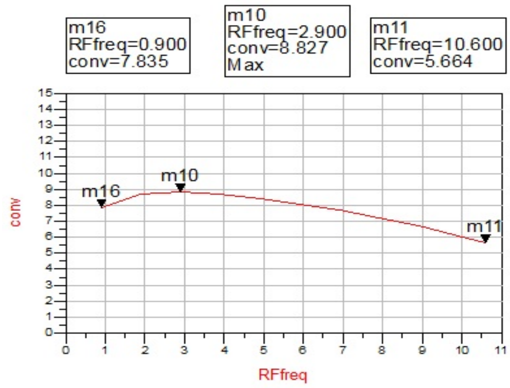


Figure 5. The Conversion Gain of 0.9~10.6GHz

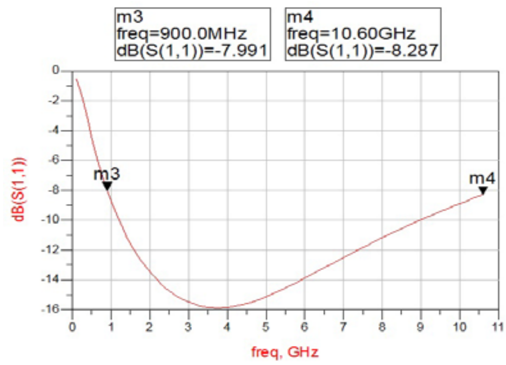


Figure 6. RF Input Return Loss

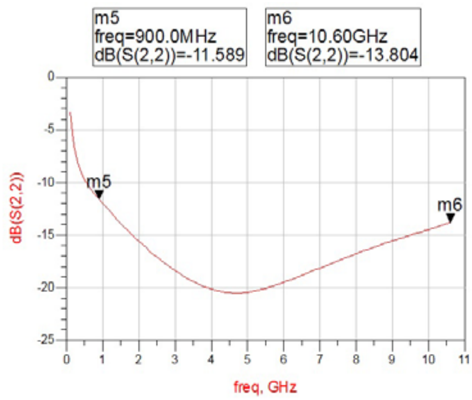
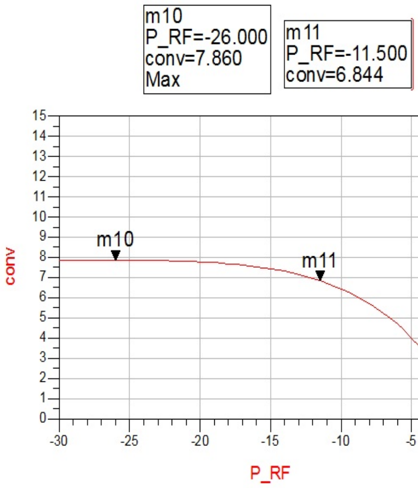
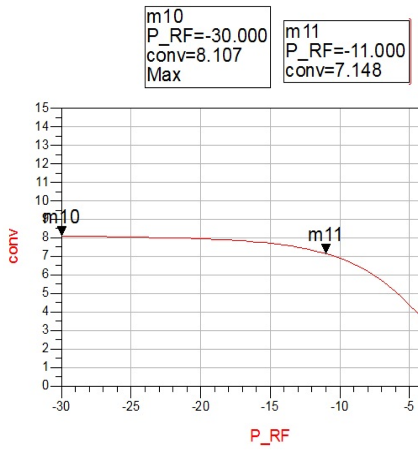


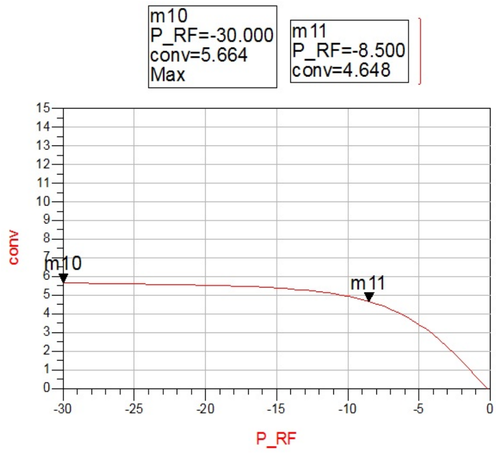
Figure 7. LO Input Return Loss



(a) 0.9GHz



(b) 5.8GHz



(c) 10.6GHz

Figure 8. 1dB Compression Point

Figure 9 shows the DSB noise figure of the mixer; the variation is very small, ranging between 0.9 and 10.6GHz.

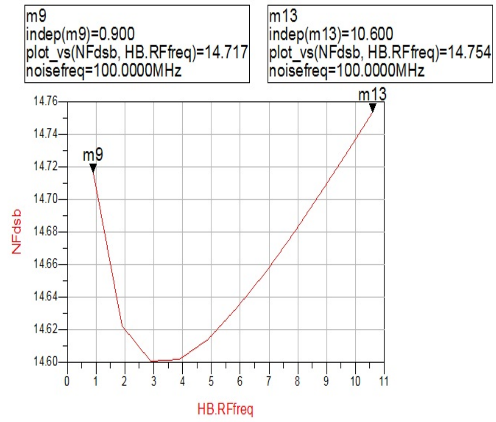
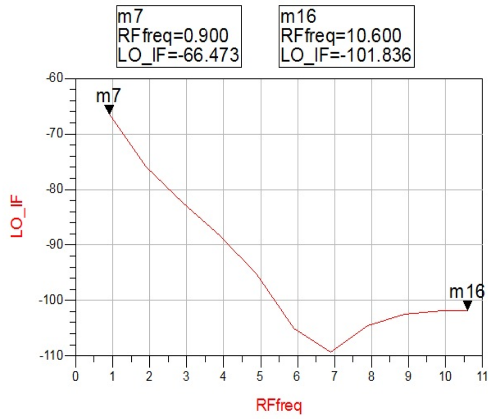
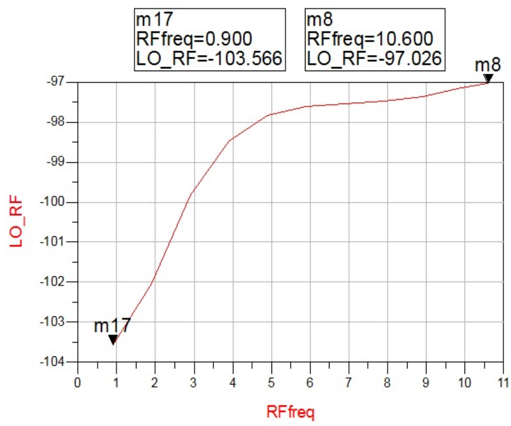


Figure 9. Noise Figure

Figure 10 shows the isolation of LO to IF and LO to RF. Since we used the double-balanced structure, isolation is very good.



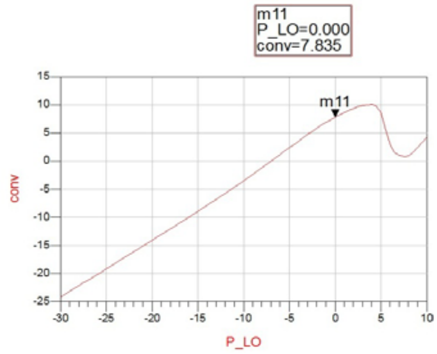
(a)



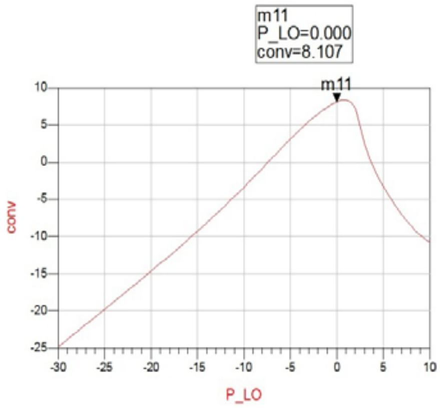
(b)

Figure 10. Isolation (a) LO to IF and (b)LO to RF

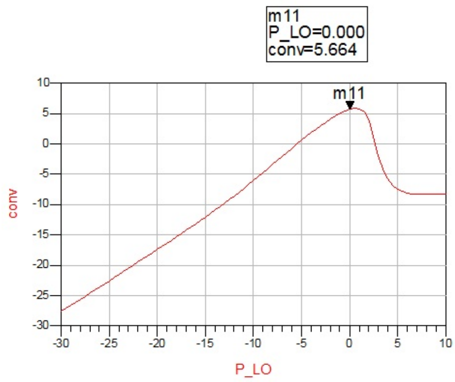
Figure 11 shows the relationship of LO power and conversion gain. LO power was set at 0dBm in the simulation; we can see that the results are actually located at 0dBm and the support LO power range is down to -5dBm.



(a)0.9GHz



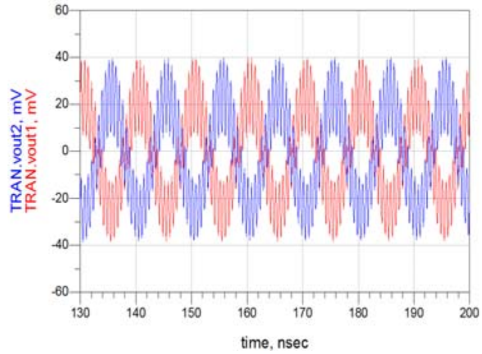
(b)5.8GHz



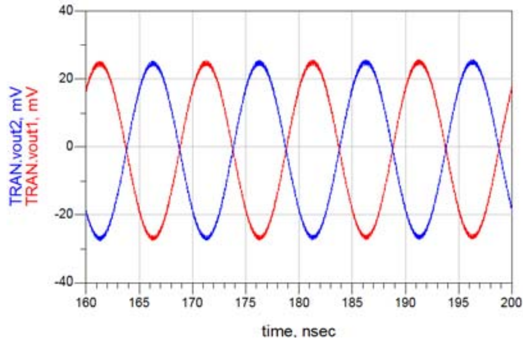
(c)10.6GHz

Figure 11. The Relationship of LO Power with Conversion Gain

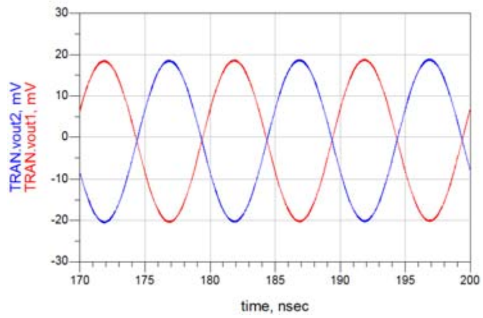
Figure 12 shows the symmetrical waveforms from the mixer output at different operating frequencies. Using the simulated output signal of the proposed mixer, we are able to obtain the base band signal with a peak-to-peak value of approximately 50mV.



(a)0.9GHz



(b)5.8GHz



(c)10.6GHz

Figure 12. The Output Waveform Diagram

The layout of this circuit is shown in Figure 13, and will be fabricated in a VIS 0.25μm RF CMOS process. The total area of the chip is less than 1.33 mm^2. As observed, there are two pairs of on-chip spiral inductors in this design. Their values have been selected to be as small as possible, so that first-order parameters: inductance and resistance remain almost unchanged within the operating frequency.

The performance of the proposed wideband mixer and a comparison with other existing mixers [9-11] around the same frequency range are summarized in Table II. The advantage of the proposed mixer represents excellent properties of linearity and low noise figures.

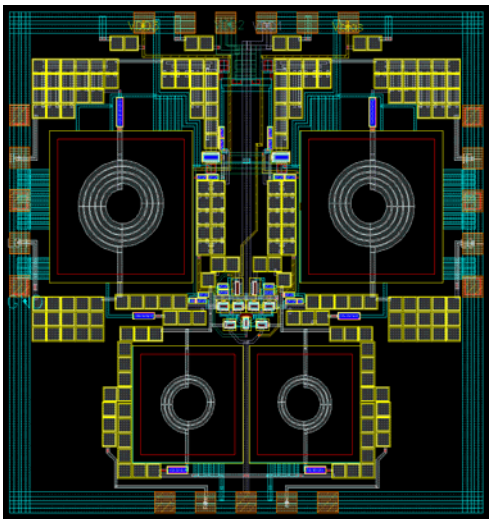


Figure 13. Mixer Layout

Table I lists the comparison of pre-simulation and post-simulation using 0.25 μm CMOS technology..

TABLE I. COMPARISON OF PRE-SIM AND POST-SIM

Specifications	Pre-Sim.	Post-Sim.
Power Supply (V)	1/1.8/2.5	
Current (mA)	10.3	
Power Dissipation (mW)	18.54	
Frequency Range (GHz)	0.9~10.6	
Conversion Gain (dB)	6~8.7	5.7~8.8
DSB Noise Figure (dB)	14.57~14.75	14.6~14.76
RF Return Loss (dB)	<-7	<-7
LO Return Loss (dB)	<-11	<-11
LO-RF Isolation (dB)	<-60	<-60
LO-IF Isolation (dB)	<-97	<-97
P-1dB (dBm)	-10	-10
Chip Area (mm)	1.16*1.149	

TABLE II. COMPARISON WITH PREVIOUS WORK

	This work	[9]	[10]	[11]
Process (um)	0.25	0.18	0.13	0.13
Power Supply (V)	1.8	1.8	1.2	1.2
Frequency (GHz)	0.9~10.6	3.1~4.8	3~7	0.7~6
Conversion Gain (dB)	6~8.7	9~11.5	5.3~8.2	5~7
Noise Figure (dB)	14.57	10.8~13.2	9.6~13.5	11~13.2
Power Dissipation (mW)	18.54	11.3	5.8	5.8
Chip Area (mm)	1.16*1.15	0.74*0.4	0.36*0.38	0.86*0.75

IV. CONCLUSION AND FUTURE WORK

This UWB down-conversion mixer combines the advantages of the current-bleeding technique and a variable MOS-resistor with the VIS process of CMOS 0.25μm 1P5M. We used the technique of current bleeding and put a resistor between the drains of the RF input conductors to benefit the flatness of conversion gain. Since there are four different supply voltages, it was necessary to reduce the number of voltages to achieve lower cost. Combining these techniques with the use of a wideband low noise amplifier and voltage controlled oscillator to act as a SOC chip is our ultimate goal.

ACKNOWLEDGMENT

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