Efficient ASIC Design of Digital Down Converter for Mobile Applications

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Abstract— **This paper presents ASIC design of digital down converter using 90nm technology for software defined applications. Computationally efficient multistage design technique is used to provide optimized solution for Third Generation Mobile Communications. Parks McClellan algorithm is used to minimize the filter order along with efficient polyphase decomposition technique. Multiplier based partially serial algorithm is used to enhance the performance in terms of area and power consumption. Multipliers and adders are optimally placed and routed to reduce the silicon area. The proposed Digital Down Converter ASIC has consumed 601 mm^2 area by consuming 3169.607 nW power to provide high performance optimized solution to software defined radios.**

Keywords-3G mobile communication; asic; base stations; radio transceivers; reconfigurable logic.

I. INTRODUCTION

The highly competitive nature of the wireless communications market and constantly evolving communication standards have resulted in short design cycles and product lifetimes. The talking point is to provide area and power efficient integrated design for Digital Down Converter (DDC) for 3G Applications [1]. In the recent past, telecommunications techniques have achieved a wide popularity, mainly due to the huge diffusion of cellular phones and wireless devices. The request for more complex and complete services, such as high speed data transmission and multimedia content streaming, has moved many research groups in the electronic field towards the study of new and efficient algorithms, codes and modulations. In Software Defined Radios (SDR), most radio receiver processing functions to be run on a general purpose (GP) programmable processor rather than being implemented strictly on non programmable hardware. The functionality of SDR receiver processor can be changed via "software reprogramming." The concept of SDR is now an IEEE Standard, i.e., IEEE P1900 [2]. These radios are reconfigurable through software updates. For high end digital signal processing where the highest possible performance is needed at low power consumption, ASICs are still the processors of choice. However, ASICs are very expensive and require long time in design and development. ASICs are inherently rigid and unsuitable to the applications that are constantly evolving. For these reasons, Programmable Logic Devices like Field Programmable Gate Arrays (FPGAs) have been emerged as an alternative to ASICs in wireless communication systems. FPGAs are mainly used for the flexibility they provide. The FPGAs suffer from the drawbacks of inefficient resource utilization, high cost and power consumption [3]. The cost factor can be improved by using less expensive FPGAs for system design and by efficient utilization of FPGA resources. The power factor can be improved by optimal usage of SRAM which can be taken care during FPGA manufacturing by using various techniques [4].

ASIC is an integrated circuit that is used for a particular application. It is composed of series of circuits that are taken from the technology dependent library to generate gate – level net list to implement the required functionality [5]. ASICs provide an advantage of high speed as compared to other programmable devices like PLDs, PALs and FPGAs since they are designed to perform a specific task. ASICs can be made compact by incorporating significant amounts of circuitry onto a single chip, which results in minimum power utilization [6]. By reducing inter-package interconnections, ASICs help in reduction of noise. ASICs provide increased performance at relatively low power consumption and comparatively less area-delay product (ADP). Besides, it consumes less energy per sample (EPS) and gives cost effective and reliable solutions [7]. Hence, ASICs are mainly used to increase the performance and power efficiency of the circuits but inability to reconfigure is the major drawback associated with these devices. The FPGA based DDC design [1] is extended to DDC ASIC to improve the performance in terms of area and power. FPGA's though providing the advantage of flexibility still leads to improper utilization of resources. So, having an integrated solution, i.e., a dedicated ASIC design for the proposed DDC will lead to further reduction of resources in terms of area and power. This results in cost effective

solution for wireless communication applications.

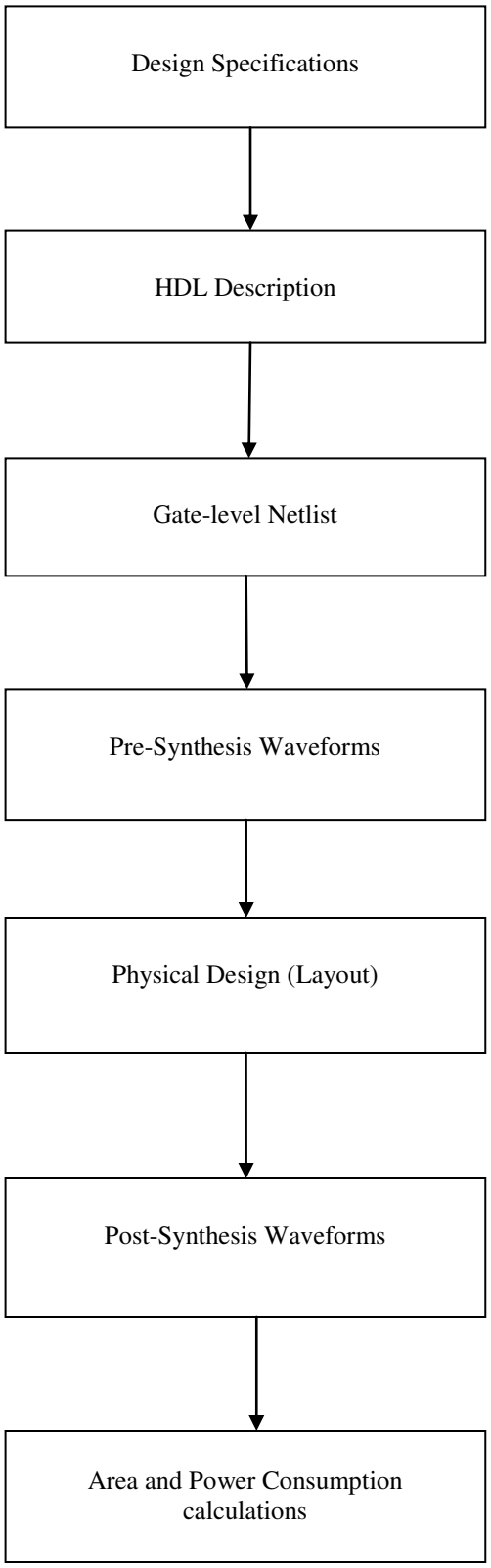

Figure 1. Flow Diagram of ASIC in Cadence

Figure 1 depicts the flow of ASIC in Cadence environment. In the present paper, the proposed design is implemented in technology dependent 90 nm foundry at 1.2 V. Firstly, the design is coded in Verilog hardware description language and then the gate level netlist is synthesized and the results are verified using pre-synthesis waveforms. Then the physical design implementation is done to find the total number of cells, area and power consumption and the results are verified using post-synthesis waveforms.

II. DIGITAL DOWN CONVERTER

The Software Defined Radio system can change its radio functions by swapping software instead of replacing hardware, seems to be the best solution given that mobile standards are springing up like mushrooms [8]. SDR thereby makes it possible to reprogram cell phones to operate on different radio interface standards. But that's not all. Putting much of a radio's functionality in software opens up other benefits. A mobile SDR device can cope with the unpredictable dynamic characteristics of highly variable wireless links [9]. SDRs use a single hardware front end but can change their frequency of operation, occupied bandwidth, and adherence to various wireless standards by calling various software algorithms. Such a solution allows inexpensive, efficient interoperability between the available standards and frequency bands [10]. Figure 2 illustrates SDR BS receiver that consists of two sections – a front-end high-data rate processing section and a back-end symbol rate or chip-rate processing section.

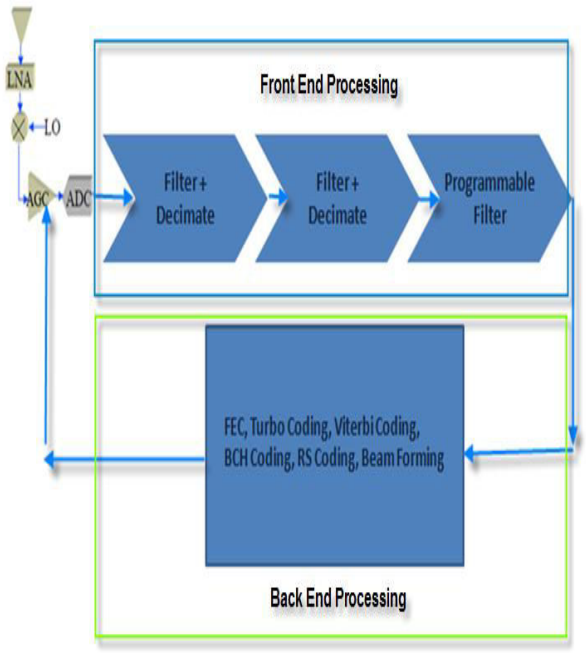

Figure 2. Reconfigurable SDR BS Receiver

Reconfigurable architectures provide flexible and integrated system-on-chip solutions that accommodate smooth migration from archaic to innovative designs, allowing recycling of hardware resources across multiple generations of the standards [11]. Software defined radio (SDR) technology enables such functionality in wireless devices by using a reconfigurable hardware platform across multiple standards. Sampling rate converters play important role in SDR systems [12]. Digital up-converters (DUCs) and digital down-converters (DDCs) are important components of every modern wireless base station design. DUCs are typically used in digital transmitters to filter up-sample and modulate signals from baseband to the carrier frequency [13]-[15]. DDCs, on the other hand, reside in the digital receivers to demodulate, filter, and down-sample the signal to baseband so that further processing on the received signal can be done at lower sampling frequencies. They are more popular than their analogue counterparts because of small size, low power consumption and accurate performance [16]-[22].

DDC performs decimation and matched filtering to remove adjacent channels and maximize the received signal-to-noise ratio (SNR) [23]. For the reference WCDMA DDC design, the carrier bandwidth is = 5.0 MHz, Number of carriers is = 1, IF sample rate is = 61.44 MSPS, DDC output rate 7.68 MSPS, Input precision is = 14 bits, Output precision is = 16 bits and Mixer resolution 0.25 Hz approximately and SFDR up to 115 dB is required. The DDC input is assumed to be real, directly coming from the ADC. The mixer translates the real band pass input signal from intermediate frequency to a complex baseband signal centred at 0 Hz. Mathematically, the real input signal is multiplied by a complex exponential as shown in Eq. (1) to produce a complex output signal with real and imaginary components Eq. (2) and Eq. (3) respectively. The sinusoidal waveforms required to perform the mixing process is obtained by using the Direct Digital Synthesizer (DDS). The decimators in the DDC need to down sample the IF data from 61.44 MHz back to 2x chip rate. The factor of 61.44/7.68 = 8 can be partitioned using different possible configurations. The down sampling by eight at once will result in an extremely long filter length and result in an inefficient hardware implementation. The use of shaping filter with decimation factor of 2 allows the remaining stages to be implemented as either one half band filter with decimation factor of 4 or two half band filters with decimation factor of 2 each. The second configuration is more suitable for hardware implementation because of less hardware consumption [24]-[26].

$$e^{-jw_o n} = \cos(w_o n) - j\sin(w_o n) \quad (1)$$

$$Y_r = X(n)\cos(w_o n) \quad (2)$$

$$Y_i = -X(n)\sin(w_o n) \quad (3)$$

III. DESIGN SPECIFICATIONS

An efficient DDC is designed for WCDMA Applications. The proposed DDC design is using three decimator stages. The input sample rate of first decimator is 61.44 MSPS, and the output sample rate is 30.72 MSPS. The pass band frequency is 2.34 MHz and the pass band ripple is 0.002 dB. It results in a digital filter of order 10 whose magnitude and phase response is shown in Figure 3.

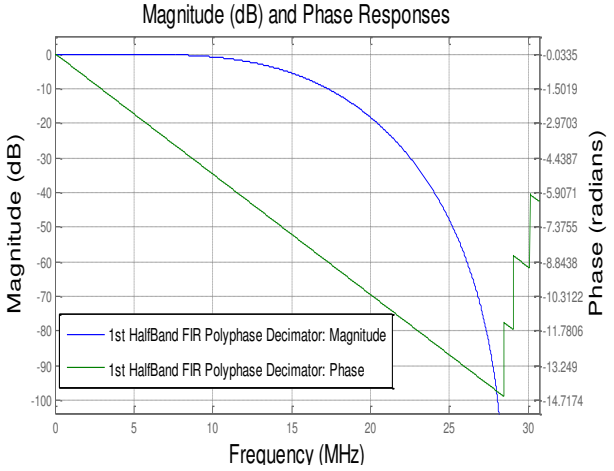

Figure 3. First Stage Half Band Decimator Response

The proposed partially serial pipelined MAC algorithm design technique based stage 1 decimator is shown in Figure 4. The 11 coefficients of first stage decimator have been processed by using 3 multipliers in partially serial style using MAC algorithm to optimize both speed and area factor simultaneously. The input pipeline registers are used to store the new coefficient values required for processing in the next cycle to further enhance the speed. The CE delays are used to make synchronization between stage 1 and stage 2.

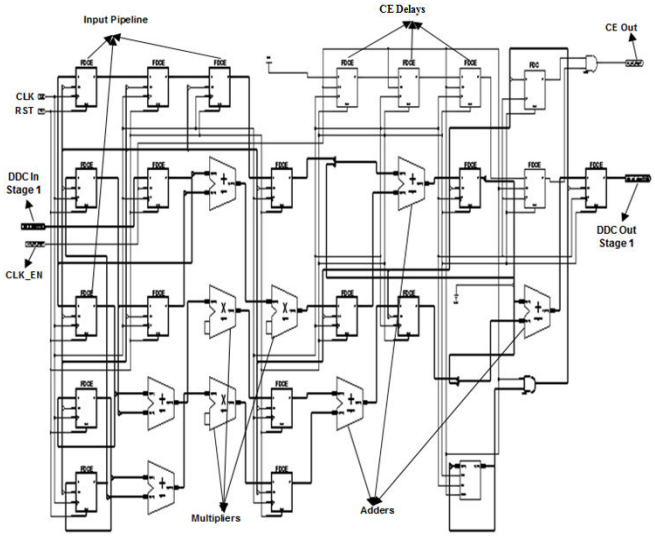

Figure 4. Stage 1 PSPMAC Based Decimator

The pass band edge of second decimator is 2.34 MHz and pass band ripple is 0.0001 dB. It results in digital filter with order 18 whose response is shown in Figure 5. The second stage decimator requires 27 coefficients for its hardware implementation.

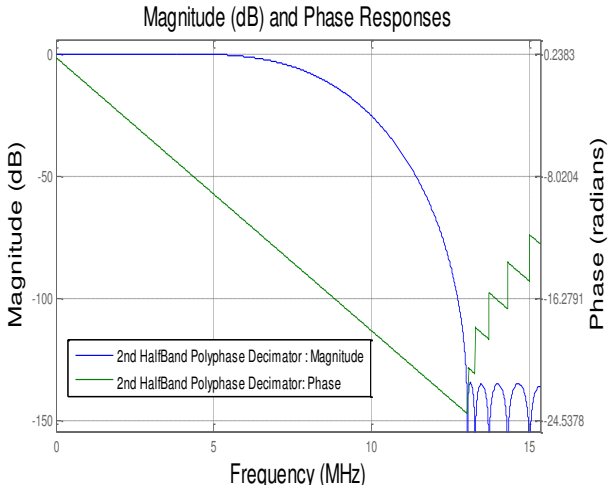

Figure 5. Second Stage Half Band Decimator Response

The second stage decimator requires 27 coefficients for its hardware implementation. To design the required decimator partially serial pipelined in partially serial pipelined MAC (PSPMAC) style 5 multipliers have been used as shown in Figure 6. The input pipeline registers are used to store the new coefficient values required for processing in the next cycle to enhance the speed further. The CE delays are used to make synchronization between stage 2 and stage 3.

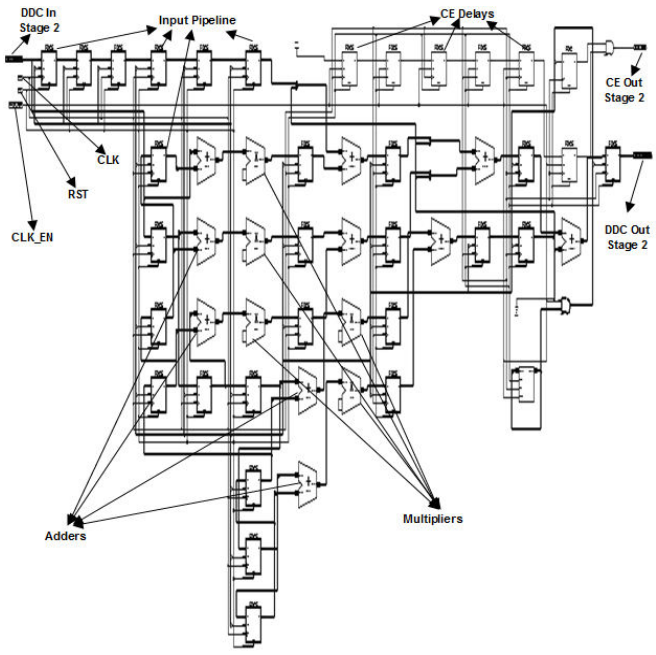

Figure 6. Stage 2 PSPMAC Based Decimator

The next stage RRC filter is used for sampling rate conversion from 15.36 MSPS to 7.68 MSPS. This 2x over-sampling rate is needed in the timing recovery process to avoid the signal loss due to the sampling point misalignment. The response of the filter is shown in Figure 7.

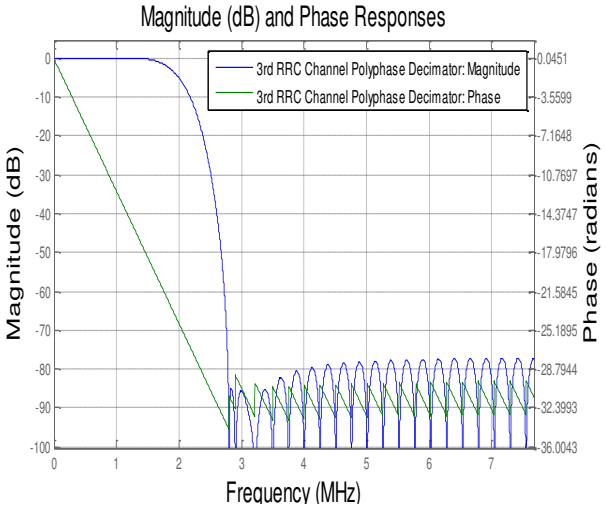

Figure 7. RRC Channel Filter

RRC filter is designed with 1.92 MHz cut off frequency, 0.22 MHz roll-off factor and 50 dB side lobe attenuation using Chebyshev window whose filter response is shown in Figure 6. The DDC is designed by cascading these three stages with 16 bit coefficients as shown in Figure 8.

Finally, the third stage RRC decimator has also been designed using partially serial architecture and only first section of it is shown in Figure 9. The 61 coefficients required to design this RRC filter have been processed using 38 multipliers to improve both area and speed. The delay pipelining and output registers are used for synchronization. The cascade of all optimized stages zoomed view is shown in Figure 10.

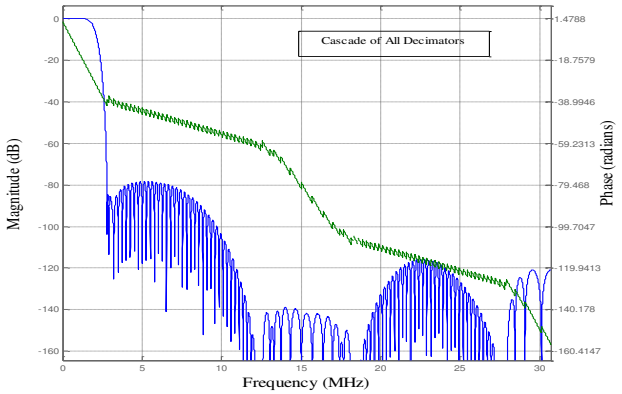

Figure 8. WCDMA DDC Output Response

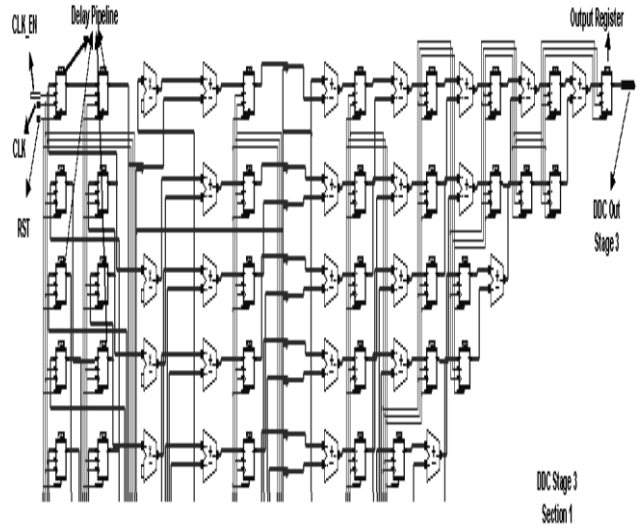

Figure 9. Stage 3 PSPMAC Based RRC Decimator

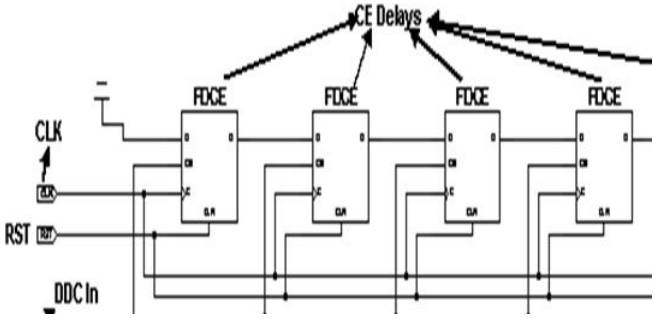

Figure 10. Proposed WCDMA DDC

IV. Hardware Synthesis And Simulation

In the proposed DDC designs CORDIC algorithm based optimized DDS design is used in place of DDS compiler block to generate sinusoidal waveform needed for frequency translation [27]. The FIR Compiler blocks of existing designs are replaced by equiripple techniques based decimators for optimal filter length to reduce the hardware requirement. It is further supported by the half band filter concept to improve the computational complexity for enhanced speed. Finally, Poly-phase decomposition technique is utilized in hardware implementation of proposed design to optimize both speed and area together by introducing the partially serial pipelined MAC architecture. The third stage of decimation has been developed using efficient RRC filter [28] design. All the decimators are implemented using MAC Algorithm with optimal number of embedded multipliers of target FPGA along with pipelined registers to enhance the speed performance and resource utilization. The Virtex-II Pro FPGA device is used for implementation that contains 136 embedded multipliers [29].

Two designs have been developed using different input output precisions. DDC is implemented using input precision of 14 bits and output precision of 16 bit and DDC 2 is implemented using input and output precision of 12 bits. The developed DDCs are simulated using Modelsim Simulator. The output response of DDC1 is shown in Figure 11 and output response of DDC 2 is shown in Figure 12. It can be observed from the simulated waveforms that the output response of both the designs is similar but speed performance of DDC2 is better as compared to DDC1.

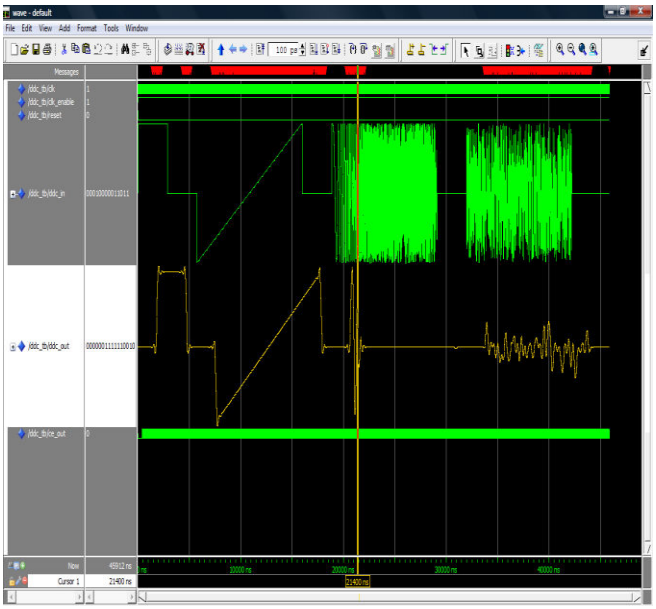

Figure 11. Optimized WCDMA DDC 1 Response

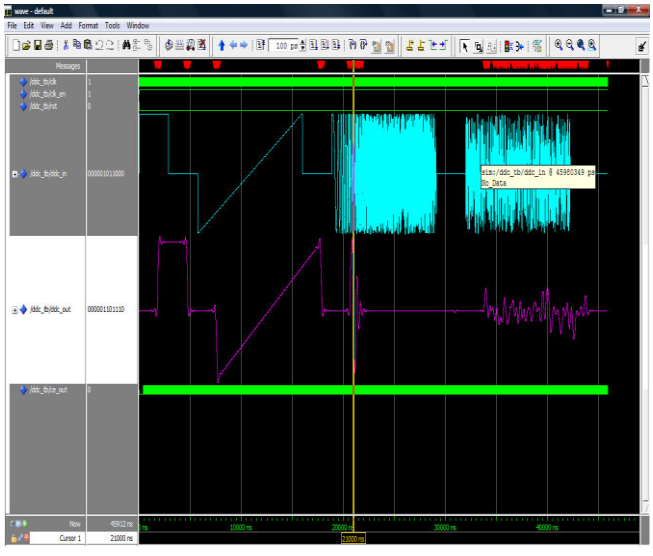

Figure 12. Optimized WCDMA DDC 2 Response

The optimized DDC designs are finally mapped for hardware implementation and synthesised on Virtex-II Pro based xc2vp30-7ff896 target device. The resource consumption of proposed DDC design on specified target device is shown in Table I.

TABLE 1. RESOURCE UTILIZATION

Logic Utilization	DDC Design 1	DDC Design 2
Number of Slices	1477	1462
Number of Flip Flops	2535	2533
Number of LUTs	1429	1366
Number of I/Os	34	28
Number of MULT	46	46

The proposed optimized DDC 2 can operate at a maximum frequency of 146.36 MHz and DDC 1 can operate at 119 MHz as compared to 122.88 MHz in case of [23]. So the proposed DDC 2 provides an improvement of 19% in speed and DDC 1 provide almost same speed as that of existing DDC design. The developed DDC designs have shown better resource utilization as compared to DDC design of [24] which is shown in Table II. Bar graph of the above resource utilization of the proposed DDC design results is shown in Figure 13.

TABLE II. RESOURCE UTILIZATION COMPARISON

Logic Utilization	DDC Design [26]	Proposed DDC Designs
Number of Flip Flops	4.93%	9%
Number of Slices	7.9%	10%
Number of MULT	3.8%	33%

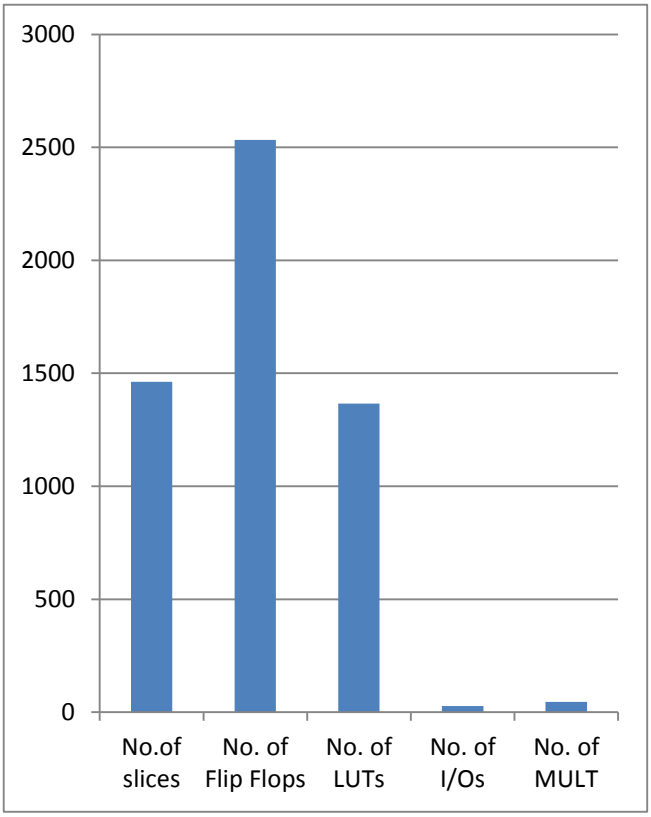

Figure 13. Resource Utilization Bar Graph

V. ASIC DESIGN ANALYSIS

An application-specific integrated circuit (ASIC), is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. A chip designed to run in a specific environment is an ASIC. ASICs use a hardware description language (HDL) to describe the functionality of ASICs such as Verilog or VHDL. The design is coded in Verilog hardware description language (HDL) [30, 31]. Here, ASIC implementation is done to calculate the power, delay, total no. of cells and area. The proposed filter is designed and simulated using 90nm technology cadence environment. Initially, RTL is developed from Verilog file as shown in Figure 14 which is verified using Pre synthesis simulation as shown in Figure 15. Physical design implementation is performed using optimized placement and routing as shown in Figure 16. Finally placed and routed DDC is validated using Post synthesis waveforms as shown in Figure 17. The performance of developed DDC was evaluated for different parameters as shown in Table III. It can be observed from result analysis that proposed DDC require 601mm^2 area and consume 3169.61 nW power.

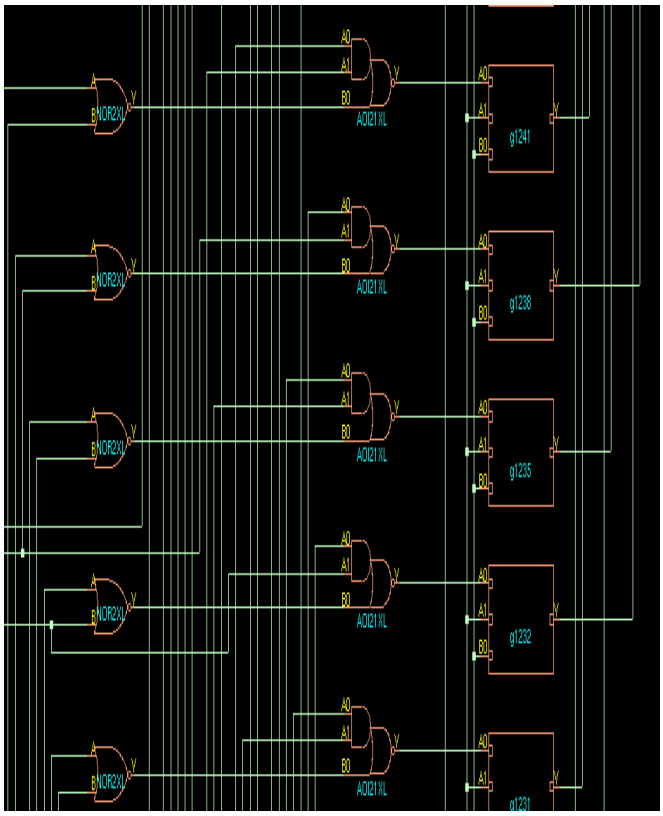

Figure 14. Gate level Netlist of DDC Design

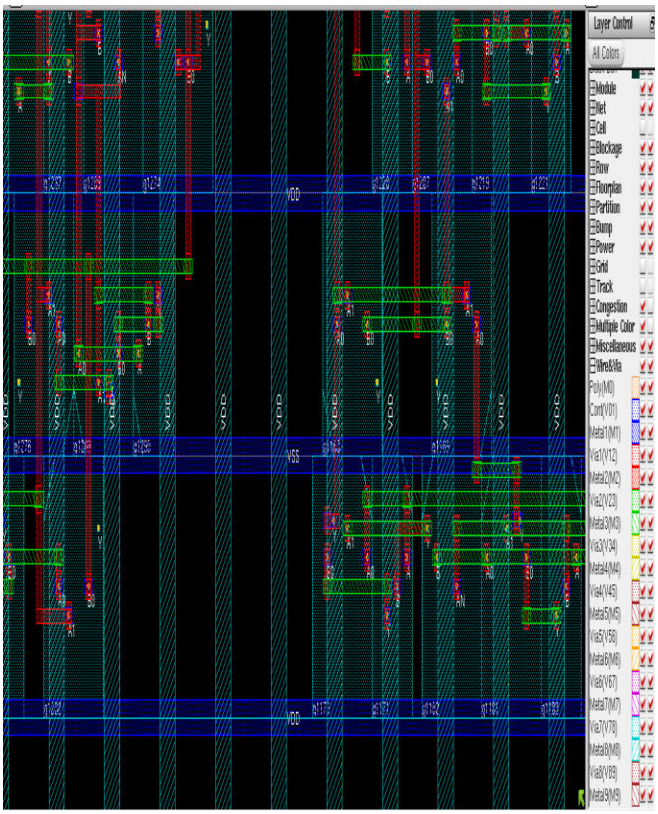

Figure 16. DDC Physical Design

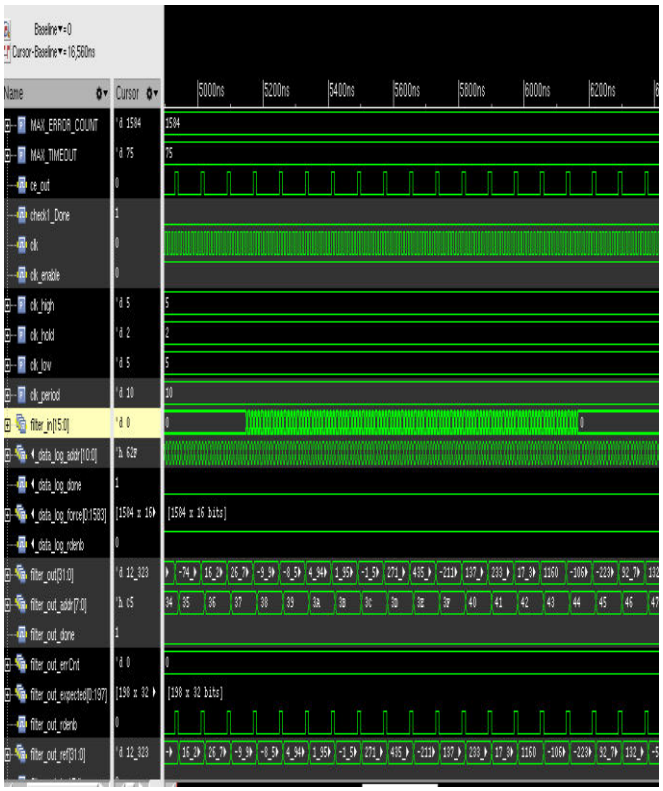

Figure 15. Pre-Synthesis Waveform of DDC

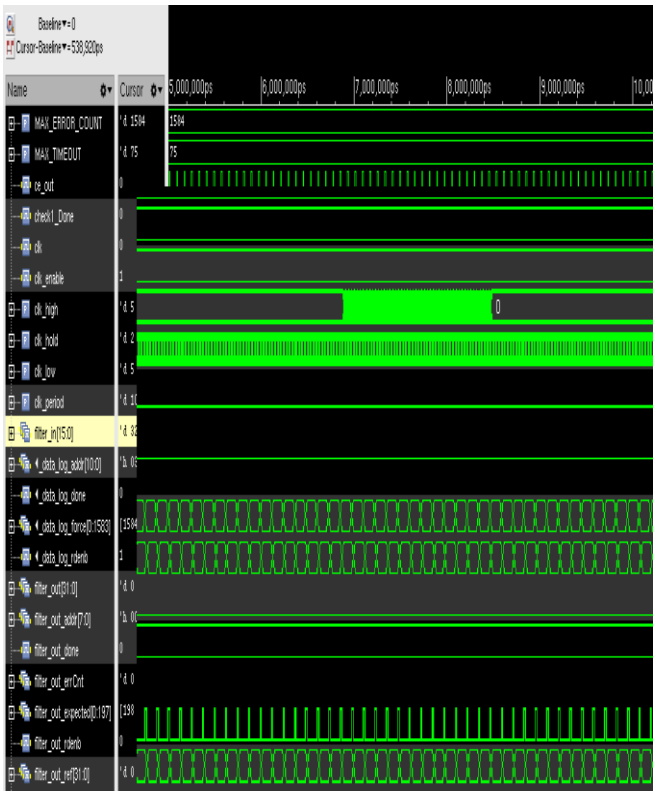

Figure 17. Post-Synthesis Waveform of DDC

Various parameters of DDC design after ASIC realization has been studied and summary of the results obtained are listed in Table III showing operational power supply, technology, total number of cells obtained, total cell area, leakage power, dynamic power and total power. Finally, the area and power consumption of DDC [1] and the proposed DDC ASIC are compared in Table IV. Bar graph of the above obtained results in shown in Figure 18.

TABLE III. DDC ASIC PARAMETERS

Parameter	Value
Power Supply	1.2 V
Technology	CMOS 90 nm
Total No. of Cells	138
Total Cell Area	601mm^2
Leakage Power	2347.455 nW
Dynamic Power	822.151 nW
Total Power	3169.607 nW

TABLE IV. AREA AND POWER COMPARISON

PARAMETERS	DDC[1]	PROPOSED DDC ASIC
Area	1462 Slice Registers	601 mm^2 Silicon Area
Power	-	3169.607 nW

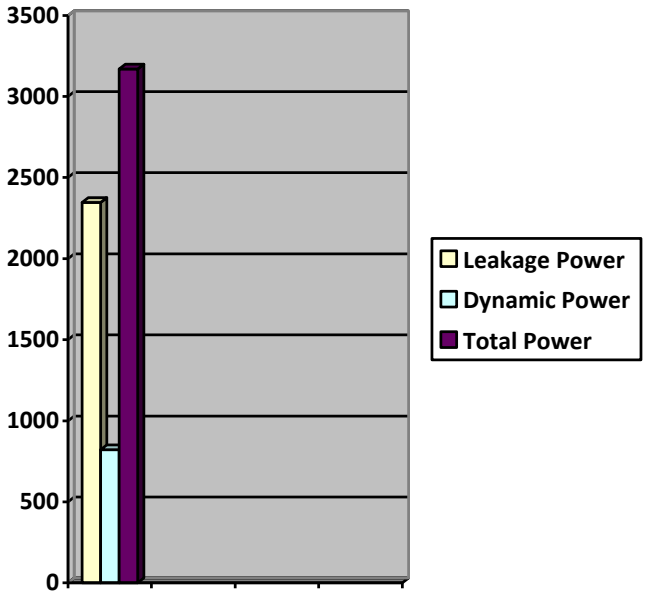

Figure 18. DDC ASIC Power Bar Graph

VI. CONCLUSION

This paper presents an efficient and cost effective DDC design for software defined radios. The proposed DDC designs are developed and implemented on multiplier based Virtex II Pro target FPGA using optimized MAC algorithm. Three decimator stages are optimized separately and then cascaded together. The optimized DDC has been developed using partially serial pipelined MAC algorithm for area and speed optimization. The ASIC realization of the proposed design is done to find the power consumption of the DDC circuit. From the results, it is concluded that the proposed design obtained has low power consumption, i.e., 3169.61 nW and reduced area utilization, i.e., 601mm^2. The DDC designs are efficiently floor planned and routed to achieve the desired timing constraints. The developed DDCs have shown improved resource utilization to provide cost effective solution for software radios in terms of low power consumption and reduced area.

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