Architecture for Extreme Low Power Sensing in Wireless Sensor Network Devices

Jerker Delsing, John Borg, Jonny Johansson

Luleå University of Technology
EISLAB
Luleå, Sweden
jerker.delsing@ltu.se, johan.borg@ltu.se, jonny.johansson@ltu.se

***Abstract*—When discussing powering wireless sensor network nodes, there are a few major energy consumers: communications, microcontroller and the sensor. We propose a wireless sensor network platform architecture minimizing the energy consumption of sensing. The architecture proposed herein is based on a reactive approach to sensing. A number of possible hardware approaches are evaluated and compared. This comparison indicates that analog storage between the sensing element and the sensor electronics can be a feasible method for reducing the energy consumption of the system.**

Keywords-low power WSN sensing; WSN node architecture; wireless sensor network node.

I. INTRODUCTION

One of the most common questions regarding wireless sensor networks, WSN, is what the power consumption at the sensor node must be. Much work has been done on low-powered sensor nodes and their communication abilities: see, for example, [1]–[7]. Some specific examples are schemes handling the reduction of communication [8], effective routing and multihop schemes, and the reactive partial waking up of WSN nodes [9].

Most often, the sensing element itself is disregarded from an energy budget point of view. The current state of the art for sensor interfacing is to convert the sensor data to digital form. The most common approach is using an A/D converter. Other well known approaches involves letting the sensor data influence a digital pulse train of which we easily can measure parameters like frequency, pulse width or duty cycle. None of these approaches puts the power consumption of the sensor into focus. All of these approaches are based on the assumption that all data should be transfered to some computational stage on the WSN node or any device higher up in the system architecture.

In this paper, we propose an architecture for low power interfacing of a sensing element to a WSN node. The architecture exploits the idea of detecting no or discardable changes in data. Such detection should then inhibit further processing of sensor data as early as possible. The proposed architecture is based on a reactive wake-up chain starting at the sensing element itself.

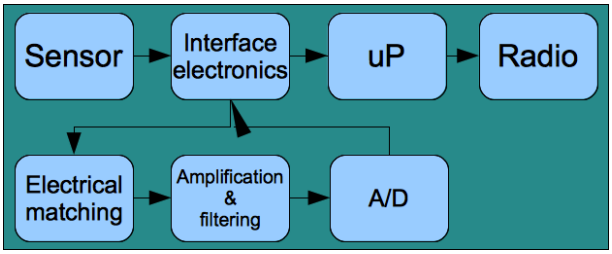

Figure 1. Traditional WSN node architecture, A1

A. WSN node architecture

The basis for this WSN node architecture is the determination of changes in sensing element data as early as possible. In many real systems data changes are small and are most often not of interest to the surrounding system. From an energy consumption point of view, we like to keep as much of the WSN node asleep as possible when determining whether a data sample constitutes a significant change compared with the previous sample.

Consider a WSN node architecture as in Figure 1. The most frequently used approach is to read the data into the μP store and compare it with the previous data. Energy is spent on sensing element sampling, signal amplification and filtering, A/D conversion and data comparison in the μP.

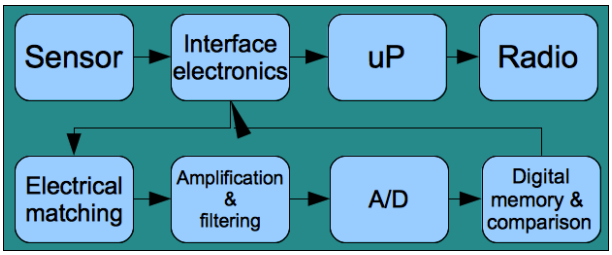

Figure 2. WSN node architecture, A2, with external digital sensor memory and comparison logic.

The next opportunity for comparison is by adding a digital memory and comparison function after the A/D conversion, as shown in Figure 2. Energy is spent on sensor sampling, signal amplification and filtering, A/D conversion and storage and comparison of the data in digital memory. Enabling

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the μP to sleep while performing sensor data sampling if there are no changes or small changes in sensor data will use energy only for the HW cost of digital memory, some configurable logic (to allow for the setting of change limits) and sending a wake-up signal to the μP.

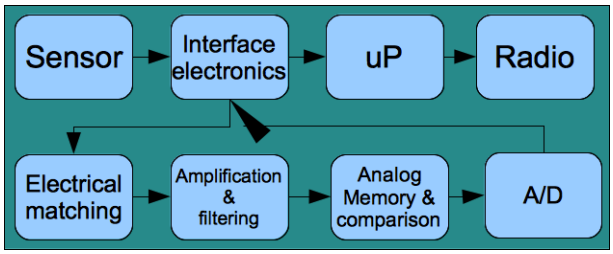

Figure 3. WSN node architecture, A3, with external analog memory and comparison logic before the A/D conversion.

In terms of energy cost here, the A/D conversion is the most power-hungry process. Can we bypass A/D conversion as well? A possibility for this is given in Figure 3. Here, we introduce analog memory with the capability of storing and comparing at least two values with associated logic and signaling to the μP. HW developments supporting this architecture using charge-coupled device technology, or ccd, were made available in the seventies [10]. Recently, new findings presented by Borg and Johansson [11] indicate that ccd technology implemented in standard CMOS processes exhibits properties supporting the proposed architecture. Energy is spent on sensor sampling, signal amplification and filtering and analog storage (ccd) and associated logic. Thus, A/D conversion and the μP can sleep during sensing element data sampling if there are no changes or small changes in the sensed data.

II. Energy analysis of the architecture

To analyze the energy consumption of the presented architectures, we will use two different sensing situations:

- Temperature sensing using a PT100 element as the sensing element
- Ultrasound pulse echo measurement using piezo ceramic transducers as sensing elements

This analysis is conducted using published state-of-the-art data (from our group and others) and data from commercial devices. In this way, we can build an accurate picture of the total energy consumption of the proposed architectures. No circuit simulations are made here, nor have we built any complete devices.

The energy analysis is based on the following model. The total electrical power P_{tot} consumed by a WSN node can be described as:

$$P_{tot} = P_{sens} + P_{cond} + P_{A-mem} + P_{AD} + P_{D-mem} + P_{\mu P} \quad (1)$$

The total energy usage is then obtained by introducing the time needed for each operation (after which it can be turned off). To make the analysis reasonably simple, we assume that the architecture supports turning off E_{sens}, E_{cond}, once data has been stored either in analog or digital form.

For data sampling from one sensor, we assume a sensing and conditioning time t_{sens_cond}, an analog storing time t_{A-mem}, an A/D time t_{AD}, a digital memory time t_{D-mem} and a μP time $t_{\mu P}$. Thus, we obtain the total power E_{tot} used for data sampling from one sensor as:

$$E_{tot} = P_{sens} * t_{sens} + P_{cond} * t_{cond} + P_{A-mem} * t_{A-mem} + P_{AD} * t_{AD} + P_{D-mem} * t_{D-mem} + P_{\mu P} * t_{\mu P} \quad (2)$$

Provided that we have some understanding of the real values of these energies and times, we can calculate the total power consumption. In the following equation, we will do this for two sensor types, a PT-100 sensor and an ultrasonic pulse echo sensor, for each of the three architecture types A1, (see Figure 1), A2 (see Figure 2), and A3 (see Figure 3).

A. Energy analysis PT-100 sensor

In this case, we assume the power consumption and time needed for a PT-100 sensor and its associated electronics, according to table I. For each of the three different architectures in Figures 1-3, we then calculate the expected span of energy consumption (see Figure 4).

Device	Energy consumption [mW]	Time awake [μs]
PT100	0.1-1 [12], [13]	10
Conditioning electronics	0.01	10
Analog memory	0.1-50 [10], [14], [15]	1
A/D (10-14 bit)	0.05 - 2 [16], [17]	1
Digital memory	0.01-0.1	1(storage time)
μP	1-10 [18]	30

Table I
Energy consumption and timing for a PT100 WSN sensor node;, observe the logarithmic scale on the y axis.

B. Energy analysis ultrasound sensor

Here, we discuss the power consumption and time needed for a piezo electric transducer in an ultrasound pulse echo system. A typical pulse echo measuring situation with typical sound signals is shown in Figure 5. In table II, the power consumption and related timing for the sensor and associated electronics areis given. For each of the three different architectures A1-A3 of Figure 1-3, we then calculate the expected span of (maximum and minimum) energy consumption (see Figure 6).

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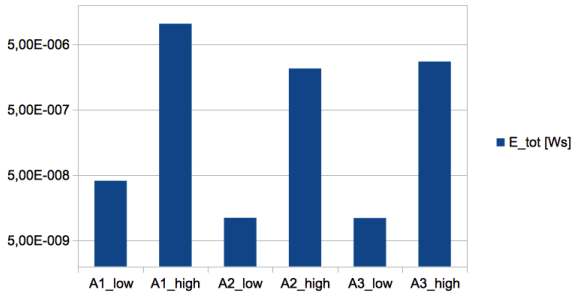

Figure 4. Energy usage for different WSN node architectures and a PT100 temperature WSN node.

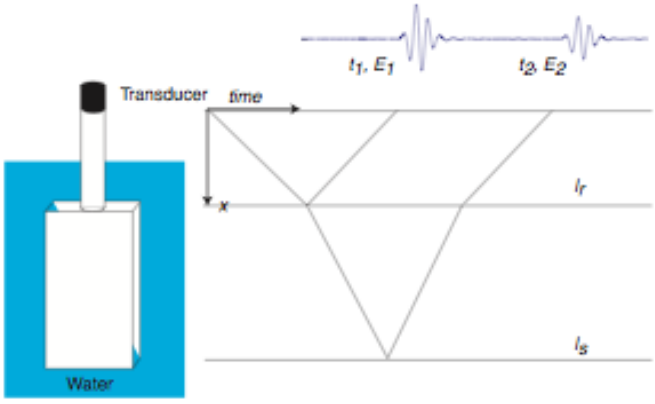

Figure 5. Ultrasound pulse echo measurement with associated acoustic signals

Device	Energy consumption [mW]	Time awake [μs]
Piezo excitation	0.01 [19]	1 (1 μs long pulse excitation
Amplifier and filtering	1-100 [20]–[22]	10-20 (signal duration + startup time)
Analog memory	0.1-100	10-15 (signal duration + startup time)
A/D	0.1-10	10-15 (sampling + startup time)
Digital memory	0.01-0.1	10 (storage time)
μP	1-10	30 (300 clock cycles at 10MHz)

Table II
ENERGY CONSUMPTION AND TIMING FOR AN ULTRASOUND WSN SENSOR NODE;, OBSERVE THE LOGARITHMIC SCALE ON THE Y AXIS.

III. RESULTS AND DISCUSSION

Under the assumptions that we made, we have compiled energy consumption data for two sensing scenarios. These data are shown in Figures 4 and 6. It is obvious that the μP uses a large amount of energy. Thus, any architecture that

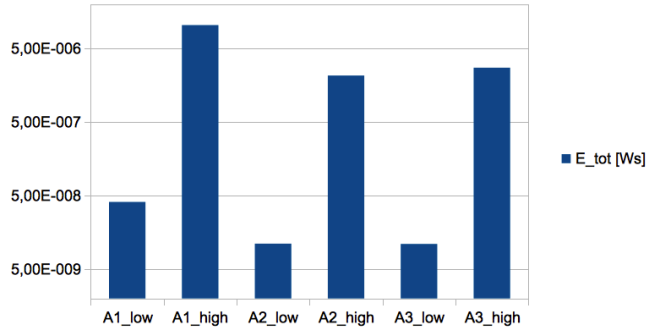

Figure 6. Energy usage for different WSN node architectures for a piezo electric based ultrasound pulse echo WSN node.

can avoid waking up the μP has clear advantages from an energy consumption point of view.

It is also clear that in a sensing situation with a dynamic sensor signal, such as ultrasound, avoiding A/D conversion is a promising approach. If analog memory and comparison techniques can be developed similar to what we have seen for A/D converters, analog storage architecture will be a strong contender forin future WSN designs.

IV. CONCLUSION

The reactive architecture proposed here for minimal energy consumption of sensing on WSN platforms is promising. Based on an analysis of current state-of-the-art sensor interface electronics, an approach using analog storage provides interesting data when compared with more mature technology such as ADC:s and memory logic.

Future work will reveal whether if a reactive architecture based on an analog storage approach will show improvements in energy consumption similar to those of advanced ADC. If such improvements are shown, the analog storage approach has clear merit for use in future WSN node designs.

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