Analytical Modeling of Parametric Yield Considering Variations in Leakage Power and Performance of Nano-Scaled Integrated Circuits

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***Abstract*— In this paper, we present an analytical method to model the joint probability density function of delay and leakage power. In order to model the joint distribution of these two parameters, they should be modeled independently through an accurate method. The manufacturing process variations as the sources of delay and leakage power variations are considered in our modeling. We also demonstrate that the proposed method is so accurate in modeling joint cumulative density function which is the very parametric yield whose predicting is the main objective of this work. Finally, the proposed method is verified by HSPICE simulations for combinational benchmark circuits in 45 nm technology. We compare the accuracy of our method with that of classic bivariate Gaussian estimation. Simulation results reveal that the mean percentage error of our proposed technique for joint cumulative density function of ISCAS85 benchmark circuits is 2.5 % by average. The average improvement achieved in accuracy of modeling joint cumulative density function through our work compared to aforementioned classic method is 17.1 % and 16.8% respectively without and with considering correlated intra-die variations.**

Keywords- ***Process Variation*; *Parametric Yield*; *Simulation*; *CMOS Circuits.***

I. INTRODUCTION

The scaling of CMOS has resulted in the increasing magnitude of the variabilities which manifest themselves in the forms of random and systematic variations. Sources of variations could range from random dopant fluctuation to non-idealities imposed by photolithography [1] [2].

The dramatic increase in leakage power with scaling, and a strong dependence of leakage on highly varying process parameters, raises the importance of statistical leakage and parametric-yield optimization. Leakage-power consumption increases are due to both channel (subthreshold)-leakage and gate-leakage currents [3]. The subthreshold current is a strong exponential function of highly variable process parameters. It has been demonstrated that the variability of subthreshold leakage depends primarily on L and V_{th} [4]. Leakage power is inversely correlated with chip frequency. Hence, the Joint Probability Density Function (JPDF) of delay and leakage should be modeled precisely in order to budget one while optimizing another. As a result, parametric yield modeling considering the correlation between delay and leakage consumption is of great importance.

Yield –driven optimization tools require accurate statistical models for both timing and leakage consumption considering correlation between them. There have been works which have limited their yield estimation to either timing or leakage [5], [6]. However, these approaches neglect the correlation between delay and leakage power.

Although [7] proposes a methodology to model the parametric yield considering leakage/performance correlation, it only presents a closed-form equation for total chip leakage that models the dependence of the leakage current distribution on different process parameters. The only closed-form expression for JPDF of delay and leakage has been proposed by [8][9], wherein the cornerstone of modeling is taking the JPDF of delay and logarithm of leakage as bivariate normal distribution. [10] and [11] despite of improving and building their method upon [8][9] still use the same model which is bivariate normal approximation.

In this paper, we present an analytical approach to accurately model the JPDF of delay and leakage power. In order to verify the efficacy and accuracy of our proposed method, we present the results of HSPICE Monte Carlo simulation as well as those of our model for the performance and leakage consumption of ISCAS85 benchmark circuits [12]. The simulations have been performed in Nangate 45 nm open cell library technology [13]. It should be mentioned that the method presented in this paper is not limited only to this specific issue in Integrated Circuits industry. This method can be extended to any application in engineering and science where modeling and simulation of the JPDF of several random variables is the main objective. This paper is organized as follows. Section II briefly introduces the main formulations we use to model the delay and leakage power under variations. Section III introduces our proposed analytical yield modeling. Section IV discusses the simulation results and a comparison is made between our method and previous work. Finally, Section V concludes the paper.

II. FORMULATIONS OF DELAY AND LEAKAGE POWER UNDER VARIATIONS

In order to model delay and leakage power under process variations, we need to determine which parameters of the circuit are subject to variations. In this paper, similar to [9], we assume that gate-length and gate-length-independent threshold voltage are the sources of variation. It is also assumed that these sources are normally distributed. According to [9], delay and leakage power of an individual gate can be expressed as following:

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$$Delay = d_{nom} + \sum_{i=1}^{p} \alpha_i (\Delta P_i)$$

$$Ln(Leakage) = V_{nom} + \sum_{i=1}^{p} \beta_i (\Delta P_i) \quad (1)$$

Where d_{nom} and $\exp(V_{nom})$ are the nominal values of delay and leakage power, respectively. α's and β's also represent the sensitivities of delay and log of leakage to the process parameters under consideration. The Random Variable (RV) ΔP_i represents the change in the process parameters from their nominal value. In our case, the sources of variations are gate-length and gate-length-independent threshold voltage. Therefore, (1) can be modified to the following for each gate:

$$\begin{aligned} Delay &= d_{nom} + \alpha_1 \Delta V_{th0N} + \alpha_2 \Delta V_{th0P} + \alpha_3 \Delta L \\ Ln(Leakage) &= V_{nom} + \beta_1 \Delta V_{th0N} + \beta_2 \Delta V_{th0P} + \beta_3 \Delta L \end{aligned} \quad (2)$$

where ΔV_{th0N} and ΔV_{th0P} represent the change in NMOS and PMOS gate-length independent threshold voltage. ΔL also represents the change in gate-length.

III. ANALYTICAL YIELD MODELING

The parametric yield of a circuit given delay and power constraints can be expressed as:

$$Y = P(D \le D0, P \le P0) \quad (3)$$

which is the probability of delay and leakage being less than *D0* and *P0*, respectively. Srivastava and Chopra propose a bivariate Gaussian random variable for yield [8][9]. According to [8][9], it is assumed that delay and logarithm of leakage are normally distributed. As a result, they proposed the bivariate normal distribution for JPDF of delay and logarithm of leakage as follows:

$$f_{xy}(x,y) = \frac{e^{-\frac{\frac{(x-\mu_x)^2}{\sigma_x^2} - \frac{2.\rho.(x-\mu_x).(y-\mu_y)}{\sigma_x.\sigma_y} + \frac{(y-\mu_y)^2}{\sigma_y^2}}{2(1-\rho^2)}}}{2\pi\sigma_x\sigma_y.\sqrt{1-\rho^2}} \quad (4)$$

where, *x*, *y*, and ρ respectively stand for delay, natural logarithm of leakage, and correlation coefficient. However, even if the gate delays are assumed to be normal, it should be mentioned that maximum operation is an inherently nonlinear function. The maximum of two normal distributions is a non-Gaussian distribution. Blauuw et al discuss and explain the non-Gaussian nature of delay distribution [14]. Besides, the simulation results reveal that natural logarithm of leakage consumption deviate from normal distribution. For some input states of gates, the leakage distribution does not show lognormal behavior. As a result, the accurate JPDF of delay and natural logarithm of leakage is skewed by both variables. Hence, there is a need to analytically calculate the JPDF of delay and leakage power in order to obtain a more accurate prediction.

A. Analytical JPDF of Delay and Leakage Power

Given two random variables *x* and *y* and two functions *g(x,y)* and *h(x,y)* we assume we have the following functions:

$$z = g(x, y) \quad , \quad w = h(x, y) \quad (5)$$

These functions are also random variables whose JPDF shall be expressed in terms of JPDF of *x* and *y*. Given this fact, we shall express the JPDF $f_{zw}(z,w)$ of the random variables $z=g(x,y)$ and $w=h(x,y)$ in terms of the JPDF $f_{xy}(x,y)$ of the random variables *x* and *y*. The Jacobian function $J(x,y)$ is, by definition, the determinant given by:

$$J(x, y) = \begin{vmatrix} \frac{\partial g(x,y)}{\partial x} & \frac{\partial g(x,y)}{\partial y} \\ \frac{\partial h(x,y)}{\partial x} & \frac{\partial h(x,y)}{\partial y} \end{vmatrix} \quad (6)$$

To find $f_{zw}(z,w)$, we solve the systems (5) for *x* and *y*. If this system has no real solutions in some region of the *zw* plane, $f_{zw}(z,w)=0$ for every (z,w) in that region. Suppose, then, that (5) has one or more solutions (x_i,y_i), that is,

$$z = g(x_i, y_i) \quad , \quad w = h(x_i, y_i) \quad (7)$$

In this case,

$$f_{zw}(z,w) = \frac{f_{xy}(x_1,y_1)}{|J(x_1,y_1)|} + \frac{f_{xy}(x_2,y_2)}{|J(x_2,y_2)|} \ldots + \frac{f_{xy}(x_i,y_i)}{|J(x_i,y_i)|} + \ldots \quad (8)$$

where (x_i, y_i) are all pairs satisfying (7) [15]. The aforementioned procedure is extendable to any n×n systems. Now, for calculating the JPDF of delay and leakage power, we can replace *z* and *w* by delay and leakage power, respectively, in previous analysis. However, in our case, we may have n sources of variation where n is not necessarily equal with 2. In this case, we have to add n-2 auxiliary equations to systems. Hence, in our case where we have 3 sources of variation, our 3*3 1st order systems are as following:

$$\begin{cases} Delay = z = g(\Delta V_{th0N}, \Delta V_{th0P}, \Delta L) \\ Ln(Leakag) = w = h(\Delta V_{th0N}, \Delta V_{th0P}, \Delta L) \\ E = \Delta L \quad \text{Auxiliary Equation} \end{cases} \quad (9)$$

$$\begin{bmatrix} Delay \\ Ln(Leakage) \\ E \end{bmatrix} = \begin{bmatrix} \alpha_1 & \alpha_2 & \alpha_3 \\ \beta_1 & \beta_2 & \beta_3 \\ 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} \Delta V_{th0N} \\ \Delta V_{th0P} \\ \Delta L \end{bmatrix} + \begin{bmatrix} d_{nom} \\ V_{nom} \\ 0 \end{bmatrix}$$

Equation (9) can be simply expressed as follows:

$$Y = \Sigma \bullet X + \Phi \quad (10)$$

Where *Y* and *X* are respectively dependent variables and sources of variations vectors. Σ and Φ are respectively n×n coefficients matrix and constants vectors. Now, (9) should be reordered to solve for vector X. Now, X is obtained from the following:

$$X = \Sigma^{-1} \bullet (Y - \Phi) \quad (11)$$

Therefore,

$$\begin{bmatrix} \Delta V_{th0N} \\ \Delta V_{th0P} \\ \Delta L \end{bmatrix} = \begin{bmatrix} \alpha_1 & \alpha_2 & \alpha_3 \\ \beta_1 & \beta_2 & \beta_3 \\ 0 & 0 & 1 \end{bmatrix}^{-1} \times \begin{bmatrix} Delay - d_{nom} \\ Ln(Leakage) - V_{nom} \\ E \end{bmatrix} \quad (12)$$

According to (6), (9), the Jacobian function of this system is obtained through the following:

$$J(\Delta V_{th0N}, \Delta V_{th0P}, \Delta L) = \begin{vmatrix} \alpha_1 & \alpha_2 & \alpha_3 \\ \beta_1 & \beta_2 & \beta_3 \\ 0 & 0 & 1 \end{vmatrix} = \alpha_1\beta_2 - \alpha_2\beta_1 \quad (13)$$

Now, by (8) and (13), the JPDF $f_{zwE}(z,w,E)$ of delay, Ln(Leakage), and auxiliary variable (E) in terms of the JPDF of ΔV_{th0N}, ΔV_{th0P}, and ΔL can be expressed as following:

$$f_{zwE}(z,w,E) = \frac{f_{\Delta V_{th0N}\Delta V_{th0P}\Delta L}(\Delta V_{th0N}, \Delta V_{th0P}, \Delta L)}{\alpha_1\beta_2 - \alpha_2\beta_1} \quad (14)$$

Where, ΔV_{th0N}, ΔV_{th0P}, and ΔL are obtained from (12). JPDF of delay and Ln(Leakage) can be obtained through the following integration:

$$f_{zw}(z,w) = \int_{-\infty}^{+\infty} f_{zwE}(z,w,E).dE \quad (15)$$

B. Analytical Parametric Yield

According to (3), the parametric yield of a circuit given delay and leakage power constraints is the probability of delay and leakage power being less than *D0* and *P0*. Subsequently, having found the JPDF of delay and leakage power, the parametric yield of a circuit can be expressed as following:

$$Y(D0, P0) = \int_{-\infty}^{P0} \int_{-\infty}^{D0} f_{zw}(z,w).dz.dw \quad (16)$$

The parametric yield is a 3-dimentional surface versus delay and leakage power constraints. This surface monotonically increases from 0 to 1 as it represents a probability.

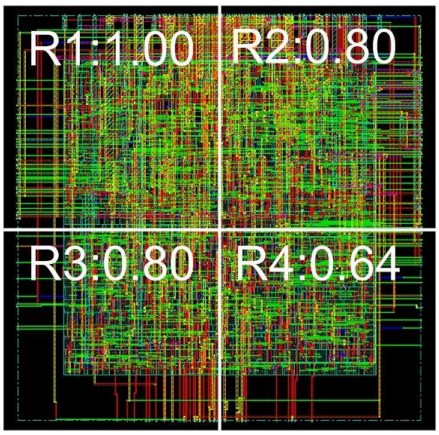

Figure 1. Partition of c7552 physical layout using a grid to model the correlated components of variation where the refernce for correlation coefficients is the top-left square.

C. Correlated Intra-Die Variations

The sources of variation are correlated within the die area. To handle the correlated components of variations, the overall chip is divided into a grid as shown in Figure 1. The correlation coefficient varies from one and falls off to zero with increasing distance. Each square in the grid corresponds to a random variable of the process parameter which has correlations with all other random variables corresponding to other squares in the grid. The values at the top of each of the grids show the correlation coefficients with the top left square on the grid.

To simplify the problem, this set of correlated random variables is replaced by another set of mutually independent random variables with zero mean and unit variance using the principal components of the set of correlated random variables. A vector of random variables, say X, with a correlation matrix C, can be expressed as a linear combination of the principal components Y as [8]:

$$X = \Delta_X + \Omega V^{-1} D^{1/2} Y \quad (17)$$

Where Δ_X is the vector of the mean values of X, Ω is a diagonal matrix with the diagonal elements being the standard deviations of X, V is the matrix of the eigenvectors of C, and D is a diagonal matrix of the eigenvalues of C. If ΔP_p in (1) is generated by (17), correlated sources of variations are incorporated in calculating delay and leakage power consumption.

IV. Results and Discussion

We implemented our proposed model and bivariate normal model in MATLAB and compared the accuracy of both approaches by HSPICE Monte Carlo simulations. We performed 10.000 Monte Carlo simulations on ISCAS 85 benchmark circuits assuming that all sources of variations have ($3\sigma/\mu$=20%). In this paper, we assume that sources of variations are channel-length and gate-length independent threshold voltages of NMOS and PMOS transistors. In this work, the full-chip simulations on ISCAS 85 circuits have been set up similar to those of [8] in terms of sources of variations. In our approach, the JPDF of delay and leakage power are calculated analytically by means of Jacobian matrix.

Figure 2 depicts the JPDF and Joint Cumulative Distribution Function (JCDF) of bivariate normal model for c432 from the benchmark circuits. Figure 3 shows the JPDF and JCDF of our model and simulation results. As shown in Figure 2 and Figure 3, the JPDF of our model is visually more similar to that of simulation results compared to bivariate normal model. The errors are calculated with regard to HSPICE simulation results. The Mean Percentage Error (MPE) of model is calculated as following:

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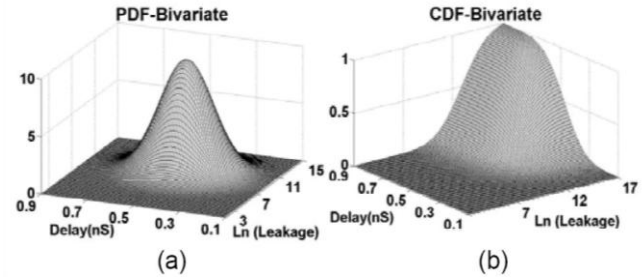

Figure 2. Bivariate normal model diagram of c432 versus Delay and Ln (Leakage) under variations having ($3\sigma/\mu$ = 20%) (a) Joint PDF (b) Joint CDF.

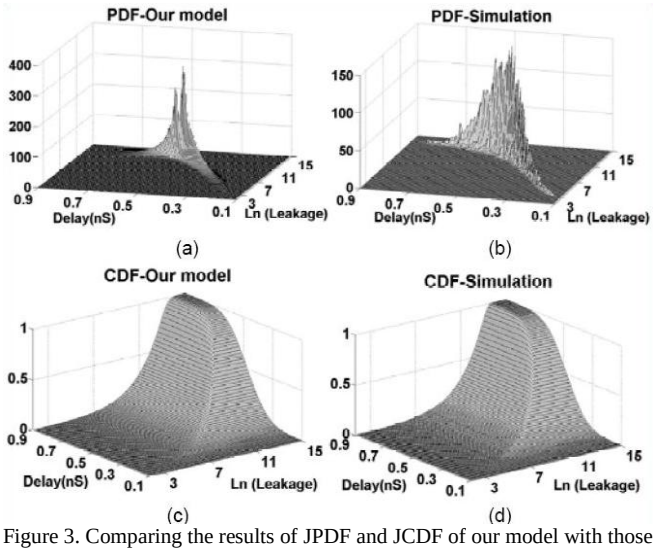

Figure 3. Comparing the results of JPDF and JCDF of our model with those of HSPICE simulation under variations having ($3\sigma/\mu$ = 20%) for c432 (a) JPDF of our model (b) JPDF of simulation (c) JCDF of our model (d) JCDF of simulation.

$$MPE = \frac{1}{n}\sum_{i=1}^{n}\left|\frac{Model(i) - SPICE(i)}{SPICE(i)}\right| \qquad (18)$$

where Model(i) and SPICE(i) are the i^{th} point in the model and SPICE simulation, respectively. The improvement in the mean error achieved by our model compared to bivariate model for ISCAS 85 benchmark circuits are collected in Table I with and without correlated intra-die variation. We have calculated the average error improvement achieved for estimating the JCDF of delay and leakage by our model to be 17.1% compared to bivariate normal model when correlated intra-die variations have not been considered. The mentioned average error improvement has been calculted to be 16.8% by considering correlated intra-die variations. We have assumed that the correlated intra-die variations follow the pattern of Figure 1 for all circuits.

V. CONCLUSION

We proposed a methodology for modeling the JPDF and parametric yield considering variations of delay and leakage power. In this method, we analytically calculated the JPDF of leakage power and delay by means of Jacobian matrix. Then, JCDF (parametric yield) was extracted by integration. We demonstrated that JPDF and JCDF achieved by our modeling outperform their counterparts in [8][9]. Simulation results in 45 nm technology on ISCAS85 benchmark circuits revealed that our proposed model improves the accuracy of JCDF 17.1% and 16.8% by average, respectively, without and with considering correlated intra-die variations. The proposed method in this paper is generic and can be incorporated in modeling any JPDF in engineering, considering the correlations among the random variables, where accuracy of the model is of great importance.

TABLE I
MEAN PERCENTAGE ERROR (%) OF JCDF OBTAINED FROM OUR MODEL AND BIVARIATE NORMAL MODEL

Test Gates	Without Correlated Intra-Die Variations		With Correlated Intra-Die Variations	
	Bivariate Model	our Model	Bivariate Model	our Model
c17	21	1.7	19	1.6
c432	15.2	1.3	14.1	1.35
c499	14.4	1.6	15.2	1.67
c1355	20	1.7	21.4	1.65
c1908	19.8	1.4	18	1.25
c2670	26	5.2	24.3	3.98
c3540	22	3.6	21	3.24
c5315	17.8	4.2	19	5.15
c6288	23.4	2.7	22.6	3.1
c7552	16.8	1.3	18.7	1.53
AVG	19.6	2.5	19.3	2.5

REFERENCES

[1] M. Orshansky, S. R. Nassif, and D. Boning, Design for Manufacturability and Statistical Design: A Constructive Approach. New York, NY: Springer, 2008.

[2] A. Srivastava, D. Sylvester, and D. Blaauw, Statistical Analysis and Optimization for VLSI: Timing and Power. New York, NY: Springer, 2005.

[3] M. Mani, A. Devgan, M. Orshansky, and Y. Zhan, "A statistical algorithm for power and timing-limited parametric yield optimization of large integrated circuits," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 26, no. 10, Oct. 2007, pp-1790-1802.

[4] R. Rao, A. Devgan, D. Blaauw, and D. Sylvester, "Parametric yield estimation considering leakage variability," in Proc.Des.Autom.Conf., 2004, pp. 442-447.

[5] H. Chang and S. S. Sapatnekar, "Statistical timing analysis considering spatial correlations using a single PERT-like traversal," in Proc. ACM/IEEE Int. Conf. Comp. Aided-Des. ICCAD, 2003, pp. 621-625.

[6] C. Visweweriah et al, "First-order incremental block-based statistical timing analysis," in Proc.Des.Autom.Conf., 2004, pp. 331-336.

[7] R. R. Rao, A. Devgan, D. Blaauw, and D. Sylvester, "Analytical yield prediction considering leakage/performance correlation," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 25, no. 9, Sep. 2006, pp-1685-1695.

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[8] A. Srivastava et al, "Accurate and efficient gate-level parametric yield estimation considering correlated variations in leakage power and performance," in Proc.Des.Autom.Conf., 2005, pp. 535-540.

[9] A. Srivastava, K. Chopra, S. Shah, D. Sylvester, and D. Blaauw, "A novel approach to perform gate-level yield analysis and optimization considering correlated variations in power and performance," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 2, Feb. 2008, pp-272-285.

[10] K. Chopra, S. Shah, A. Srivastava, D. Blaauw, and D. Sylvester, "Parametric yield maximization using gate sizing based on efficient statistical power and delay gradient computation," in Proc. Int.Conf.on Comp.-Aided Design, 2005, pp. 1023-1028.

[11] D. Sylvester, K. Agarwal, and S. Shah, "Variability in nanometer CMOS: impact, analysis, and minimization," Elsevier the VLSI Journal of Integration, 41 (2008), pp. 319-339.

[12] F. Brglez and H. Fujiwara, "A Neutral Netlist of 10 Combinational Benchmark Circuits," Proc. IEEE Int. Symp. Circuits and Systems, IEEE Press, Piscataway, N.J., 1985, pp. 695–698.

[13] FreePDK45. [online] Available:
http://www.eda.ncsu.edu/wiki/FreePDK45:Contents [Retrieved, October 2015]

[14] D. Blaauw, K. Chopra, A. Srivastava, and L. Scheffer, "Statistical timing analysis: from basic principles to state of the art," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 4, Apr. 2008, pp-589-607.

[15] A. Papoulis, Probability, Random Variables and Stochastic Process. New York: McGraw-Hill, 2002.

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