Ultra Low Power CMOS Phase Locked Loop synthesizer for Very High Frequencies

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Abstract—**This paper describes the design of an essential component in wireless transceivers, the frequency synthesizer. The synthesizer is implemented using Phase Locked Loop (PLL). Second order PLL, type II, with a reference frequency 10MHz is designed using 180nm analog CMOS process technology. The synthesizer generates signals in frequency range of 10-100 MHz. The simulated power consumption of the system is 37µW with a deviation from the true periodicity; root mean square periodic jitter is in range of 5 ps.**

Keywords- PLL; CMOS; ,frequency; synthesizer.

I. INTRODUCTION

The main job of frequency synthesizer is to create a set of frequencies multiple of a reference frequency. Such specification can be made using three techniques: the look up table synthesizer, the direct/indirect synthesizer and Phase-Locked Loop (PLL) synthesizers [1]. PLL frequency synthesizers offer high level of stability and accuracy determined by the crystal oscillator; they are also easy to control using a digital control circuit. PLL plays a major role in the field of communication systems [2][3], where the major target is saving battery energy, PLL is the most power consumer block in the transceiver [4]. Radio Frequency, nowadays, is used as the intermediate between the sensor unit and the computer for biomedical applications, mostly in the muscular stimulation (heart diseases) [5]. Any circuit within the chip should consume ultra-low power and area. In this paper, a PLL is proposed as a frequency synthesizer, based on Phase/Frequency Detector (PFD), Charge Pump (CP), Voltage Control Oscillator (VCO) and Frequency Divider (FD), which are implemented using 0.18µm CMOS. In order to minimize the power consumption, a lower supply voltage is used. N-divider is used to synthesize the Reference Frequency (F_{ref}). Targeting high output frequency needs high power consumption.

In this paper, we discuss a compromise VHF PLL with a limited current budget. The paper is organized as follows. Section II presents the theoretical background. Circuit design and simulation results are discussed in Section III. In Section IV, the summary of system performance is presented. Conclusion and future work are discussed in Section V.

II. SYSTEM DESIGN AND BEHAVIORAL SIMULATION

In this section, a behavioral model is introduced to define the system specs and ensure the system stability. PFD detects the phase and frequency error. CP and Loop Filter compute the phase error and convert it to average voltage information used by VCO, which creates a frequency synchronized with $F_{ref.}$.

The system is modeled in Figure 1 using linear approaches; PFD/CP detects the error in the phase. VCO generates the output frequency from the input controlled voltage.

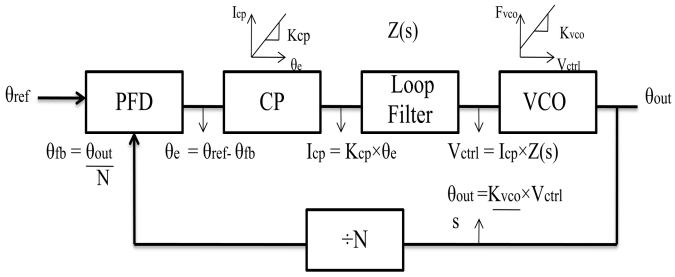

Figure 1. Model of PLL

From the theory of the Feedback [5]:

$$H_{CL} = \frac{\theta_{out}}{\theta_{ref}} = \frac{N \times H_{OL}}{1 + H_{OL}} \quad (1)$$

where H_{CL} is the closed loop gain, while H_{OL} is the open loop gain.

$$H_{OL} = \frac{K_{CP} \times Z(s) \times K_{VCO}}{s \times N} = \frac{K_{vco}\, I_p\, R_p}{2\pi N} \times \frac{s + \frac{1}{R_p C_p}}{s^2} \quad (2)$$

where;
K_{CP}: The charge pump gain (A/rad).
K_{VCO}: The VCO gain gain (Hz/V).
Z(s): The Loop Filter (LF) impedance

To ensure the system stability, from (2), a phase of H_{OL}< 180° should be guaranteed at the unity gain frequency (f_t). PLL second order has two poles at DC (phase $H_{OL}(0)$ = 180°); a zero is introduced at low frequency to maintain the system stability. In contrast, Phase Margin (PM)>0, i.e., the system stability is guaranteed as shown in Figures 2. Figure 3 shows the weak overshoot of the step response.

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The maximum overshoot is often used as a measure of the relative stability of the control system. The settling time is

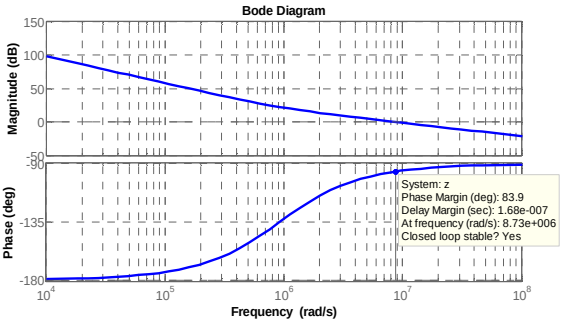

Figure 2. Phase Margin

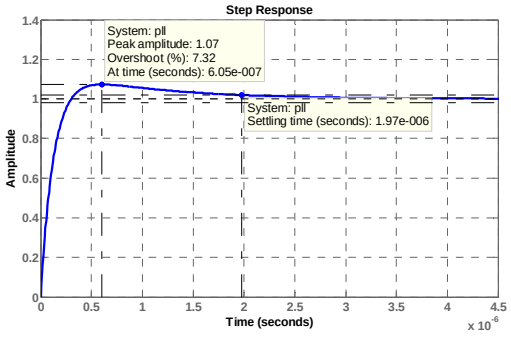

Figure 3. Step response

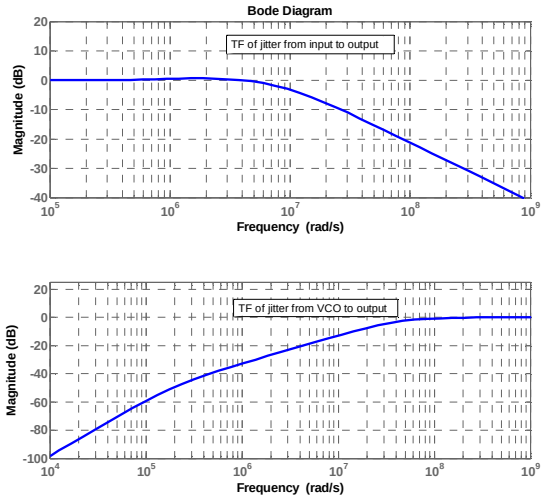

Figure 4. Transfer of jitter

$2\mu s \propto \frac{1}{5f_t}$. In our application, the time needed to achieve lock condition (constant input output phase difference), is not critical; thus, the unity gain frequency is used to be in order of 1MHz.The transfer function for Type II PLL has a low pass characteristic; as a result, slow jitter at the input propagates to the output, but fast jitter does not. On the other hand, the phase noise VCO transfer function is a high pass filter introduced in (3). Figure 4 presents the phase noise transfer functions of the input reference and the VCO. For that reason, in our design, the CP consumption has been reduced, while increasing the VCO current for a better phase noise at the frequency of interest, while respecting the estimated low power consumption budget.

$$\frac{\varphi_{FBDIV}}{\varphi_{ref}}(s) = \frac{s^2}{s^2+2\zeta\omega_n s+\omega_n} \quad (3)$$

where;
ζ: Damping ratio.
ω_n: Natural frequency (Hz).

III. CIRCUIT DESIGN AND SIMULATION

A. *Phase Frequency Detector / Charge Pump/ Loop Filter*

PFD is a circuit that measures the phase and frequency difference between the signal that comes from the VCO and the reference signal. Outputs pulses (Down & Up) have widths proportional to the phase error. Figure 5 presents a PFD using 2 True Single-Phase-Clock (TSPC) D-Flip-Flop [6]. Clocks are exploited for resetting; F_{ref} to reset F_{fb} and vice versa. In comparison to the conventional PFD, the AND gate, generating the reset signal [7], is removed. The delay due to the propagation of the signal will be saved. The CP converts the error in phase to current information. It has three states as illustrated in Table I.

TABLE I. THREE STATES OF CHARGE PUMP

$\overline{\text{Down}}$	Up	Vctrl
1	0	rise
0	1	reduce
1/0	1/0	unchanged

The main feature of the architecture shown in Figure 6 is the reduction of dead zone (the delay needed on CP digital command signals to avoid all ones condition) and the guarantee of a safe operation without any CP current glitches on the Loop Filter (LF) capacitance. PFD design is suitable for fast PLL operating at higher frequency; we should guarantee that the maximum delay of the PFD is greater than the CP switching speed in order to target a zero PFD dead zone.

B. *Voltage Controlled Osicllator*

The main part of the system is the VCO, based on ring oscillator [8], and designed by a ring connection between five inverters [9]. The charging and discharging currents are equal, both depend linearly on V_{ctrl}. The F_{osc} is proportional to both currents. Thus, F_{out} of the presented architecture varied linearly withV_{ctrl}.

$$F_{out} = \frac{1}{2N \times T_d} \quad (4)$$

Where T_d is the delay introduced by one inverter.

$$T_d = \frac{C_L \times V_{supply}}{I_{cha}} + \frac{C_L \times V_{supply}}{I_{dis}} = \frac{C_L}{I} \quad (5)$$

Where;
V_{supply}: is the supply voltage equal 0.5 V.
C_L: is the load capacitance seen by one gate.
$I_{cha/dis}$: charging and discharging current.

From the presented architecture, $I_{char} = I_{dis} = I$. From (4) and (5), we can deduce that F_{out} is proportional to the current.

From Figure 7, the I_{dis} controlled by an input voltage applied to the gate.

$$I \propto ((V_{ctrl} - V_{th})V_{dsat} - \frac{1}{2}V_{dsat}^2) \quad (6)$$

Where
V_{th} : is the transistor threshold voltage.
V_{dsat} : is the drain source saturation voltage.
From (4), (5) and (6) results:

$$F_{out} \propto \frac{((V_{ctrl} - V_{th})V_{dsat} - \frac{1}{2}V_{dsat}^2)}{2N \times C_L} \propto V_{ctrl} \quad (7)$$

Two series of inverters are used as a buffer to protect the oscillation. When the VCO is close to its steady state, the phase and frequency of the output clock are adjusted slightly to match the phase and frequency of the input reference clock.

C. Feedback Divider

The divider divides VCO's clock to generate FBCLK to compare both phases.

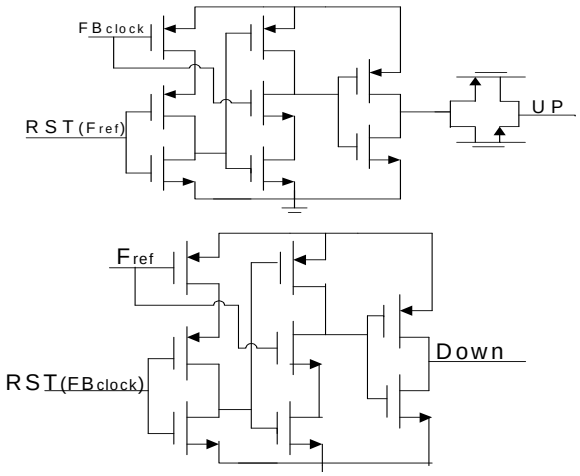

Figure 5. Phase Frequency Detector

It is made up of TSPC Flip Flop [10].

D. Simulation Results

Once the lock is achieved, as shown in Figure 10, after settling time 4µs, shown in Fig (8), the output clock would be equal to $N \times F_{ref}$.

Figure 9 shows the corresponding voltage on the loop filter capacitor as it will saturate when the output clock matches the reference clock frequency.

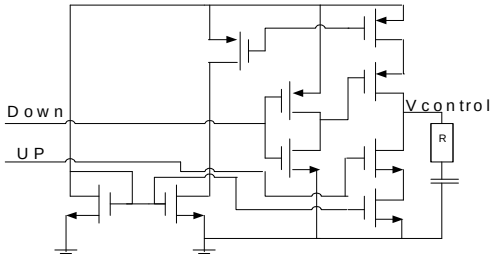

Figure 6. Charge Pump/ Loop Filter

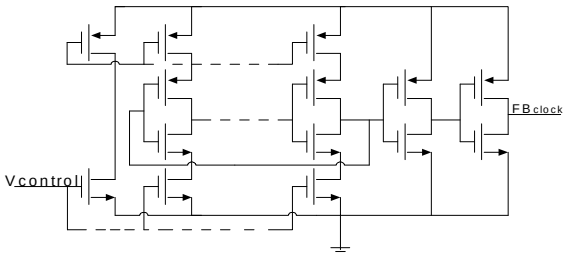

Figure 7. Voltage Controlled Oscillator

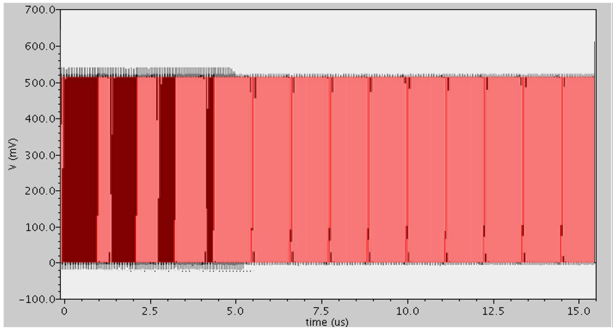

Figure 8. Transient simulation of input/output frequency, N=1

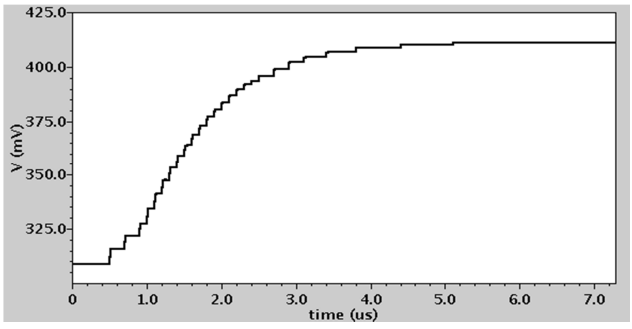

Figure 9. Evolution of voltage control

The controlled voltage is stabilized at 410 mV.

Table II gives a summary of the loop parameters in comparison with other solution.

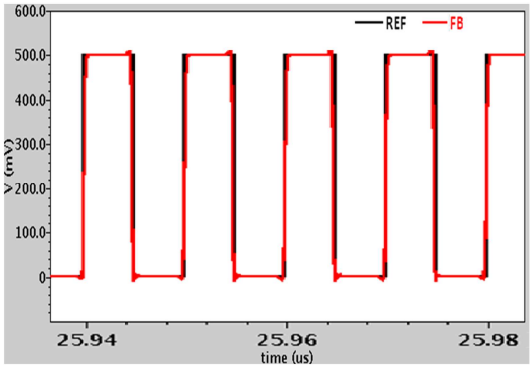

Figure 10.PLL in locked condition reference signal versus feedback signal

TABLE II. LOOP PARAMETERS FOR FIRST ARCHITECTURE

Loop parameter	This work	[11]
F_{osc}	100MHz	3MHz
K_{vco}/K_{vco}(assuming same control current)	303 MHz/V	300 MHz /V
I_{cp}	1.1µA	0.9 µA
C_p	3.61PF	10PF
C_2	--	2PF
PM	83.9°	45.4°
Power consumption	0.375PW/Hz	4.47PW/Hz
Techno	180 nm	90 nm

IV. CONCLUSIONAND FUTURE WORK

The paper presented a designed PLL with low power consumption and small loop capacitance. PFD uses reference and feedback clock to reset each other; UP and DOWN signals don't get high simultaneously, yield to low glitches for a small loop capacitance value, which is the gain as we kept low area required for the application.

CP current is reduced given that its phase noise transfer function is a LPF (decay in the band of interest) while a VCO large current to reduce its output phase noise given that its phase noise transfer function is a HPF. System and design are done to optimize the power consumption. System stability is guaranteed as PM >60°.

In our future work, we target designing this PLL to operate at higher frequency; for that reason, we have discussed above about the condition for zero PFD dead zone.

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