A Low-Voltage Folded-Cascode OP Amplifier with a Dynamic Switching Bias Circuit and Application to Switched Capacitor Filters

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***Abstract*—Wideband filters employing Operational Amplifiers (OP Amps) are required in sensing devices such as video cameras for environment sensing. A high-speed low-voltage Folded-Cascode (FC) OP Amp with a Dynamic Switching Bias (DSB) circuit capable of processing video signals, which enables low power consumption, high gain with wide bandwidths, and a wide dynamic range, was proposed. Through simulations, it was shown that the OP Amp with the reduced 3-V power supply is able to operate at a 14.3 MHz dynamic switching rate, allowing processing video signals, and a dissipated power of 57 % compared to that in the conventional 5-V power DSBFC OP Amp while keeping a 0.6 V wide output dynamic range. The 2nd-order switched capacitor Low-Pass Filter (LPF) and the 4th-order switched capacitor LPF were tested as its applications. The response of the former was near the theoretical frequency response within frequencies below 5 MHz. The sample-hold circuit in the latter was optimized considering the feed-through phenomenon. The latter showed practical level gains in frequencies over 5 MHz within a stop-band while showing a sharp roll-off near the theoretical frequency response within frequencies below 4 MHz. The power dissipation of either of these switched capacitor LPFs was also reduced to nearly 57 % of that in each switched capacitor LPF with the conventional 5-V power DSBFC OP Amp.**

Keywords-CMOS; operational amplifier; dynamic switching; switched capacitor circuit; filter.

I. INTRODUCTION

This work is an extension of work originally presented in SENSORDEVICES 2018 [1]. Wideband filters are essential for signal processing in video electronic appliances. Specifically, a wideband Low-Pass Filter (LPF) is needed in sensing devices such as a CCD (Charge-Coupled Device) camera with a monitor handling a wide bandwidth video signal of over 2 MHz. The CMOS (Complementary MOS) Switched Capacitor (SC) techniques suitable for realizing analog signal processing ICs (Integrated Circuits), have promising use in video signal bandwidth circuits. It has been demonstrated that SC techniques using CMOS Operational Amplifiers (OP Amps) are useful for implementing analog functions such as filters [2]-[5]. Although CMOS OP Amps are suitable for such filter ICs, the use of several OP Amps results in large power consumption. Especially, the power consumption of OP Amps in high speed operation becomes large because they have wideband properties. There is a possibility that this causes unstable operation.

Until now, several approaches have been considered to decrease the power consumption of OP Amps, including the development of ICs that work at low power supply voltages [6][7]. In the two-stage Folded-Cascode (FC) OP Amp operating at the low power of 1 V [7], resistive biasing and capacitive level shifter are required to increase the output voltage swing. The requirement of four resistors for the resistive biasing makes it difficult to realize as an IC. A clocked current bias scheme for FC OP Amps suitable for achieving a wide dynamic range has typically been proposed to decrease the power consumption of the OP Amp [8][9]. Since the circuit requires complicated four-phase bias-current control pulses and biasing circuits, it is not suitable for the high speed operation and results in a large layout area.

Recently, the author proposed an FC CMOS OP Amp with a Dynamic Switching Bias circuit (DSBFC OP Amp), of simple configuration, to provide low power consumption while maintaining high speed switching operation suitable for processing video signals [10]. This OP Amp operating at the 5-V power supply voltage is not necessarily enough for use in low-voltage signal processing applications under the progress of miniaturization of equipment. That is, the development of OP Amps with a still lower power supply voltage is expected to decrease their power dissipation.

In this paper, a Low-Voltage (LV) DSBFC OP Amp with the 3-V power supply voltage [1] is proposed, which enables low power consumption and is suitable for achieving wide bandwidths and realizing as an IC. The point of view in design for architecture and operation of the LV DSBFC OP Amp is discussed in Section Ⅱ. Simulation results for performance of the LV DSBFC OP Amp are shown in Section Ⅲ. As application examples of this OP Amp, its practicability for a 2nd-order SC Butterworth LPF and a 4th-order SC Butterworth LPF is also evaluated in Section Ⅳ. Finally, conclusions of this work are summarized in Section Ⅴ.

II. LOW-VOLTAGE DSB OP AMP CONFIGURATION

Figure 1 shows a configuration of an LV DSBFC OP Amp, in which the power supply voltages (±1.5 V) were reduced to 60 % of the previous ones (±2.5 V). The DSB method is also used for implementing low power

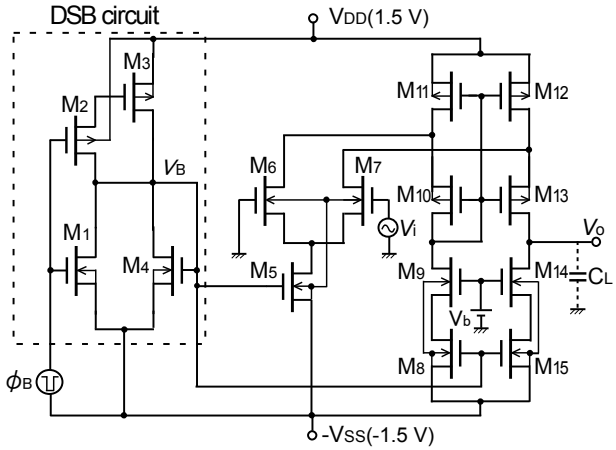

Figure 1. Configuration of the low-voltage DSBFC OP Amp.

TABLE Ⅰ. LOW-VOLTAGE DSBFC OP AMP DESIGNED VALUES.

FET	W/L (μm/μm)	FET	W/L (μm/μm)
M1	15/2.5	M6, M7	2000/2.5
M2	30/2.5	M8, M15	92/2.5
M3	50/4	M9, M14	1055/2.5
M4	44/6	M10, M13	2000/2.5
M5	187/2.5	M11, M12	390/2.5

consumption. When the power supply voltage is simply reduced, the gain of OP Amps is restrained and their bandwidths become low. So, in the newly developed circuit, each FET (Field Effect Transistor) size of the LV DSBFC OP Amp was optimized to achieve high-speed switching operation of 14.3 MHz. This OP Amp has a DSB circuit suitable for low power dissipation and an FC OP Amp to achieve a wide dynamic range even in low power supply voltages. The DSB circuit consists of a bias circuit of M1-M4. The FC OP Amp consists of a current mirror of M10-M13 and current sources of M8, M9, M14, and M15. The current sources M5, M8, and M15 of the FC OP Amp are controlled by switching a bias voltage V_B of the DSB circuit dynamically from V_B* to -1.5 V to reduce the power consumption still more. Table Ⅰ shows its designed values. A minimum channel length of p-MOS FETs and n-MOS FETs is 2.5 μm. In order to achieve almost the same transconductance g_m as that in the conventional 5-V power DSBFC OP Amp, a channel width W of M11 and M12 and that of M10 and M13, in p-MOS current mirror circuits, were increased by nearly fourfold and twofold, respectively. Each W of n-MOS current sources M9, M14, M8, and M15 was increased by nearly one and a half. The bias voltage of V_B* at the on state of the FC OP Amp was adjusted to nearly 0 V (larger than the conventional one) to decrease W of the current source M5 maintaining a high switching speed of the DSB circuit. W of M1-M3 was increased by over twofold. W of M4 was adjusted to an optimum value. The bias voltage Vb of the current source consisting of M9 and M14 was set at 0.15 V.

In the DSB circuit, when an external control pulse ϕ_B driving an inverting switching circuit of M1-M4 is -1.5 V, the OP Amp turns on by setting V_B at an appropriate level of nearly 0 V by enabling M3 and M4 to operate in the saturation region, and operates normally as an operational amplifier. Conversely, when ϕ_B becomes 1.5 V, the OP Amp turns off by setting V_B at nearly -1.5 V, enabling M1 to operate in a low impedance and M3 in a high impedance. This high impedance status of M3 occurs because the gate of M3 is set at a potential determined by the capacitive coupling between gate and source of M2 and between gate and drain of M3 at the transition of ϕ_B to 1.5 V. Therefore, the OP Amp does not dissipate power at all during this off period, which brings about low power consumption.

III. SIMULATION RESULTS

The LV DSBFC OP Amp performance was tested through SPICE simulations. The power supply voltages V_{DD} and Vss are 1.5 V. Typical performances compared with those of the conventional DSBFC OP Amp with a power supply of 5 V are shown in Table Ⅱ. The values of parameters of open loop gain, phase margin, unity gain frequency, slew rate, and settling time are almost the same as those in the conventional 5-V power DSBFC OP Amp. As the inherent static nonlinearity of the LV DSBFC OP Amp, the total harmonic distortion THD for the 10 kHz input signal, enabling 0.6 Vp-p to output, was 0.73 %, which is a little large compared to the conventional one. However, this is less than 1 %.

The LV DSBFC OP Amp operated in a dynamic switching mode with a Duty Ratio (DR) of 50 % and a switching frequency, *fs*, of 14.3 MHz as shown in Figure 2. The output sine wave voltage for the input signal of 1 mV was nearly equal to that in the static operation mode of this OP Amp. Like this, the distortion by the dynamic operation seems to be hardly seen. In the dynamic switching operation mode of 50 % duty ratio, the power dissipation was 9.3 mW, which is 66 % of that (14.0 mW) observed in the static operation mode as shown in Figure 3. This is also 57 % of that (16.3 mW) of the conventional 5-V power DSBFC OP Amp. This shows this OP Amp's extremely low power consumption characteristics due to the reduced effect of power supply voltages (60 % of that in the conventional 5-V power

TABLE Ⅱ. TYPICAL PERFORMANCES FOR THE LOW-VOLTAGE 3-V POWER AND CONVENTIONAL 5-V POWER DSBFC OP AMPS. C_L=1 PF.

Performance parameters	3V power DSBFC OP Amp - this work	5V power DSBFC OP Amp
Power supply voltages	±1.5 V	±2.5 V
Switching frequency *fs*	14.3 MHz	14.3 MHz
Open loop gain Ao	47.1 dB	51 dB
Phase margin θ	32.8 degrees	34.2 degrees
Unity gain frequency *fu*	603.7 MHz	709 MHz
Slew rate SR (C_L=10 pF)	131 V/μs	140 V/μs
Settling time ts	10 ns	12 ns
Distortion THD (*fin*=10 kHz, *Vo*=0.6 Vp-p)	0.73%	0.40%
Power dissipation (C_L=5 pF) in 50 % switching duty ratio	9.3 mW	16.3 mW

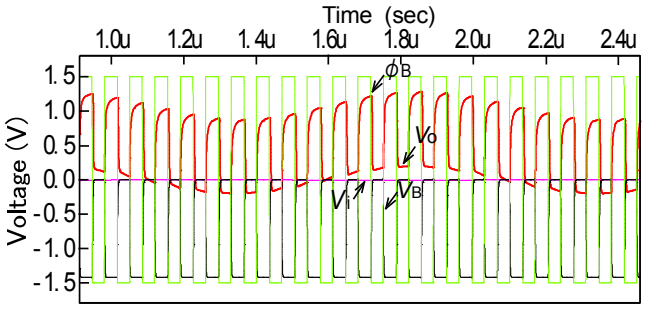

Figure 2. Simulation waveforms of the low-voltage DSBFC OP Amp. Input signal frequency f_{in}=1 MHz, V_{in}=1 mV, f_S=14.3 MHz, C_L=2 pF.

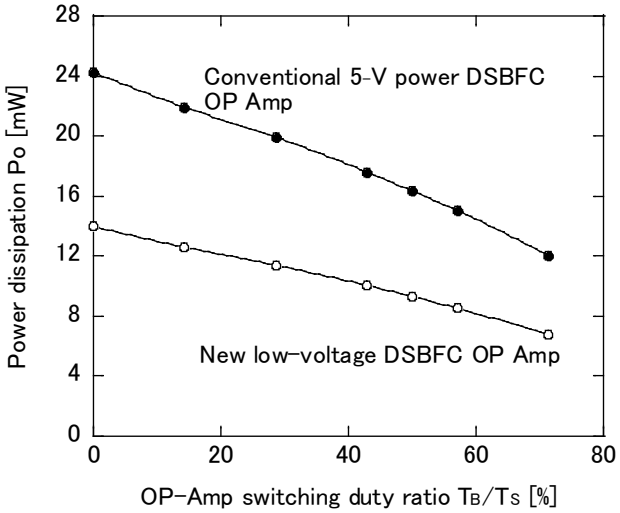

Figure 3. Power dissipation vs. OP-Amp switching duty ratio in the DSB mode. f_S=14.3 MHz, C_L=5 pF.

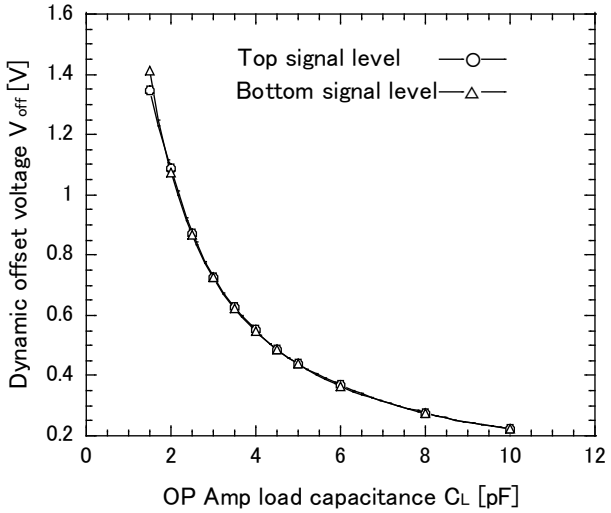

Figure 4. Dynamic offset voltage vs. OP Amp load capacitance in the LV DSBFC OP Amp. f_{in}=0.5 MHz, V_{in}=1 mV.

DSBFC OP Amp) and dynamic switching operation.

The LV DSBFC OP Amp switches dynamically to the off state. At this time, though p-MOSFETs M11 and M12 remain the on-state, MOSFETs M6, M7, M9, M10, M13, and M14 change to the on-state weakly. The output terminal of *Vo* of the OP Amp is set at a voltage depending on the load capacitance through the capacitive coupling between the drain and the gate of the MOSFET M13. So, a large output swing in *Vo* occurs at the off-state transition. A dynamic offset voltage Voff (defined as the difference of the on-state and the off-state output voltages) at the off-state transition of the OP Amp vs. load capacitance C_L was tested (Figure 4). In small load capacitances less than 1.5 pF, top and bottom signal levels of the dynamic off swing do not match. This causes distortion at an output signal of the OP Amp. Therefore, we can see that the load capacitance C_L over 2 pF is desirable for its operation.

IV. APPLICATION TO SC LPFS

To demonstrate the practicability of the above LV DSBFC OP Amp, the feasibility of its application to two kinds of SC LPFs was investigated.

A. 2nd-Order SC LPF

At first, a 2nd-order SC IIR (Infinite Impulse Response) LPF with the Butterworth frequency characteristic was tested. When a sampling frequency f_S=14.3 MHz (equal to four times of NTSC (National Television System Committee) color sub-carrier frequency 3.58 MHz) and a cutoff frequency f_C=2 MHz, respectively, were chosen for this LPF, the discrete-time transfer function using the z-transform is given by (1) [11].

$$H_1(z) = -\frac{0.11735(1+z^{-1})^2}{1-0.82524z^{-1}+0.29464z^{-2}} \quad (1)$$

The circuit configuration and operation waveforms realizing this transfer function are shown in Figures 5 and 6, respectively [11]. This SC LPF was designed referencing an SC biquadratic circuit with integrators in the reference [12]. It consists of a sample-hold circuit with a holding capacitor Cs1 and a CMOS sampling switch controlled by ϕ_{SH}, CMOS switches ϕ_1, ϕ_2 for charge transfer, capacitors A-E, G, and I, and two LV DSBFC OP Amps (OP Amps 1 and 2). In this SC LPF, in order to enable easily to determine the capacitance value of each capacitor, the coefficient of A is set to be equal to that of B. Capacitors in this SC LPF can be basically divided into two groups. In one group (C, D, E, and

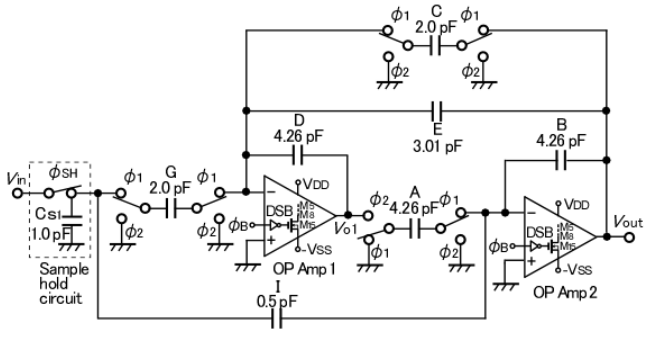

Figure 5. Configuration of the 2nd-order SC LPF.

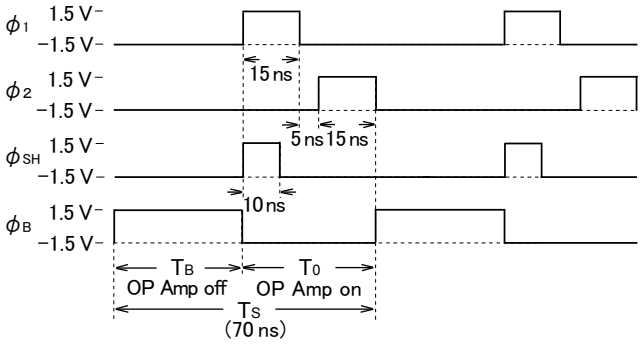

Figure 6. Operation waveforms of the 2nd-order SC LPF.

G), charges are supplied to OP Amp 1. In another group (A, B, and I), charges are supplied to OP Amp 2. Even if a capacitance of each capacitor group is multiplied by constant times, the transfer function of the SC LPF does not change because the multiplication of two capacitor coefficients is performed in the numerator and the denominator of its transfer function, respectively. Therefore, capacitances of integral capacitors B and D are here chosen as a reference capacitance in each group and each coefficient of B and D is normalized to 1. At this time, 1 for every normalized coefficient of A, B, and D is obtained because A and B were set to the same coefficient as described above. In Figure 5, when the coefficients of A, B, and D are normalized to 1, other coefficients are determined in the following.

I=K=0.11735

G=2K+2I=0.4694

C=1+b_1+b_2=0.4694

E=1-b_2=0.70536

Here, b_1=-0.82524 and b_2=0.29464. When the smallest coefficient of I (=0.11735) is replaced as a reference capacitance of 0.5 pF, each capacitance in the SC LPF IC is set in proportion to the above coefficient as shown in Figure 5.

Because an SC LPF's input signal is desirable to be maintained by a sample-hold circuit for stabilizing, this sample-hold circuit is applied to the SC LPF. In this case, the transfer function is multiplied by the following zero-order hold function due to a sample-hold effect.

$$H_s(j\omega)=\frac{\sin(\omega T_s/2)}{\omega T_s/2} \quad (2)$$

Here, Ts represents the one cycle period of sampling pulses. Therefore, when the transfer function (1) is replaced using $z=e^{j\omega T_s}$, the magnitude of the transfer function of the 2nd-order SC LPF considering the sample-hold effect is given by (3).

$$|H(j\omega)|=\frac{\sin(\omega T_s/2)}{\omega T_s/2}\ |H_1(j\omega)| \quad (3)$$

Here, $|H_1(j\omega)|$ in (3) is the following function.

$$|H_1(j\omega)|=\frac{0.2347(1+\cos(\omega T_S))}{\sqrt{1.76783-2.13678\cos(\omega T_S)+1.65128\cos(2\omega T_S)}} \quad (4)$$

The sampling switch was designed to a channel width / channel length W/L=105/2.5 (μm/μm) for each of p-MOSFET and n-MOSFET. Other CMOS switches were designed to 75/2.5 (μm/μm). CMOS switches are turned on and off by non-overlapping two-phase clock pulses ϕ_1, ϕ_2, swinging from -1.5 V to 1.5 V. These sampling and CMOS switches were designed to have a balanced structure with each equal L and W of p-MOS and n-MOS FETs to suppress a feed-through phenomenon as much as possible. This phenomenon is easy to be caused by a capacitive coupling between gate and output terminals.

Major CMOS process parameters are given as a gate insulating film thickness t_{ox}=50 nm, a p-MOSFET threshold voltage V_{TP}=-0.6 V, and an n-MOSFET threshold voltage V_{Tn}=0.6 V.

The operation principle of this SC LPF is as follows. The output signal V_{o1} of OP Amp 1 is obtained as an additional output of an integrated signal of V_{in} using a negative integrator (capacitor D, G SC circuit, and OP Amp 1), an integrated signal of V_{out} using a negative integrator (capacitor D, C SC circuit, and OP Amp1), and a signal multiplied V_{out} by E/D. The output signal V_{out} is an additional output of an integrated signal of V_{o1} using a positive integrator (A SC circuit, capacitor B, and OP Amp 2), and a signal multiplied V_{in} by I/B. V_{out} is basically fed back to an input of OP Amp 1 like this. V_{in} is also integrated twice and added after being decreased by an appropriate capacitance ratio. Due to these integration using positive and negative integrators, addition and feedback operations, the function of LPF is achieved.

The actual operation of the SC LPF is described in the following. In this SC LPF, charge transfer operations through clock pulses ϕ_1, ϕ_2, are performed during the on-state period T_o of the LV DSBFC OP Amps (when the control pulse ϕ_B is set at -1.5 V). The off-state period T_B (the remaining period of the one cycle period Ts) is separately provided to realize low power consumption for this SC LPF. An input signal V_{in} is sampled during the sampling phase of ϕ_{SH} (10 ns) in the on-state period T_o. After sampling operation, its corresponding charge is stored on the holding capacitor C_{s1}. The voltage at the off-state transition of ϕ_{SH} is transferred to an output terminal V_{out}, charging all capacitors, during the clock phase of ϕ_1. During the subsequent clock phase of ϕ_2, each charge of two capacitors C and G is discharged and each charge of remaining capacitors is redistributed. During such on-state period of T_o, the LV DSBFC OP Amps turn on by setting a bias voltage of V_B at an appropriate level of nearly 0 V and operate normally as operational amplifiers.

Subsequently, ϕ_B becomes 1.5 V at the off-state transition of the OP Amps, while ϕ_2 is switched off. During this off period T_B, the OP Amps turn off and so these do not dissipate power at all. Therefore, when T_B is set relatively long as compared to the one-cycle period Ts, the power

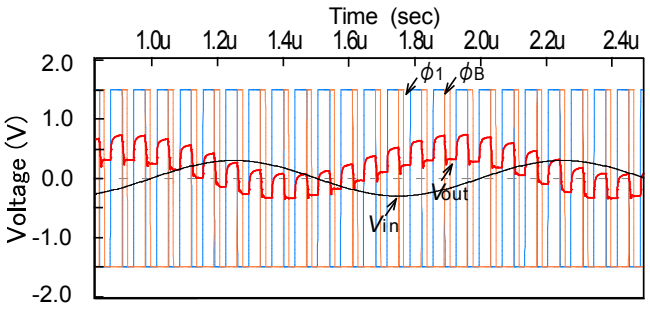

Figure 7. Simulation waveforms for the 2nd-order SC LPF. V_{in}=0.3 V_0-p, f_{in}=1 MHz, C_L=4 pF.

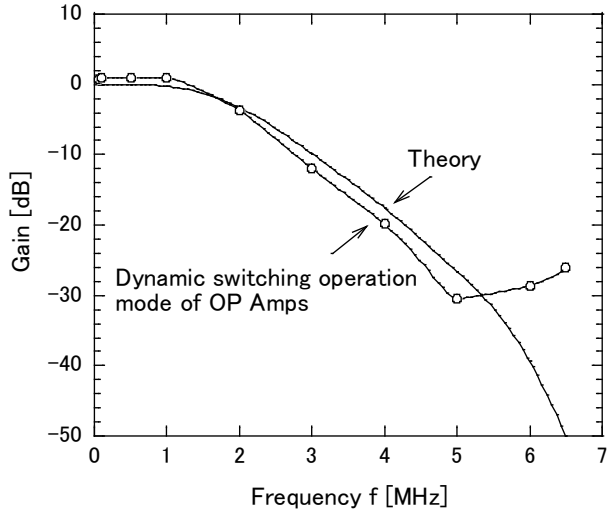

Figure 8. Frequency response of the 2nd-order SC LPF in the DSB mode of the OP Amp. T_B=35 ns.

consumption of the SC LPF is expected to become lower than that observed in ordinary static operation for an SC LPF using conventional OP Amps.

Operation waveforms for an input signal of 1 MHz with an amplitude of 0.3 V and an output load of 4 pF are shown in Figure 7. In the dynamic switching operation, an output load of the LV DSBFC OP Amp increases to nearly 5 pF including internal capacitances of the SC LPF. For the pass-band frequency signal (≦2 MHz), almost the same signal as the input one was obtained. The frequency response of the SC LPF in the dynamic switching operation of the LV DSBFC OP Amp is shown in Figure 8. Figure 9 shows the frequency response of the SC LPF in the static operation mode of OP Amps. Both frequency responses are almost the same. This means that there is almost no gain deterioration by employing the DSB operation of the LV DSBFC OP Amps. The frequency response was near the theoretical one from 100 kHz to near 5 MHz. In the high frequency range over 6 MHz, it deteriorated due to a sampling phase effect. The gain below -26 dB was obtained at over 6 MHz within the stop-band. Though this stop-band gain is not low enough, it is expected to be improved by making the roll-off steeper through the increase of filter order.

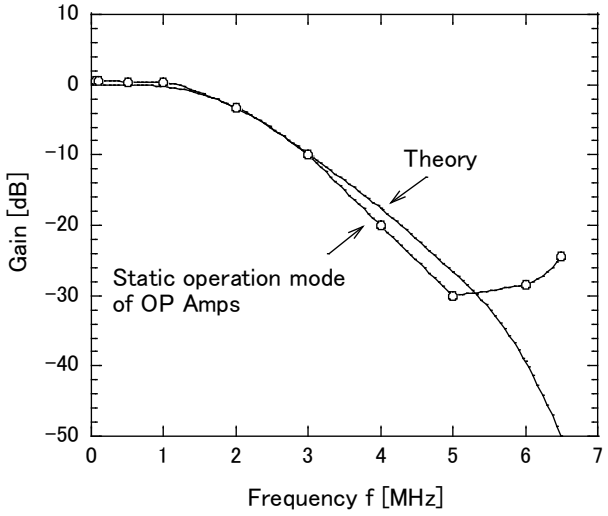

Figure 9. Frequency response of the 2nd-order SC LPF in the static operation mode of the OP Amp. ϕ_B = -1.5 V.

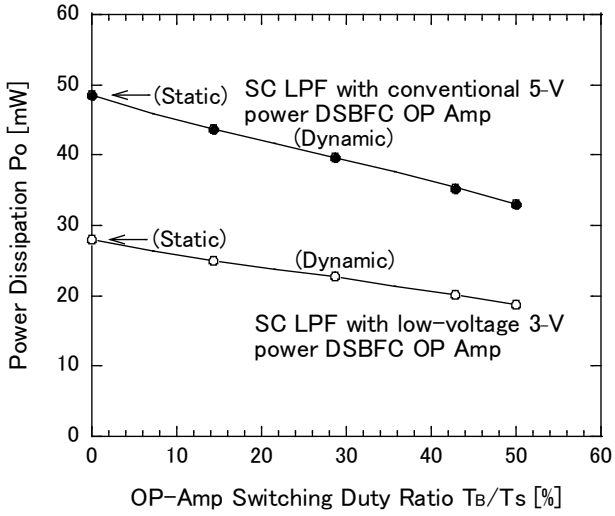

Figure 10. Power dissipation vs. OP Amp switching duty ratio in the 2nd-order SC LPFs. f_{in}=1 MHz.

The power dissipation vs. the OP Amp switching duty ratio in the 2nd-order SC LPF is shown in Figure 10. The power dissipation of the SC LPF itself decreased in proportion to the off period T_B of the OP Amp. In the dynamic switching operation mode of T_B=35 ns (DR=50 %), the power dissipation of the SC LPF (18.7 mW) was reduced to 66.8 % as compared to that in the static operation of the OP Amps (28.0 mW). Thus, the dynamic switching operation of the LV DSBFC OP Amp is useful for reducing the power dissipation of the SC LPF. This power dissipation was 56.8 % compared to that in the SC LPF using the conventional 5-V power DSBFC OP Amp (32.9 mW). This low power characteristic was realized by the low power supply voltages and dynamic switching operation.

B. 4th-Order SC LPF

As another application example of the above LV DSBFC OP Amp, a 4th-order SC IIR LPF with the Butterworth frequency characteristic was tested. The high filter order of the fourth was selected because it is expected to achieve a sharp roll-off gain characteristic. The 4th-order SC LPF was designed to achieve a roll-off characteristic with a gain of below -30 dB at over 4 MHz within the stop-band. The other design condition was set as follows. That is, the sampling frequency *f*s=14.3 MHz and the cutoff frequency *f*c=2 MHz were chosen as the same values as those in the 2nd-order SC LPF, that enables it to process video signals. Under this condition, the discrete-time transfer function is given using the z-transform by (5). That is, (5) can be rewritten like (6) considering the independence of two transfer functions.

$$H_2(z) = \frac{-0.10573(1+z^{-1})^2}{1-0.74578z^{-1}+0.16869z^{-2}} \cdot \frac{-0.13976(1+z^{-1})^2}{1-0.98582z^{-1}+0.54484z^{-2}} \quad (5)$$

$$H_2(z) = H_{21}(z) \cdot H_{22}(z) \quad (6)$$

The circuit configuration realizing this transfer function is shown in Figure 11 [13]. Its operation waveforms are the same as those in the 2nd-order SC LPF shown in Figure 6. The 4th-order SC LPF was designed referencing a SC biquadratic circuit with integrators [12] in the same way as the 2nd-order SC LPF. This SC LPF consists of two-stage biquadratic circuits cascading two 2nd-order SC LPFs of LPF1 and LPF2, provided with a sample-hold circuit with a holding capacitor C_{S1} and a sampling switch controlled by ϕ_{SH}, CMOS switches ϕ_1 and ϕ_2, capacitors A_1, B_1, C_1, D_1, E_1, G_1, I_1, A_2, B_2, C_2, D_2, E_2, G_2, and I_2, and four LV DSBFC OP Amps. The transfer function of this SC LPF circuit is shown in (7).

$$H_2(z) = (-)\frac{D_1I_1+(A_1G_1-2D_1I_1)z^{-1}+D_1I_1z^{-2}}{D_1B_1+(A_1C_1+A_1E_1-2D_1B_1)z^{-1}+(D_1B_1-A_1E_1)z^{-2}} \cdot (-)\frac{D_2I_2+(A_2G_2-2D_2I_2)z^{-1}+D_2I_2z^{-2}}{D_2B_2+(A_2C_2+A_2E_2-2D_2B_2)z^{-1}+(D_2B_2-A_2E_2)z^{-2}} \quad (7)$$

The same way of thinking as that in the 2nd-order SC LPF is applicable in determining each capacitance of LPF1 (A_1, B_1, C_1, D_1, E_1, G_1, and I_1) and LPF2 (A_2, B_2, C_2, D_2, E_2, G_2, and I_2) as well. As shown in (5) and (6), each transfer function for the LPF1 and LPF2 is independent of each other. Therefore, the normalization of the coefficients in the LPF1 and LPF2 can be made independently. In Figure 11, when the coefficients of A_1, B_1, D_1, A_2, B_2, and D_2 are normalized to 1, the transfer function (7) is changed to (8).

$$H_2(z) = (-)\frac{I_1+(G_1-2I_1)z^{-1}+I_1z^{-2}}{1+(C_1+E_1-2)z^{-1}+(1-E_1)z^{-2}} \cdot (-)\frac{I_2+(G_2-2I_2)z^{-1}+I_2z^{-2}}{1+(C_2+E_2-2)z^{-1}+(1-E_2)z^{-2}} \quad (8)$$

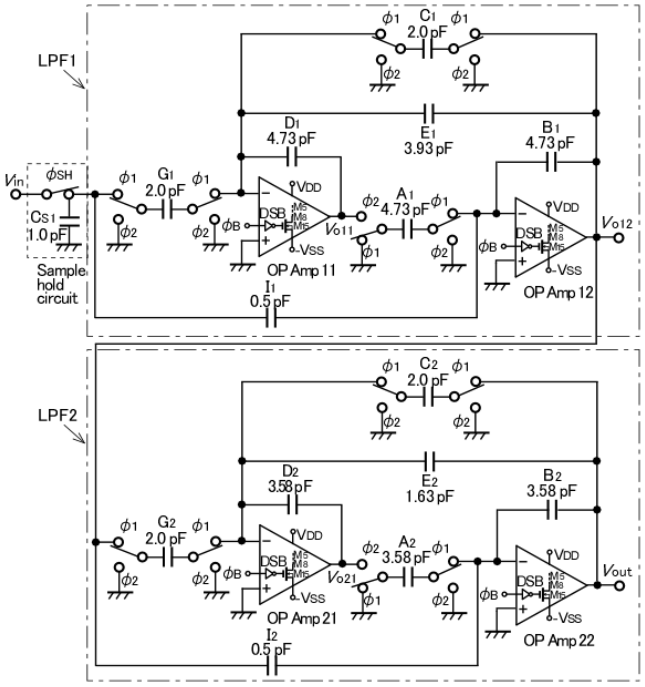

Figure 11. Configuration of the 4th-order SC LPF.

Because the coefficients in (8) are equal to those in (5), other coefficients are determined as follows.

$I_1=K_1=0.10573$

$G_1=4K_1=0.42292$

$C_1=1+b_{11}+b_{12}=0.42291$

$E_1=1-b_{12}=0.83131$

$I_2=K_2=0.13976$

$G_2=4K_2=0.55904$

$C_2=1+b_{21}+b_{22}=0.55902$

$E_2=1-b_{22}=0.45516$

Here, b_{11}=-0.74578, b_{12}=0.16869, b_{21}=-0.98582, and b_{22}=0.54484. When the smallest coefficients of I_1=0.10573 in the LPF1 and I_2=0.13976 in the LPF2 are replaced as a reference capacitance of 0.5 pF, each capacitance in the 4th-order SC LPF IC is set in proportion to the above coefficients as shown in Figure 11. A sample-hold circuit is also applied in this SC LPF to maintain its input signal for stabilizing. At this time, the transfer function (5) is multiplied by the zero-order hold function (2) in the same way as that in the previous 2nd-order SC LPF. Therefore, when the transfer function (5) or (6) is replaced using $z=e^{j\omega T_s}$, the magnitude of the transfer function of the 4th-order SC LPF considering the sample-hold effect is given by

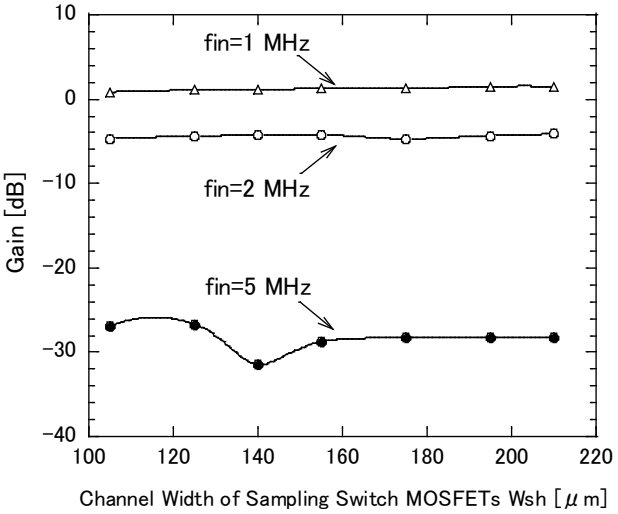

Figure 12. Gain vs. channel width of sampling switch MOSFETs. Cs1=1 pF.

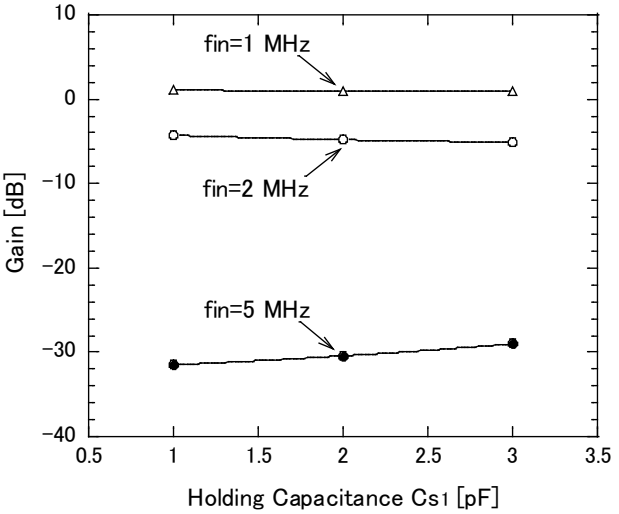

Figure 13. Gain vs. holding capacitance. W/L of sampling switch MOSFETs=140/2.5 (μm/μm).

(9).

$$|H(j\omega)|=\frac{\sin(\omega T_S/2)}{\omega T_S/2}\ |H_{21}(j\omega)|\cdot|H_{22}(j\omega)| \qquad (9)$$

Here, $|H_{21}(j\omega)|$ and $|H_{22}(j\omega)|$ in (9) are the following functions, respectively.

$$|H_{21}(j\omega)|=\frac{0.21146(1+\cos(\omega T_S))}{\sqrt{1.58464-1.74317\cos(\omega T_S)+0.33738\cos(2\omega T_S)}} \qquad (10)$$

$$|H_{22}(j\omega)|=\frac{0.27953(1+\cos(\omega T_S))}{\sqrt{2.26869-3.04587\cos(\omega T_S)+1.08968\cos(2\omega T_S)}} \qquad (11)$$

In this 4th-order SC LPF, the load capacitances of LV DSBFC OP Amps were set as a 2 pF because twofold capacitances as compared to that in the 2nd-order SC LPF are loaded. The sample-hold circuit in this SC LPF was designed

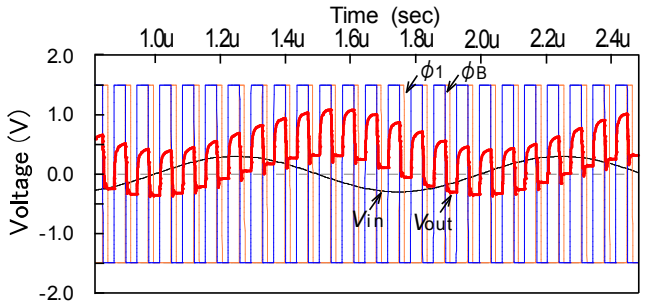

Figure 14. Simulation waveforms for the 4th-order SC LPF. V_{in}=0.3 V_0-p, f_{in}=1 MHz, C_L=2 pF.

as follows considering the feed-through phenomenon.

Figure 12 shows the gain of the 4th-order SC LPF in the DSB mode of the LV DSBFC OP Amp vs. the channel width Wsh of each of p-MOSFET and n-MOSFET in the sampling switch. The gain of the 4th-order SC LPF became minimum at a Wsh of nearly 140 μm when the input signal frequency *f*in is equal to 5 MHz within the stop-band, while its gain remains almost unchanged for input signals of 1 and 2 MHz within the passband. This is thought to be due to the following phenomenon. When Wsh is larger than 140 μm, the feed-through via the difference of capacitive coupling between gate and output terminals of the above MOSFETs does not become negligible at the off-state transition of the sampling switch and so the gain corresponding to *f*in=5 MHz increases. When Wsh is smaller than this value, a driving ability of the sampling switch becomes insufficient, which brings about an increase of the gain. Like this, Wsh of the sampling switch is optimized to 140 μm. The feed-through in the sample-hold circuit is also dependent on a holding capacitance. Figure 13 shows the gain of the 4th-order SC LPF in the DSB mode of the LV DSBFC OP Amp vs. the holding capacitance. As the holding capacitance Cs1 increases, the gain corresponding to *f*in=5 MHz in the stop-band deteriorates little by little. That is, we can see that a smaller capacitance is desirable as Cs1. So, the Cs1 of 1 pF in this 4th-order SC LPF was also chosen.

Other CMOS switches were designed to 75/2.5 (μm/μm), which is the same one as that in the 2nd-order SC LPF. In this 4th-order SC LPF consisting of a cascade connection of two different 2nd-order SC LPFs of LPF1 and LPF2 and a sample-hold circuit for common use, the operation principle is similar to the previous 2nd-order SC LPF

Operation waveforms for an input signal of 1 MHz with an amplitude of 0.3 V and an output load of 2 pF are shown in Figure 14. In the 4th-order SC LPF, the output signal amplitude nearly close to the input signal was also obtained for passband frequency signals. The frequency response of the 4th-order SC LPF in the dynamic switching operation of the LV DSBFC OP Amps is shown in Figure 15. The roll-off characteristic in near 3-4 MHz was greatly improved compared to that in the 2nd-order SC LPF. The response was near the theoretical one from 100 kHz up to near 4 MHz. At 4 MHz within the stop-band, the gain below -28 dB was obtained. In the high frequency range over 5 MHz within the stop-band, although it deteriorated due to a sampling phase

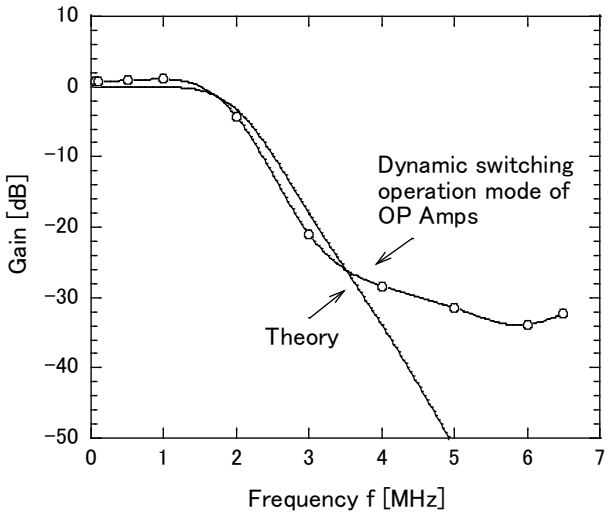

Figure 15. Frequency response of the 4th-order SC LPF in the DSB mode of the LV DSBFC OP Amp. T_B=35 ns.

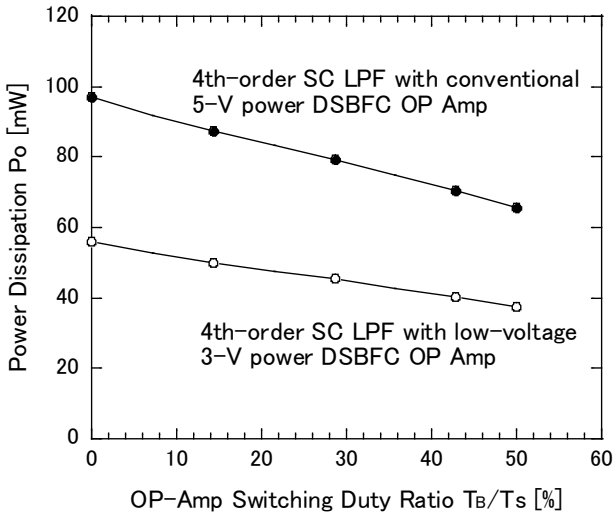

Figure 16. Power dissipation vs. OP Amp switching duty ratio in the 4th-order SC LPFs. f_{in}=1 MHz.

effect, the gain below -31.5 dB (a practical level) was achieved. In this way, a wide stop-band with a high attenuation (a sharp roll-off characteristic) in the high frequency response became possible due to the two-stage biquadratic SC LPF configuration with the increased filter order of the fourth. Like this, it is clear that the LV DSBFC OP Amp is also applicable to the high-order SC LPF.

The power dissipation vs. the OP-Amp switching duty ratio in the 4th-order SC LPF with the 3-V power LV DSBFC OP Amps compared to that in the 4th-order one with conventional 5-V power DSBFC OP Amps is shown in Figure 16. The power dissipation of the 4th-order SC LPF with the LV DSBFC OP Amps itself decreased in proportion to the off-state period T_B of the OP Amps. In the dynamic switching operation mode of T_B=35 ns (=50 % switching duty ratio) and $\phi_1 = \phi_2$ =15 ns, the power consumption of this 4th-order SC LPF (37.4mW) decreased to 66.8 % as

TABLE Ⅲ. TYPICAL PERFORMANCES FOR THE 2ND-ORDER AND 4TH-ORDER SC LPFS EMPLOYING THE LV DSBFC OP AMPS.

Performance parameters	Simulation results	
	4th-order SC LPF	2nd-order SC LPF
Sampling and switching frequency fs	14.3 MHz	14.3 MHz
Input signal amplitude	0.3 $V_{0\text{-}P}$	0.3 $V_{0\text{-}P}$
Cutoff frequency fc	2 MHz	2 MHz
Gain at a stop-band over 5 MHz	≦-31.5 dB (Dynamic mode)	≦-26.0 dB (Dynamic mode)
Power consumption	56.0 mW (Static)	28.0 mW (Static)
	37.4 mW (Dynamic:T_B/T_S=50 %)	18.7 mW (Dynamic:T_B/T_S=50 %)

compared to that in the static operation of the LV DSBFC OP Amps (56 mW). This value is twice as large as that in the 2nd-order SC LPF with the LV DSBFC OP Amps (18.7 mW) because the 4th-order SC LPF consists of a cascade-connection of two 2nd-order SC LPFs. However, the power consumption of this 4th-order SC LPF with the LV DSBFC OP Amps at 50 % switching duty ratio was reduced to 56.9 % compared to that in the 4th-order SC LPF with conventional 5-V power DSBFC OP Amps (65.7 mW). Thus, even when the DSBFC OP Amps are applied to the two-stage biquadratic circuits of SC LPF, the dynamic operation of these LV DSBFC OP Amps enabling low power consumption as compared to their static operation is also useful for reducing the power consumption of SC LPF. Typical characteristics of the 4th-order SC LPF compared with those of the 2nd-order SC LPF employing the LV DSBFC OP Amps are listed in Table Ⅲ.

V. CONCLUSIONS

A high-speed Low-Voltage (LV) Folded-Cascode (FC) Operational Amplifier (OP Amp) with a Dynamic Switching Bias (DSB) circuit capable of processing video signals, which enables low power consumption, high gain with wide bandwidths, and a wide dynamic range, was proposed. Through simulations, it was shown that the OP Amp with the reduced 3-V power supply is able to operate at a 14.3 MHz dynamic switching rate, allowing processing video signals, and a dissipated power of 57 % compared to that in the conventional 5-V power DSBFC OP Amp while keeping a 0.6 V wide output dynamic range. The response of the 2nd-order Switched Capacitor Low-Pass Filter (SC LPF) tested as its application was near the theoretical frequency response within frequencies below 5 MHz. The power dissipation of this LPF was also reduced to 56.8 % of that in the 2nd-order SC LPF with conventional 5-V power DSBFC OP Amps. As another application of the LV DSBFC OP Amps, the 4th-order SC LPF was tested to achieve a practical sharp roll-off gain characteristic. The roll-off response of this 4th-order SC LPF was greatly improved compared to that in the 2nd-order SC LPF. At over 5 MHz within the stop-band, a practical level gain below -31.5 dB was achieved. The power consumption of this 4th-order SC LPF decreased to 56.9 % of that in the 4th-order SC LPF with conventional 5-V power DSBFC OP Amps.

Thus, it was confirmed that the 3-V power DSBFC OP

Amp is useful for high speed operation, low power consumption, and greatly reducing the power dissipation of the SC LPFs. This circuit should be useful for the realization of low-power wide-band signal processing ICs. For example, it has a possibility of changing current A/D (Analog-to-Digital) converters, D/A (Digital-to-Analog) converters, and active-RC LPFs in CCD cameras into low-power SC circuits employing this LV DSBFC OP Amp, and of realizing low-power SC versions instead of current SC Amps for prevention of the deterioration of CCD camera's output signal. It has also applicability to Amps and/or LPFs required in various kinds of sensing devices and video equipment. Furthermore, it is noteworthy that the performance is expected to be improved still more by employing MOSFETs with a minimum shorter channel length than 2.5 μm used in this work.

As shown above, although the frequency response was improved to a practical level by increasing the filter order, there might be a limitation in the filter order, because one OP Amp per one order LPF must be used and so power dissipation will increase in proportion to the filter order.

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