Low-Cost Technology for the Integration of Micro- and Nanochips into Fluidic Systems on Printed Circuit Board: Fabrication Challenges

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***Abstract*—Nowadays, micro- and nanochips are usually fabricated with Silicon and/or glass. A simple, low-cost and reliable integration packaging method that provides flexibility to the incorporation of electronic and fluidic devices into a system has not been fully developed yet. The use of Printed Circuit Board material as substrate to create dry film resist microfluidic channels is the core technology to provide such an integration method. The feasibility and potential of the proposed packaging method is demonstrated in this work.**

Keywords - dry film resist, printed circuit board, inkjet printing, integration, low-cost.

I. INTRODUCTION

This paper is an extension of the work presented in [1] where the use of the TMMF dry film resist (DFR) from Tokyo Ohka Kogyo Co., Ltd. to create microfluidic channels on top of printed circuit board (PCB) to facilitate the access to nanofluidic channels is treated.

Microfluidic devices fabricated with dry film resist and Silicon (Si) and/or glass substrate have previously been reported [2] [3] [4]. Moreover, nanofluidic devices are usually fabricated with Silicon and/or glass [3] [5] [6] [7] [8]; even if nano-imprint technologies are used to fabricate them, a rigid substrate (usually glass) is required [9] [10]. What concerns the microelectronic chips; those are usually fabricated with Silicon.

The use of Silicon and/or glass to build fluidic systems elevates their cost [11] and the reliable fluidic connection of nanofluidic devices to the outside world still needs to be optimized in order to reduce costs and simplify the fabrication process.

Furthermore, a reliable method that combines great flexibility at integrating microelectronic devices in fluidic systems and low-costs are necessary to enable a broad use of microfluidic devices in quotidian life instead of expensive and voluminous equipment.

A low-cost fabrication method for microfluidic channels on top of a substrate composed by a micro- or nanochip inlaid in PCB material is presented. Inkjet printed interconnections are proposed to provide electrical connection between the chip(s) and the PCB electronics.

Following this approach, the chip(s) can be kept small in size and simple (standard) in technology thus decreasing costs. Furthermore, even if the silver ink and Rogers substrate have a relatively high cost, the overall cost is still lower than fabricating the devices with only Silicon and glass; even if some of the materials present relatively long curing times due to the low curing temperatures, still a device can be fabricated, with this technology, in less than seven days.

In addition, the low-cost PCB facilitates the fluidic and electrical connections to the outside world allowing the integration of micro- and nanodevices in a simple, robust and fast way.

In this work, the principle of the packaging integration technology is explained. In Section III, the physical properties of the materials used are presented. In Section IV, the fabrication process is detailed. Then, the challenges associated with the fabrication process are treated; first the challenges associated with the inlaying of the chip(s) in the PCB to form the substrate are described, followed by the fabrication of DFR fluidic channels on the substrate, and finally the challenges associated with the inkjet printing of electrical interconnections are discussed. The common factor to each challenge is the use of different materials as a substrate. Finally, the TMMF microfluidic interconnection is tested against leakage and the compatibility of the materials is studied by means of a thermal shock test in order to determine delamination. In addition, the suitability of the use

of inkjet printing technology for the creation of the electrical interconnections is studied by determining its performance under drastic temperature changes. To finalize this work, conclusions and future work are presented.

II. PRINCIPLE

The key material enabling the integration of micro- and nanochips into fluidic systems based on the lamination of DFR on PCB is a non-conductive adhesive (NCA).

The already fabricated chips are inlaid on the PCB material by means of a NCA. The chip(s) together with the PCB material compose the substrate for the fabrication of the microchannels that run over the chip. The microchannels are realized in dry film resist.

Concerning the electric access to the chip(s), inkjet printed interconnection lines are created between the electrical contacts of the chip(s) and the pads on the PCB.

Figure 1a shows a schematic of the concept when integrating a nanofluidic chip using the proposed technology; in this case the DFR microfluidic channels interconnect the nanofluidic channels in the chip to the macroworld. The microelectrodes in the nanofluidic device can be accessed via inkjet printed electrical interconnections.

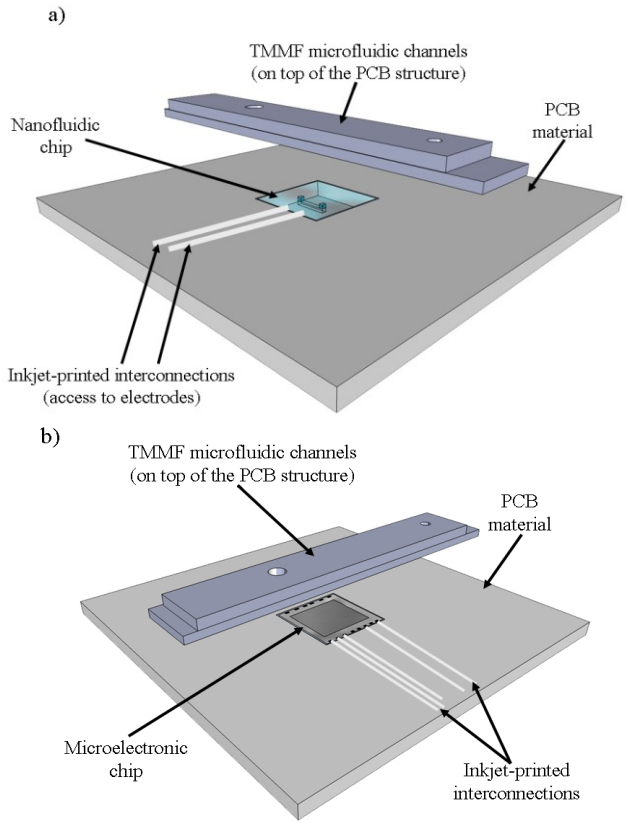

Figure 1. Schematic of different applications of the proposed technology, (a) integration of a nanofluidic chip, (b) integration of a microelectronic chip.

Figure 1b illustrates the concept when integrating a microelectronic chip using the proposed technology, for example an image sensor. In this case the dry film resist enables the construction of a microfluidic channel on top of the microchip and the inkjet printed conductive ink enables the possibility of accessing the functionality of the image sensor by the creation of electrical interconnection lines between the connection pads on the microchip and the pads on the PCB.

The challenges associated with the three aspects (NCA, DFR, inkjet printed ink) mentioned in this section are treated within the scope of this work. Quantitative as well as qualitative results are presented to evaluate the feasibility and robustness of the proposed integration method.

III. MATERIALS

TMMF dry film resist poses a unique stability when in contact with alkaline solutions and acids [3] [4] and provides high resolution and high aspect ratios [2] [4] making it the resist of choice for the fabrication of microfluidic channels.

The DFR used to fabricate the microfluidic channels is TMMF S2030, a permanent photoresist with a thickness of 30 µm for MEMS (microelectromechanical systems), manufactured by Tokyo Ohka Kogyo Co., Ltd. This negative photoresist is composed 5 % of antimony compound and 95 % of epoxy resin [2] [3].

Furthermore, the PCB material used as mechanical support for the whole system is Rogers RO4003C, a glass reinforced hydrocarbon laminate with low roughness characteristics.

Table I shows the physical characteristics of TMMF S2030 and Rogers RO4003C.

TABLE I. PHYSICAL PROPERTIES OF TMMF S2030 AND ROGERS RO4003C [2] [12]

Physical Properties of TMMF S2030 and Rogers RO4003C		
Physical Property	*TMMF S2030*	*Rogers RO4003C*
Coefficient of thermal expansion (ppm/°C)	65	X 11 Y 14 Z 46
Transition glass temperature (°C)	230	>280
Moisture absorption (%)	1.8	0.06
Dielectric constant	3.8	3.38±0.005
Transparency (nm)	400-600	-
Breaking strength (MPa)	60.3	-
Young modulus (MPa)	2100	26.889

The NCA used to glue the chips to the PCB material is a colorless two-parts epoxy-based adhesive with a glass transition temperature (Tg) of 45 °C and a coefficient of thermal expansion (CTE) of 56 ppm/°C when below the glass transition temperature, and 211 ppm/°C when above the glass transition temperature.

The ink used for the inkjet printed electric interconnections is a heat-curable silver nano-particle ink with a metal content of 20 % and a curing temperature of

125 °C. The thickness of one printed layer with such inks is in the range of 1-4 µm.

The names and brands of the NCA and the silver ink have been consciously left out.

IV. FABRICATION PROCESS

The fabrication process is divided in three steps:

- Inlaying of the chip in the PCB by using a NCA. The chip and the PCB together with the NCA form the substrate for the following steps.
- Fabrication of the microfluidic channels on the substrate.
- Fabrication of the inkjet printed interconnections between the chip and the PCB connection pads.

A. *Inlaying of the Chip(s) in the PCB*

The very first step to proceed to the fabrication of the TMMF microfluidic channels on top of PCB material is to form the substrate composed by the PCB and the chip(s). Figure 2 illustrates this process.

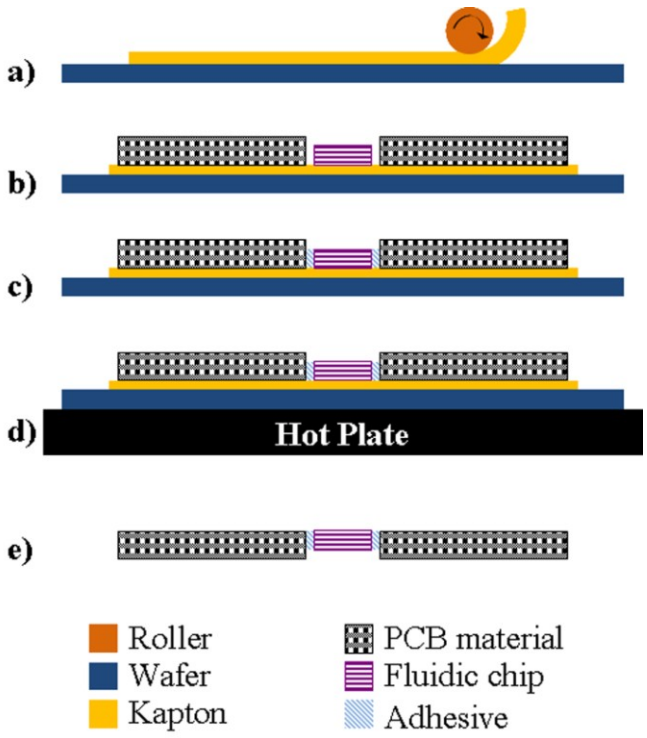

Figure 2. PCB material and nanofluidic chip leveling process flow chart.

According to Figure 2, to align the PCB material and the chip, a double sided Kapton tape is rolled on a Silicon or glass wafer or any other extremely flat and rigid surface (a). The PCB and the chip are adhered on the Kapton tape (b). The specimens are placed under vacuum to improve the adhesion between the Kapton tape and the components to be aligned. An Oxygen (O_2) plasma treatment at 50 W during 10 sec is performed using the Europlasma NV equipment. The epoxy-based adhesive is dispensed in the space between the PCB material and the chip (c). The materials are placed in a vacuum chamber to remove trapped air in the glue. The materials are placed in an oven or on a hot plate at 80 °C for 3 hours to cure the adhesive (d). When the adhesive is totally cured, the materials are cooled down to room temperature. The new substrate consisting of the chip inlaid in the PCB material is removed from the Kapton tape and turned 180 degrees (e).

To prepare the NCA, both parts from the adhesive are placed in a container and mixed with a Cat RM5 roller. The mix is placed in a vacuum chamber to remove possible trapped air.

B. *Fabrication of TMMF Microfluidic Channels*

The second stage of the fabrication process consists of laminating the TMMF microfluidic channels on top of the formed substrate. Figure 3 shows the flowchart for this process.

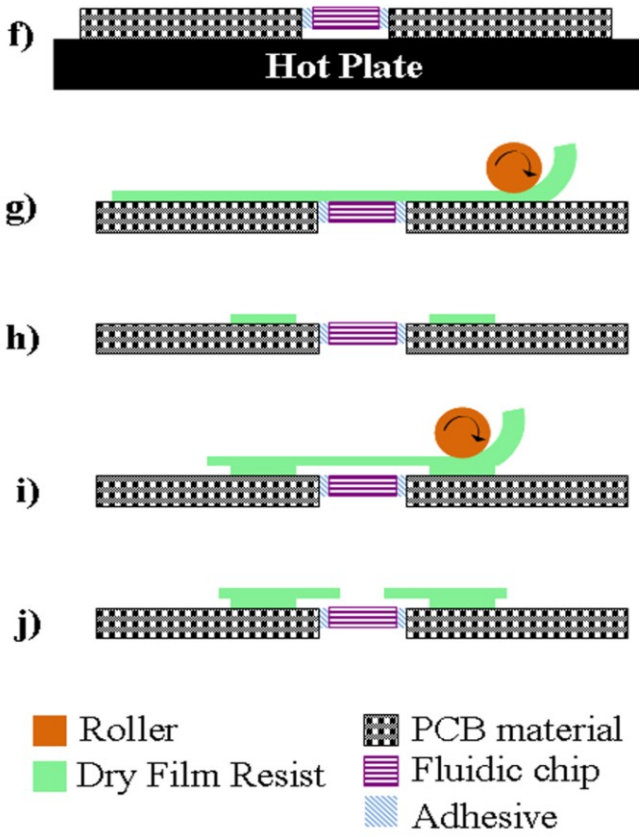

Figure 3. TMMF microfluidic channel lamination on top of the formed substrate.

The formed substrate is cleaned with ethanol and dried on a hotplate for 2 hours at 120 °C (f) to remove any adsorbed moisture; this will avoid that the humidity absorbed by the PCB material affects the DFR lamination process. An Oxygen plasma treatment is performed to the substrate in order to improve the adhesion between the TMMF resist and the formed substrate. The TMMF is protected on both sides with polyethylene terephthalate (PET).

The substrate is kept at 45 °C. One of the PET protective layers is removed from the DFR and the TMMF resist is

laminated on the substrate (g). The other PET layer is removed after the sample has cooled down. A soft baking step is performed at 90 °C during 5 minutes. The exposure is performed once the sample reaches room temperature. A post exposure baking step is performed with the same temperature and time than the soft baking step. The TMMF is developed using PGMEA (propylene glycol monomethyl ether acetate) after the sample has cooled down to room temperature (i).

Before closing the channels, the inkjet printed interconnections are printed.

A second layer of TMMF is laminated at 45 °C to close the microfluidic channels. The second layer is flood exposed after lamination without removing the remaining PET layer. The sample is cured at room temperature during one day. The PET layer is removed and access holes to the channel are punched with the help of a needle (j).

An alternative to create more stable and robust access holes instead of punching them in the TMMF is to use a through via in the PCB; in this case the access holes are accessed from the back side.

The alignment of the channels and the chip is performed manually, with the required equipment, and thus the accuracy is less than that of automated units.

C. *Fabrication of the Inkjet Printed Interconnections*

Finally, the inkjet printed interconnection lines are created.

The lines are printed with the drop-on-demand inkjet printer Jetlab 4 from Microfab Technologies, Inc., USA. The nozzle used is a piezo-actuated nozzle of 80 µm of diameter.

The substrate holder is heated at 65 °C during the printing process to avoid spreading of the ink.

The printed ink is cured in an oven during 16 hours at 125 °C.

With the 80 µm diameter nozzle, the smallest width line possible is 90 µm and the smallest space between lines possible is 70 µm.

V. CHALLENGES ASSOCIATED WITH THE FABRICATION PROCESS

Since the fabrication process is divided in three crucial tasks, the challenges associated with the fabrication process are grouped in three sections directly associated with each of the three crucial tasks.

A. *Challenges Associated with the Inlaying of the Chip(s) in the PCB*

The NCA used to keep together the chip(s) and the PCB material is an epoxy-based material.

Epoxy-based adhesives are known to present shrinkage due to the evaporation of the curing agent during the curing process [13] [14]. It is important to understand the behavior of this phenomenon given the fact that for a successful inkjet printing process, a flat surface is desired.

According to [15] a profile like the one in Figure 4 is expected after the NCA curing process.

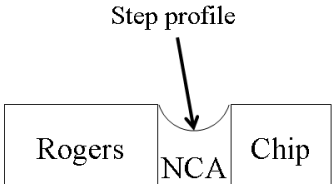

Figure 4. Profile expected in the NCA due to the curing process.

The effects of the glue shrinkage are studied into detail in Section VI Experiments.

B. *Challenges Associated with the Fabrication of TMMF Microfluidic Channels*

The challenges associated with the fabrication of TMMF microfluidic channels on the substrate are associated with the lamination of TMMF on PCB material and with the lamination of TMMF on the chip(s).

a) Lamination of TMMF on Rogers material: The challenges associated with the processing of TMMF resist on Rogers materials are pinholes in the photoresist, trapped bubbles between the resist and the PCB material, cracks in the photoresist, and closed channels.

Pinholes: TMMF might present pinholes after the soft baking step.

Experiments were conducted, and up to some extent, the pinholes can be decreased by using a plasma treatment, nevertheless, the crucial factor determining their presence is the moisture absorbed by the PCB material.

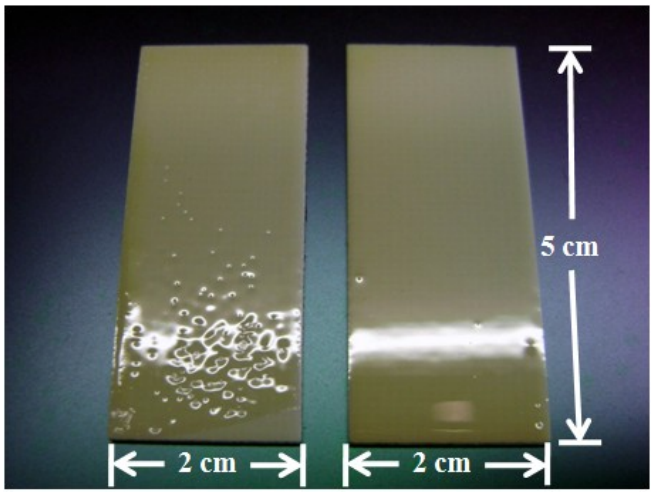

Figure 5. PCB material immersed under water prior to TMMF lamination (left) and PCB material dried at 120 °C prior to TMMF lamination (right). The presence of pinholes on the TMMF resist after soft baking is influenced by the moisture absorbed by the PCB.

Figure 5 shows two PCBs where TMMF was laminated and soft baked. In the specimen on the left side, the PCB material was immersed in water during 2 hours and its surface was dried with nitrogen prior to TMMF lamination. In the specimen on the right, the PCB material was placed on

a hotplate during 2 hours at 120 °C in order to evaporate the absorbed moisture prior to TMMF lamination.

Trapped bubbles and cracks: Experiments show that if the baking times are either higher or lower than the optimal time by at least one minute and the PCB material contains moisture absorbed from the atmosphere, trapped bubbles and cracks will form in the photoresist structures. The formation of trapped bubbles is directly related to the moisture absorbed by the PCB material and the use of inadequate baking times. The formation of cracks is related to the thermal stresses that result from a forced cooling down of the specimens after the baking steps and improper baking times. Furthermore, the moisture absorbed by the PCB material promotes the formation of cracks.

Figure 6 shows trapped bubbles between the TMMF and the PCB material as well as cracks in the dry film resist structures. The PCB material used for this experiment was not dried prior to TMMF lamination. Moreover, the baking times used in the processing were not optimal.

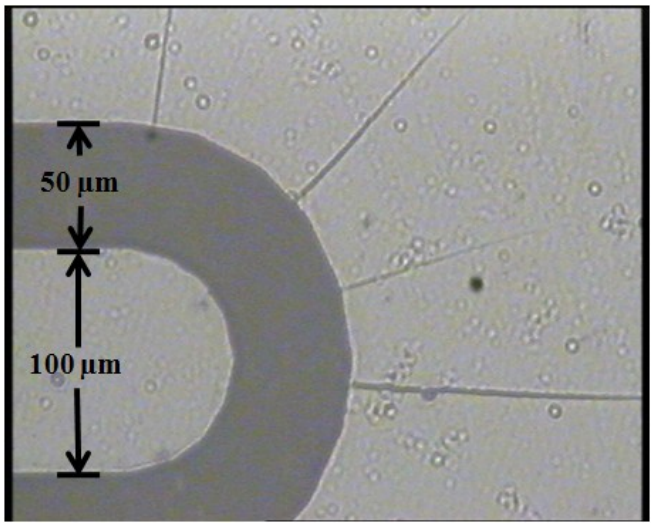

Figure 6. Trapped bubbles and cracks due to the humidity absorbed by the PCB material and the improper baking times used for processing of the TMMF.

Figure 7 shows a crack in the photoresist structure, but no trapped bubbles. The PCB material used for this experiment was dried prior to TMMF lamination, nevertheless, the baking times were not optimal.

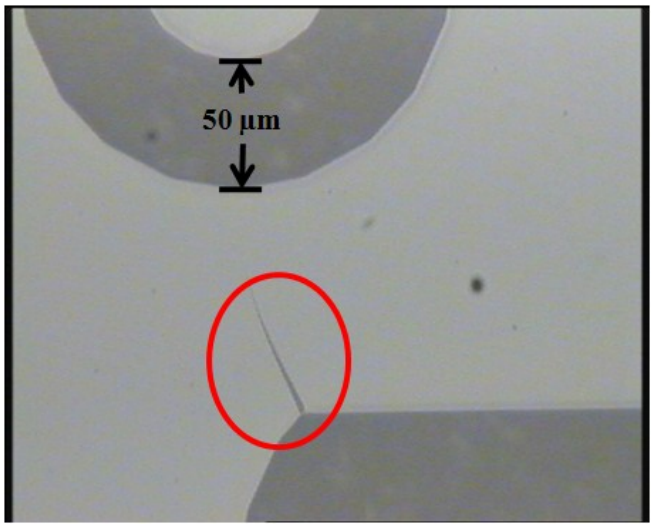

Figure 7. Cracks in the TMMF structures with angles close to 90 °. The circle in the image points the crack.The cracks are caused by the use of non-optimal baking times.

Closed channels: The exposure time should be controlled accurately when working with Rogers' materials. Scattering and diffraction of ultraviolet (UV) light during exposure is unavoidable when using a non-transparent material. Furthermore, the white color of the Rogers PCB material makes reflection of the waves a bigger problem.

The effects of an underexposed resist, as Figure 8 shows, are well known. On the other hand, overexposure can result in partially or totally closed fluidic channels.

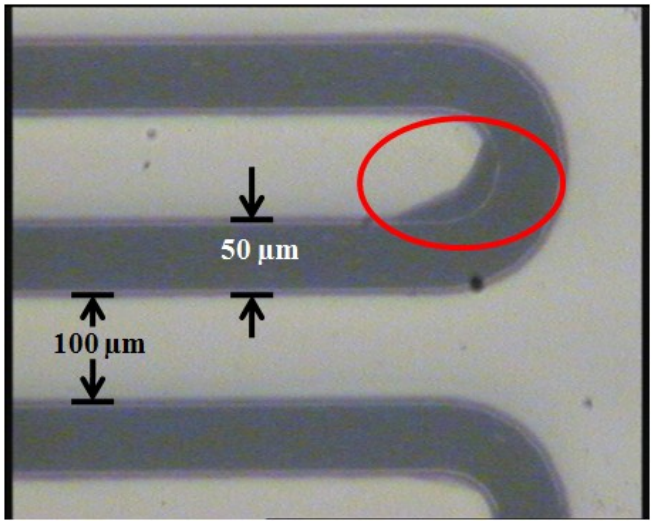

Figure 8. Effects of insufficient exposure time. The circle points an effect on the TMMF structure.

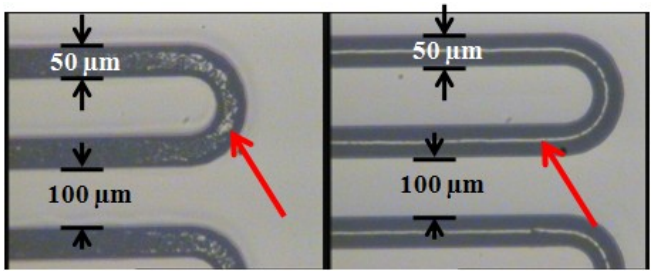

Figure 9. Closed channels on PCB material due to overexposure of the TMMF resist. The arrow in the left image points the effects of an overexposure of 2 seconds. The arrow in the right image points the effects of an overexposure of 6 seconds.

The more a sample is overexposed, the more closed the channels will be. Figure 9 shows a sample overexposed by 2 seconds (left) and a sample overexposed by 6 seconds (right).

b) Lamination of TMMF on the chip(s): Micro- and nanofluidic chips are usually made of glass and/or Silicon (Si), microelectronic chips are usually made of Silicon. PCB material and Si poses different thermal characteristics.

The thermal conductivity of the PCB material is approximately 0.71 W/m/°K [12] and the thermal conductivity of Si is around 140 W/m/°K [16]. Due to the thermal characteristics of the materials, heat transport at the baking steps is not a problem for the PCB material but it is for the Si chip(s).

The most common problem associated with the lamination of TMMF on Silicon is cracks due to heat transport at the baking steps and the difference in CTE [3]. Figure 10 illustrates this problem.

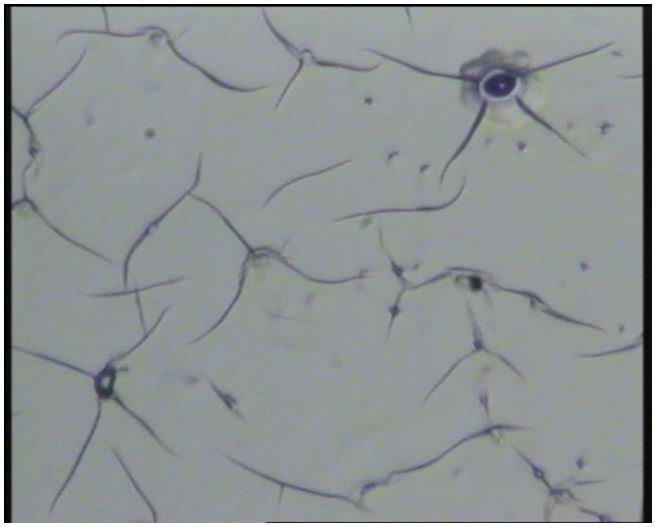

Figure 10. Cracks in the TMMF resist due to the CTEs difference between Silicon and the TMMF resist.

When the PCB material and the chip(s) are have the same thickness, as Figure 11a shows, the microfluidic chip will conduct heat around 25 times faster than the PCB material. Therefore, placing the substrate directly at 90 °C during the baking steps will originate cracks on the TMMF laminated over the chip. To solve this, the temperature needs to be ramped (2 °C/min) starting at 55 °C during the baking steps, when the temperature reaches 90 °C the samples are baked 5 minutes. Afterwards the hot plate's temperature is set to 25 °C, the sample is removed once the hot plate indicates 25 °C.

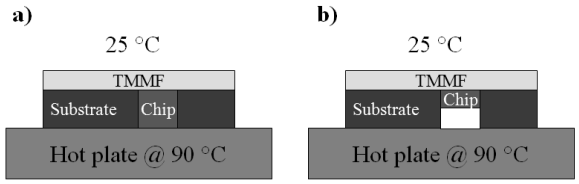

Figure 11. Cross-section of the substrate with TMMF on the hotplate when (a) the chip is the same thickness as the PCB material and (b) the chip is thinner than the PCB material..

Furthermore, if the chip is considerably thinner than the PCB material, as Figure 11b shows, the substrate can be placed directly at 90 °C. In this case, the thermal conductivity of the air between the chip and the hot plate will limit the heat flux to the chip, avoiding the presence of cracks on the TMMF.

This last method allows for less control thus the slow ramping of the temperatures is highly recommended.

C. Challenges Associated with the Fabrication of the Inkjet Printed Interconnections

The suitability of inkjet printed inks for their use in the proposed technology is studied. The main challenge and concern is the continuity of the interconnection lines, which can be affected by the step or curvature in the NCA due to its own shrinkage, especially if the step has a depth bigger than the thickness of the silver ink.

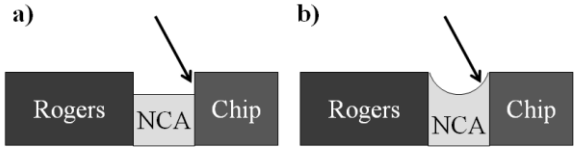

Figure 12. Possible step profiles, (a) steep step, (b) smooth step.

If the height difference between the chip and the NCA or the PCB and the NCA is steep as the arrow in Figure 12a indicates, it is expected that the continuity of the ink interconnection is interrupted. If the step is smooth as the arrow in Figure 12b points, the ink is expected to be continuous.

The adhesion of the ink is not expected to be a problem, since a plasma treatment is already performed prior to laminating the TMMF channels; however it is studied for confirmation.

VI. EXPERIMENTS

Each crucial aspect of the fabrication process is studied to test the feasibility of the proposed integration technology.

A. Inlaying of the Chip(s) in the PCB

In the case of the NCA shrinkage phenomenon, samples with different distance between the chip and the PCB material were prepared. The specimens were prepared following the procedure in Section IV.A.

The distance between the chip and the PCB is hardly controlled with precision. To control such gap, the chip(s) to be inlaid is measured and the desired distance between the chip and the PCB is added to the measurement; the hole in the PCB is created with these dimensions. The chip is placed carefully in the middle of the hole; this is the most difficult step since it is performed manually.

The step profile is measured with Dektak profiler and the angle of the step profile is obtained using Matlab code.

Figure 13 illustrates the measured step and the measured angle to avoid any misunderstanding. The step is measured from the deepest point in the NCA profile to the level of the PCB and/or chip. The angle of the NCA step with respect to a horizontal line is measured to determine the steepness of the step.

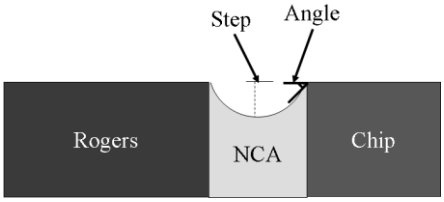

Figure 13. Sketch of where to locate the angle and step measured in each specimen.

Furthermore, few specimens cured at room temperature are prepared to determine the effects of the heat during the curing process in the substrate. Keep in mind that the materials in the substrate have very different CTEs thus the curing process temperature could affect the alignment of the chip and the PCB.

Since simulations of the curing process of an epoxy resin are complex and topic for a complete paper, it is not treated in this work and so the effect of the shrinkage in the substrate surface profile is determined in an experimental manner.

B. Fabrication of TMMF Microfluidic Channels

The TMMF microfluidic channels on the substrate are tested for leakage and exposed to sudden temperature changes.

The leakage test consists of injecting a rodhamine + ethanol + di water solution in the TMMF channels in one of the inlets. A visual inspection follows to detect any leakage. Special attention is given to the interconnection area between the different materials. Figure 14 shows the mentioned interconnection area before closing the TMMF channels.

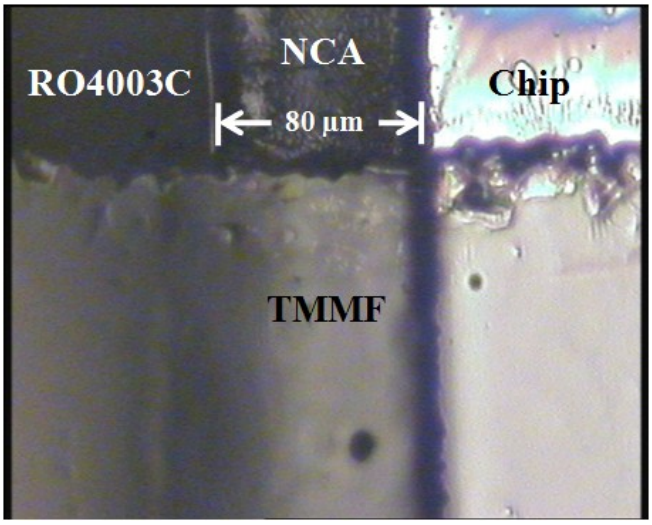

Figure 14. Close up of the interface between the different materials that form the fluidic interconnections to the nanofluidic chips.

The reliability test consists of a thermal shock test based on the military standard 883C. The purpose of this test is to accelerate the appearance of delamination and cracks.

The test consists of 15 cycles where each cycle is composed by a high temperature step at 100 °C and a low temperature step at 0 °C. The liquid used is water. After completing the test, a visual inspection is performed at a magnification no greater than 3x [17]. For further details about the test please refer to [17] and [18].

C. Fabrication of the Inkjet Printed Interconnections

The performance of the ink under sudden changes of temperature is studied to test the reliability of the inkjet printed interconnections. To do so, the resistivity of the ink is measured according to the Greek-cross method described in [18]. The resistivity is measured before and after the thermal shock test described in the previous subsection, with the exception that 20 cycles are performed during the test. The number of cycles has not considerably impact on the results; according to the standard, the cycles are increased during the test to compensate when there is less control on the temperatures and it is difficult to guarantee the variation limits specified by Option A [17]. Moreover, the adhesion of the ink is also studied before and after the reliability test using the Scotch-tape procedure described in [18]. The specimens used to perform the tests described in this paragraph are inkjet printed on Rogers.

The thickness of the ink is measured with a Dektak profiler. The thickness is necessary to calculate the resistivity values. The thickness measured is around 1 µm thus the ink thickness used for the calculations is 1 µm.

A resistivity change of maximal 20 % in the aged samples with respect to the fresh sample is considered a pass [19].

Furthermore, tests are performed printing on the whole substrate, that is to say, on the chip, NCA and the Rogers material, to test the continuity of the interconnection in the interface between the chip, the NCA and the PCB material.

Visual examination under a microscope is performed and the conductivity of the lines is tested with a multimeter.

VII. RESULTS AND SOLUTIONS

In this section the results are presented in three subsections.

First the results concerning the step originated by the shrinkage of the NCA.

Second, the results concerning the lamination of TMMF on PCB material and the chip(s) are presented. The leakage test results are exposed and the results concerning the compatibility of the TMMF and the different materials involved in the substrate.

Third, the results concerning the performance of the ink under sudden temperature changes and its continuity when printing on the materials' interface area are presented.

A. Inlaying of the Chip(s) in the PCB

Table II and Table III show the results of the step depth and angle measured for different spaces between the chip and the PCB material.

Section VI Experiments explains how the distance between the chip and the PCB material is controlled.

TABLE II. STEP DEPTH AND ANGLE

Distance between PCB and chip (µm)	Step depth (µm)	Angle side 1 (°)	Angle side 2 (°)
160	5.76	25.29	4.97
200	6.16	17.69	20.31
300	8.47	29.01	12.45

TABLE III. STEP DEPTH AND ANGLE

Distance between PCB and chip (µm)	Step depth (µm)	Angle side 1 (°)	Angle side 2 (°)
500	19.79	27.30	16.54
750	24.92	29.16	2.90
1000	32.00	3.40	30.13

The results in Table II are measured in a different specimen than those for Table III. According to Table II and Table III, the smaller the space between chip and PCB, the smaller the depth of the step is.

Furthermore, Figure 15 shows the profile of a specimen from Table II and Figure 16 shows the profile of a specimen from Table III.

According to the experiments, a NCA profile with the shape of Figure 16 can be obtained when the space between the chip and the PCB is at least 500 µm, if the space is less; a profile with peaks and irregular shape like in Figure 15 is obtained.

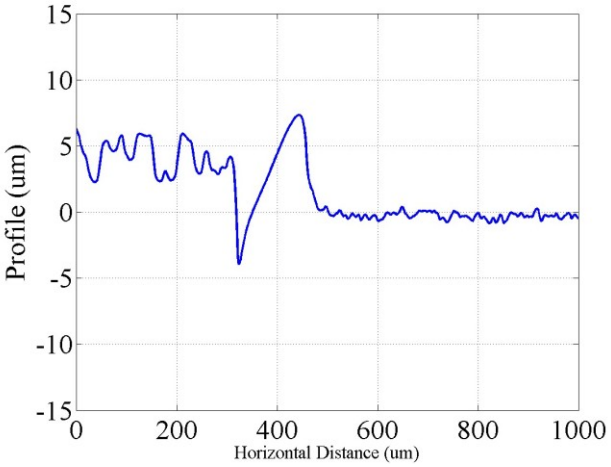

Figure 15. Profile of a specimen from Table II.

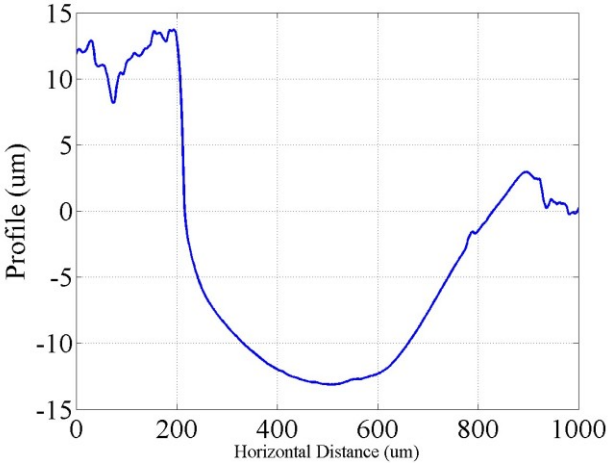

Figure 16. Profile of a specimen from Table III.

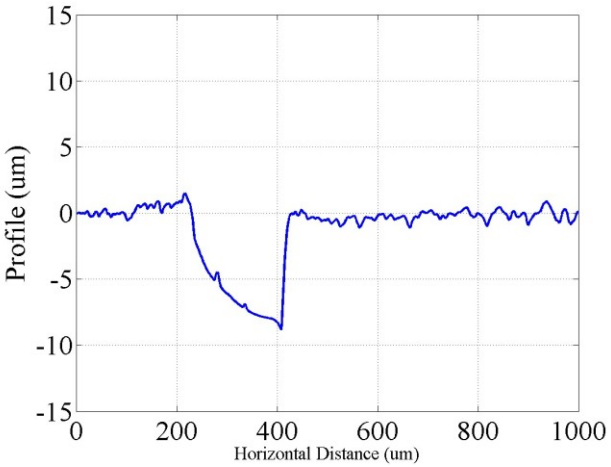

Figure 17. Profile of a specimen cured at room temperature.

Figure 17 shows the profile of a specimen cured at room temperature. During the experiments, it was observed that the specimens cured at room temperature present high

probabilities of keeping the PCB and the chip at the same level in the Z-axis, that is to say, horizontally aligned. Figure 16 shows the profile of a specimen that is cured at 80 °C; in this case the chip and the PCB are misaligned in the Z-axis by 10 µm, which is a typical value at this curing temperature.

B. Fabrication of TMMF Microfluidic Channels

The results in this section are presented in three subsections. First, the results relevant to the TMMF resist channels on the substrate; second, the results of the leakage test and third, the results of the reliability test to detect delamination problems.

a) *TMMF resist channels on the substrate.* Some factors should be kept in mind to obtain good results fabricating microfluidic channels on PCB materials. The baking times provided by the companies are optimal, nevertheless, different materials conduct the heat in a different rate, and therefore, the material temperatures might deviate from the prescribed temperature, especially when using a hot plate. Furthermore, PCB materials are more reflective than Silicon or glass; because of this, the exposure time should be tuned accurately; if channels of less than 50 µm are desired, this parameter is critical.

Figure 18 shows a TMMF structure on PCB material fabricated with optimal exposure and baking times.

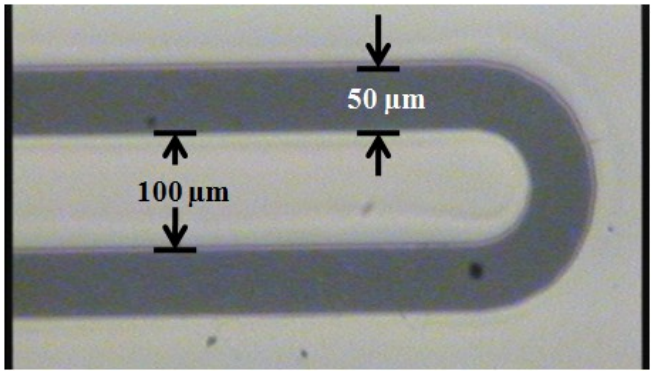

Figure 18. Microfluidic channels on PCB material. The image shows the results of optimal processing parameters (exposure and baking times).

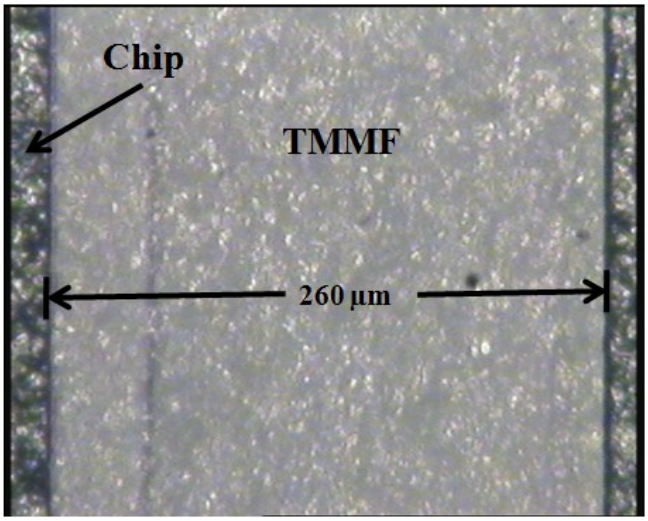

Figure 19. TMMF microfluidic channel walls on the Si chip, fabricated avoiding sudden temperature changes in the process.

Figure 19 shows the TMMF microfluidic channel walls on the Silicon chip fabricated in a way that sudden temperature changes are avoided; the temperature is slowly ramped during the baking steps. It is possible to observe that there are no cracks present in the TMMF structure.

b) Leakage test. Concerning the leakage test, Figure 20 shows a device fabricated with the packaging technology presented in this work.

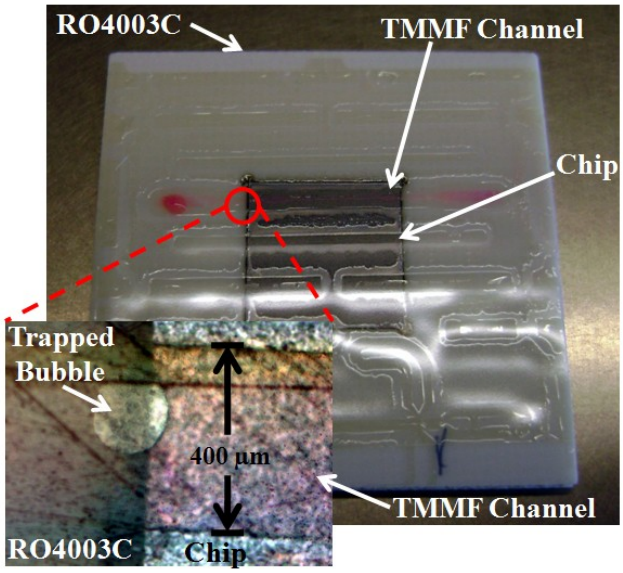

Figure 20. TMMF microfludic channels on PCB material as fluidic interconnections for nanofluidic chips. The small image in the lower left corner zooms in at the interface of the different materials that form the device; it shows no leakage of the rodhamine solution.

The pink liquid flowing through the TMMF channel is a solution of rodhamine + ethanol + di water. It is observed that no leakage occurs. The small image at the lower corner in the left was obtained with a 1X71 Olympus inverted microscope equipped with a low noise self cooling CCD

camera (color view II, Olympus); it shows, with 10x magnification, the area where the different materials interconnect. It is possible to observe the liquid solution flowing through the TMMF channel without leakage.

c) Reliability test. Figure 21 shows a device without closed channels after the thermal shock test.

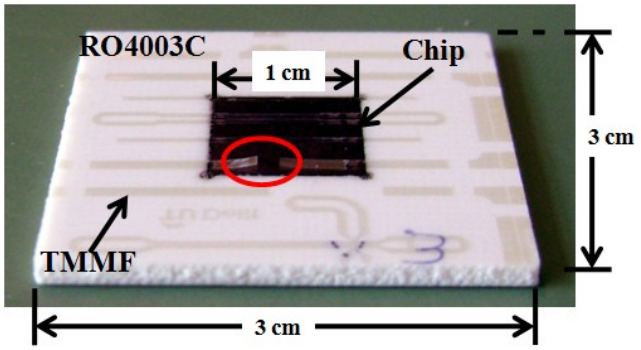

Figure 21. TMMF delamination on top of the Si chip after the thermal shock test. The circle points at the place where the delamination occurs.

The circle makes emphasis on a failure result from the test. Delamination of TMMF occurs on top of the fluidic chip. From the 3 tested specimens, the failure was observed only in the specimen from Figure 21.

C. Fabrication of the Inkjet Printed Interconnections

Table IV shows the measured resistivity values in μΩ·cm before and after the ageing test.

TABLE IV. RESISTIVITY OF THE INKJET PRINTED STRUCTURES BEFORE AND AFTER THE THERMAL SHOCK RELIABILITY TEST

Specimen number	Fresh specimen resistivity (μΩ·cm)	Aged specimen resistivity (μΩ·cm)	Increase (%)
1	38.75	38.43	-0.82
2	42.51	40.56	-4.58
3	26.79	26.47	-1.18

Even though the resistivity values can be considered high with respect to the values obtained in [18] and to the resistivity of bulk silver (1.59 μΩ·cm), the performance of the ink under sudden changes of temperature is good, in all the cases the resistivity decreased by a percentage of less than 5 %.

The adhesion characteristics before and after the ageing test are also good.

Scotch tape is used to test qualitatively the adhesion. The tape is rolled with pressure over the printed ink test structure, and then peeled off. The ink traces lifted with the tape when peeling it off are considered failures. There are no ink traces on the tape after peeling it off, which means that the ink was not peeled off from the Rogers material during the test.

The silver ink presented thus no adhesion failures before and after the reliability test.

Furthermore, Figure 22 shows the silver ink interconnection line printed on top of the components that form the substrate.

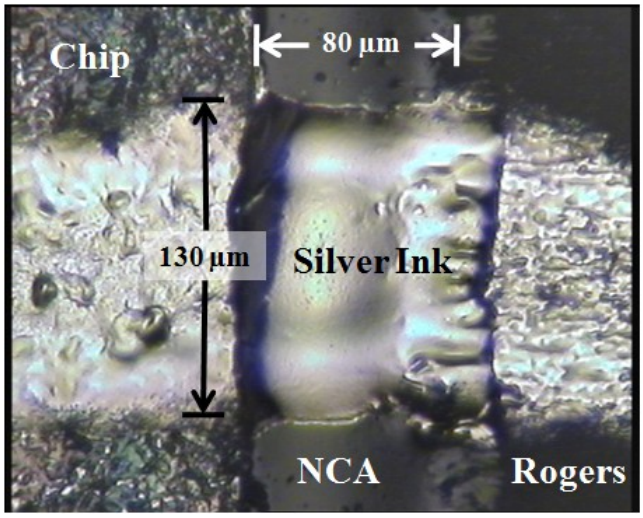

Figure 22. Interconnection silver ink line printed on the chip, the NCA and the Rogers material.

The printed silver ink line follows the profile of the surface with step depths measured in the range of 3-20 μm presenting electrical conductivity between both extremes of the line.

VIII. CONCLUSION AND FURTHER WORK

The experiments show that the step caused by the NCA cannot be completely eliminated.

To reduce the depth of the step it is recommended to have the minimum space possible between the chip and the PCB material.

Moreover, curing the NCA at room temperature is recommended in order to reduce the misalignment between the PCB and the chip in the Z-axis.

The thermal shock reliability test showed that the use of high temperature conditions could cause delamination problems mainly at the interface TMMF-NCA-Si chip. This means that the strength of the TMMF microfluidic interconnections decreases thus the probability of leakage increases.

Moreover, the experiments confirm the feasibility of the use of inkjet printed interconnection lines to create the electrical interconnection between the connection pads on the chip(s) and the connection pads on the PCB.

The silver ink shows perfect adhesion properties under room temperature conditions as well as under sudden temperature changes.

The electrical performance of the ink is not considerably affected by the rapid changes in temperatures.

Finally, the inkjet printing process and the characteristics of the NCA step allow the ink interconnection line to follow perfectly the substrate's profile, thus keeping the continuity in its conductivity and structure at all moments.

Further work includes the use of an image sensor available in the market to prove the feasibility of the proposed technology in a real life application. The PCB in turn can carry the necessary electronics for control and read-out. This enables the PCB as the core for the integration of micro- and nanochips together with electronics into a complex system.

Moreover, this work can be extended as assembly solutions for wider application areas as MEMS sensors and actuators.

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