Electro-Magnetic Modeling and Design of Through Silicon Vias Based Passive Interposers for High Performance Applications up to the V-Band

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***Abstract*— The present paper reports the design and Electro-Magnetic (EM) modeling of Through Silicon Via (TSV) based band-pass filters embedded in passive interposers for C and V-band applications. For each filter, EM simulations have been performed with the help of a FEM (Finite Element Method) 3D EM solver. Prior to filter implementation, a comparison between simulated and measured data is proposed on dedicated structures (3D solenoids, and transmission lines) to calibrate the simulator and validate the simulation methodology. The obtained simulation results are successfully correlated to measurement data up to 110 GHz. In addition, an original package characterization up to 30 GHz is also proposed to support filter design and implementation. The proposed filter architectures permit a clear reduction of the filter footprint (up to 90 % vs. conventional implementation on ceramic substrate) with good electrical performances. Depending on the application IL of 2,6 and 2,0 dB have been simulated respectively at 4 and 42 GHz. Discussion on advantages of using either high/low aspect ratio TSV together with different Back-End Of Line (BEOL) option is proposed based on these two typical examples. Perspectives are then given in terms of 3D-IC integration.**

Keywords - Finite Element Method; Through Silicon Via; Filtering; EM simulations; passive interposer; Millimeter-wave

I. INTRODUCTION

The concept of 3D Silicon integration using TSV stacking is one of the most promising technologies. It can extend Moore's law by stacking and shortening the connection path between memory and logic [2]. Due to the increase in functional integration requirements, more and more assembly house and wafer foundries are looking into 3D TSV technology, which allows stacking of Large Scale Circuits (LSI's) thereby enabling products to be made smaller with more functionality. 3D technology realizes miniaturization up to 300-400% compared to the conventional packaging [3]. Furthermore TSV are also relevant to develop "more than Moore" applications [4], where passive functions originally lying on the PCB (Printed Circuit Board) can be designed with the help of TSV up to the C-band using original component architectures such as embedded solenoids (see Figure 1). In that sense, distributed L, C filters based on TSV can be optimized and implemented within interconnect dies.

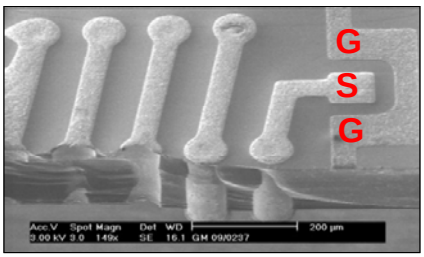
On the other hand, solenoids have limited performances at higher frequencies (in the millimeter-Wave domain). Indeed these solenoids made with low aspect ratio vias (300/75) exhibit non negligible parasitic capacitance with substrate that degrades their Self-Resonant Frequency (SRF) and thus their efficiency at higher frequencies [1]. Furthermore, passive interposer die with high aspect ratio vias cannot allow designing such solenoid but worth being considered to make filtering at higher frequencies (Ka and V bands) using a different architecture. Indeed, both Ka and V-bands – currently reserved for professional applications (aerospace, defense, satellite communications) - appear promising for developing applications such as automotive car-radar and wireless infrastructures [5][6] in order to face societal challenges: Energy harvesting, health, mobility and safety, security).

The paper will be organized as follow: a perceived state of art regarding passive component implementation is proposed in the following section of this document. Then, integrated solenoid as well as MOM capacitance will be introduced in the second section; their performances will be presented from an electrical point of view together with their relative precision taking into account the process spread. Solenoid performances obtained from wide-band frequency 2-ports S-parameter measurements will be presented. EM modeling done with the help of a 3D Finite Element Method (FEM) solver will be also described and compared to measurements. As the effect of packaging plays a significant role on the device performances, the third section of this study will be devoted to the characterization of a conventional QFN package using a very single test-case. Measurement data will be then used to calibrate the EM simulator. In the fourth section of this paper, we report the design methodology and the simulation results for a 4 GHz band-pass Chebyshev filter done using TSV. In the

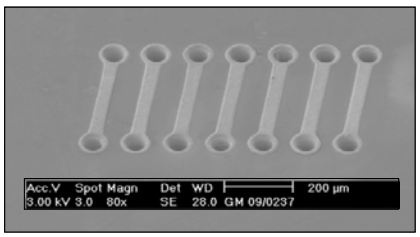
fifth section, we will introduce the micro-strip TSV based band-pass filter for Ka/V band applications. Its architecture will be presented together with characterization results obtained on transmission lines. These measured data will be used to calibrate the FEM solver and then propose an EM model of the proposed filters. The interest of using both high aspect and low aspect ratio of TSV in view of targeted applications is also documented in the paper. Simulation results based on different scenarios for BEOL and substrate options will be presented at the end of the document as well.

II. PERCEIVED STATE OF ART

Many efforts have been done to develop high performances active and passive devices especially in BiCMOS process [7][8][9] to support high performance applications. However, this is not enough; these high frequency applications will also require elite passive devices. Modification of BEOL and/or substrate properties (going to HRS for example) is already a good alternative but requires process update that is sometimes very expensive and can impact front-end components. In addition, the emergence of 3D interconnects such as TSV allows designing passive interposers to support these high performance applications. They render possible for example integrating passive filters necessary in every module.



(a)



(b)

Figure 1. SEM picturesTop view (a) and bottom view (b) of the 3D solenoids within GSG (Ground Signal Ground) pads – source IPDiA

Filters are either integrated on chip (using planar coils and Metal-Oxide-Metal (MOM) capacitors) or integrated in a hybrid application such as MCM (Multi-Chip Module) lying on a ceramic or organic substrate using a micro-strip architecture. Some well known structures have been already successfully implemented and extensively reported [10][11][12][13][14]. For the former ones, they can suffer from their low quality factors (mainly due to the resistive losses within the planar coils) while the latter ones exhibit high performances but can deviate a lot from nominal behavior compared to silicon because of process spread.

Another alternative also consists in implementing the filters on top of the carrier substrate (Printed Circuit Board for example) with the help of Surface Mounted Devices (SMD). The main advantage of such approach is the high quality factor value that can be reached. But generally they have limited performances at higher frequencies, the total footprint is bigger and the lack of accurate and scalable electrical models limits their applications and implementations in view of a high selectivity of the signals. In case of fully integrated filters within silicon IC processes, some passive integration dedicated processes have been already developed to tackle the low quality factor of the unit components. Devices are generally deposited on HRS (High Resistive Substrate) that clearly limits the effects of eddy currents [4] [15]. Thick top metals are also implemented and copper is often used to reduce the resistive losses. Thickness up to 8 µm can be considered in certain cases. Recent achievements have highlighted really good performances for band-pass filter for TV on Mobile applications [16]. For this application, coils exhibit regular planar shape, which provides a good compromise for designers between ease of layout, manufacturing and electrical performances. Besides that, Ka-band filters with really good performances have been also recently achieved using micro machined process either within silicon or glass substrate [17]. These technologies are really good candidates to develop applications in the millimeter-Wave domain. Notwithstanding, they require at least a substrate transfer technology (case of glass) that is not often compliant with classic wafers handler for which foundry need to adapt deeply their production environment [18]. On the other side, together with the emergence of new type of interconnects such as TSV, embedded solenoid implementation within silicon or glass substrate [19] is now considered to easily build a coil-type of structure. Several proposals have been done in that sense leading to very promising results [20][21]. In fact, integrated solenoids can be used to produce larger quality factor than in RF BiCMOS/CMOS planar technologies within a given footprint [22]. This increase in quality factor can be attributed to both metal thickness and the specific solenoid property of storing energy according to:

$$Q = \omega \cdot \frac{energy\ stored}{average\ power\ dissipated} \quad (1)$$

Where ω designates the pulsation (i.e.,2.π.freq)

Thus, the following part of this document will describe the solenoid architecture that we have adopted and summarize the main electrical performances measured on-wafer on this kind of devices.

III. 3D INTEGRATED SOLENOIDS

In this part, 3D integrated solenoid will be described in terms of geometry. Then, high frequency measurements will put in obviousness the real interest of such a device in the C-band.

A. Solenoid geometry description

We have already reported the fact that 3D TSV based solenoid can be implemented within a silicon die [22]. This process has been developed by IPDiA (formally NXP semiconductors). Contrary to the approach proposed in [23] where solenoid lies on top of the substrate, our 3D solenoid uses the thickness of the silicon as the third dimension. Indeed each turn of our solenoid is fabricated with the TSV as the vertical sides. A front side and back side metallization of the bulk wafer lead to connect the top and the bottom tracks, thanks to the TSV, allowing creating loops embedded within the silicon. Thereby we obtain a square section 3D solenoid architecture. On the top side of the silicon, a second level of metal is also used to realize MOM capacitors with a density of 100 pF/mm^2.

Copper is deposited onto front and back sides of a 300 µm depth high resistivity silicon substrate (HRS) according to a pattern defined in Figure 2. The vias are partially filled with the same metal on the external sides as highlighted by the SEM (Scanning Electron Microscopy) picture in Figure 1(b). Consequently N-turns 3D solenoids consist of N elementary spirals placed side by side and connected in the direction of the pitch between two consecutive vias (see Figure 2). Due to the TSV technology process, parameters such as via diameter and via height are fixed and so cannot be modified. In our case, the aspect ratio AR (height/diameter) is equal to 4. To avoid mechanical stress, the pitch between two consecutive vias is set to a minimum value equal to 125 µm. Nonetheless, the dimension of the metal tracks in front and back sides can be modified in order to improve the intrinsic component electrical characteristics as suggested by [24]. Hence the solenoid is defined according to its number of turns N, its width Dy and the metal track width W (that can be different between top and bottom traces). A change in the metal tracks width will also impact the spacing SP between two consecutive metal tracks.

B. Solenoid measurements

To support our theoretical investigations, solenoids with 1 to 6 turns were designed and grown on silicon. Then the designed test-case inductors have been placed within conventional GSG pads (Figures 3 and 4) and measured using a network analyzer PNA8364B from Agilent Technologies, with high frequency micro-probes. Full two ports S-parameter were performed for each device up to 20 GHz.

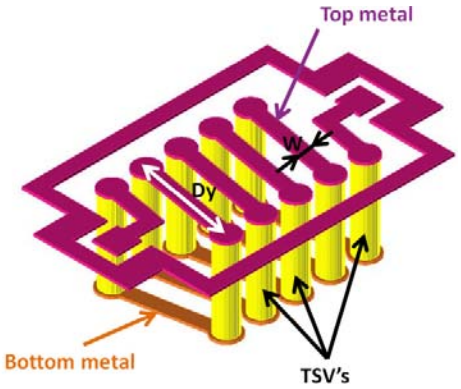


Figure 2. Synoptic representation of a 5 turns 3D solenoid within its RF test structure (bulk silicon is not represented on the picture)

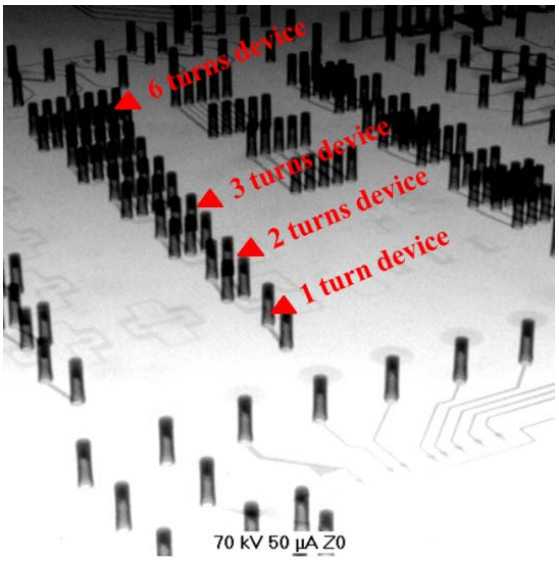


Figure 3. X-ray diffraction picture of the solenoid dedicated module (source IPDiA) – The bottom white face of the picture is the top side of the wafer

During the RF characterization, the wafer was stacked to a grounded chuck to ensure a global reference ground to the wafer, the network analyzer and the micro-probes. If no precautions are taken, a short circuit appears between the grounded chuck and the bottom metal tracks of the wafer. As a consequence, a sheet of glass fiber (~100 µm thick, ε_r =4.5) has been placed between them. The complete set of solenoids is shown on the previous X-ray diffraction picture. TSV can clearly be identified as a small vertical dark bar. For each measured device, self-inductance value and quality factor have been extracted on five crystals. In [22], we have already shown that the self-inductance variation versus the number of turns N was really close to a linear law, suggesting a very low inductive coupling between the loops. This is due to the minimum pitch defined by the process that is relatively large (= 125 µm). As a consequence, the capacitive coupling is also reduced, which allows using the inductors at several GHz. Furthermore, due to the typical

geometry of the solenoid, the quality factor is improved up to several GHz compared to classical planar IC coils either in CMOS or BiCMOS processes. A physical lumped elements electrical model was proposed also to simulate the device behavior versus frequency (see Section C.1). This model is indeed really helpful to generate contour plots in order to pick-up the right solenoid parameters (N, W, Dy, SP) and thus decrease the design iterations. Nonetheless, as any other compact model, it is not correlated to the global environment of the device (parasitic coupling, ground rails …). So in view of designing passive filters, we have also developed an EM (Electro-Magnetic) based model.

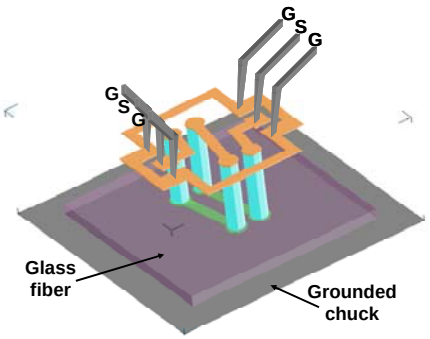


Figure 4. Illustration of the measurement test-bench used to guarantee a good ground reference together with an isolation between bottom metal traces and chuck (case of a 2-turns solenoid)

C. 3D solenoid modeling

Solenoid modeling is addressed first with a classical approach (i.e., compact modeling) and then with a 3D EM solver to provide modeling within a real environment.

1) Physical compact modeling

A first compact and physical model of the TSV based solenoid has been already issued. The schematic circuit of the model is presented in figure 5. This model has been built in order to figure-out the solenoid behavior within its RF test structure. Traditional model [25] –also called the "9 elements model" used for planar coils cannot be used in that case due to the 3D specificity of this kind of device with the parasitic 3D effects introduced by the vias. Our choice has been to follow the physical configuration of a 1-turn solenoid to deduce an RLC equivalent circuit model in the frequency range 100 MHz-10 GHz.

Knowing that each of both vias is modeled by two equivalent half-vias, the self-inductances of the top and bottom metal tracks as well as the vias are characterized respectively by L_{bot}, L_{top} and L_{via}. The metal tracks and the vias are sensitive to the skin effect. The skin depth in the copper, with a conductivity of 5.8 10^7 S/m, at 100 MHz and 1 GHz equals 6 µm and 2 µm respectively. Hence an RL ladder scheme [26] has been used to predict the increasing resistance against frequency for each of the metal tracks (R_{top} and R_{bot}) and the vias (R_{via}).

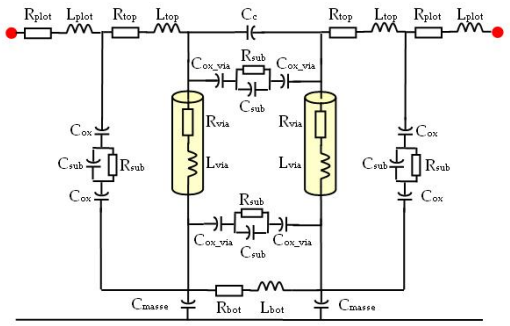


Figure 5. Schematic view of the equivalent circuit consider to derive the compact electrical model of 3D TSV based solenoid

Regarding the coupling between two adjacent vias, we can distinguish several contributions. The first one is the capacitance C_{ox_via} introduced by the oxide barrier (to avoid copper diffusion within the substrate) between the via and the substrate. The second one corresponds to the capacitance C_{sub} and the resistance R_{sub} of the substrate. As mentioned in the measurement results section, the backside of the wafer has been protected from the grounded chuck with a sheet of glass fiber. Notwithstanding, a capacitance C_{masse} exists between them and needs to be evaluated. The capacitance between the two consecutive top metal tracks (i.e. function of the spacing SP) is characterized by C_c. In the case of 1-turn 3D solenoid, C_{lines} is very weak due to the small area of the top metal tracks facing each other.

In order to address multi-turns solenoid modeling, each of the previously defined section is added for each loop of the solenoid. Coupling capacitances as well as coupling inductances are also implemented. Based on available test-structures, a good correlation has been obtained between both simulated and measured data [27].

The primary mean of this compact model is to correctly predict the main electrical characteristics of the device such as:

- its self-inductance value
- its quality factor (in link with resistive and substrate losses)
- its Self-Resonant Frequency (SRF)

Typically, designing an inductor can be very time consuming and needs most of time a real experience with this kind of device. In fact, the trade-off between series resistance and substrate losses represents a conventional scenario that RF designers need to address in an efficient and quick way when using on-chip inductors in their circuits. So, a design tool capable of optimizing the inductor layout by considering all these constraints (input parameters and overall performance) can significantly accelerate the design flow and have an impact on the time to market. Thus, a compact model that can predict the performances of a coil based on the parameters listed above – related to the input geometrical parameters (W, N, Dy), is really helpful and can be used to generate contour-plots in order to pick-up the right geometry and decrease the implementation time. The

following figures, propose some typical contour plots that can be generated with the proposed compact model:

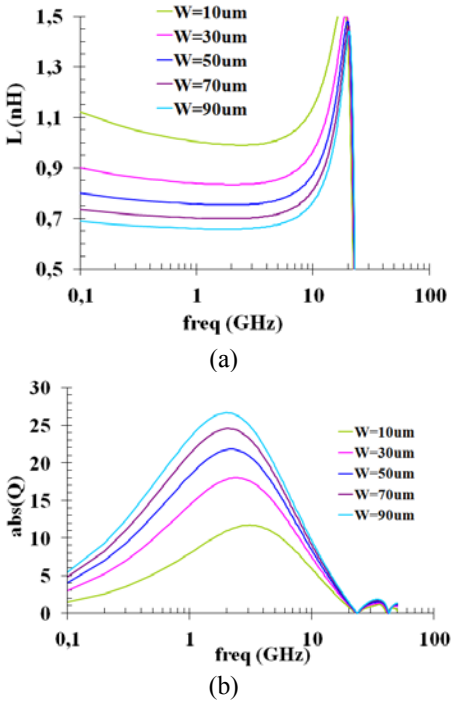


Figure 6. Simulated variations of (a) the self-inductance value and (b) quality factor vs. frequency for 1-turn solenoid (Dy was set to a fixed value during the simulations). These plots have been deduced from 2-ports S-parameter anlysis with a classical CAD simulator (i.e., SPICE). Compact model described in the previous paragraph has been used to extract the devices performances

Thanks to these plots, designers are able to find the compliant coil layout for achieving a specific inductance with the highest Q possible for a given technology of interest (only process parameters are required in the equations of the model). For example, considering a 700 pH inductor at 1 GHz, one can decide to have copper tracks that are 70 µm width with a 1-turn configuration. In that case, the expected quality-factor is equal to 22.

Nevertheless, this approach could not anticipate on the device behavior when placed in its environment. In micro wave a special care needs to be taken during the layout topology translation to tackle the unwanted current loops and identify both parasitic magnetic and electric couplings. Parasitic extractor provided by Electronic Design Automation (EDA) vendors are of particular relevance (when coupled with full-wave analysis) in that case especially for planar applications [28]. Unfortunately, they are not optimized to solve 3D problems like the one occurring in bulk silicon substrate.

2) Electro-Magnetic (EM) modeling

Dedicated test-cases presented in the previous paragraph have been simulated using the 3D FEM solver EMPro from Agilent. First, TSV have been defined within the substrate stack taking into account the partial fill of the vias with copper, the barrier between the copper and the silicon bulk (to avoid copper diffusion in the silicon). Geometry of the vias is also simplified: the circular shape of the TSV is converted to an octagonal one, in order to speed-up the mesh and thus the simulation time without losing any accuracy on the results. Bulk silicon has been described with the help of its relative dielectric permittivity (ε_r=11.9) and its resistivity - equal to 1000 Ω.cm. First a comparison between simulated and measured S-parameter has been performed (see Figure 7). Then, both self-inductance value and quality factor against frequency have been computed for comparison purpose (Figure 8). Self-inductance and quality factor values have been extracted according to the following relations:

$$L = \frac{imag\left(\frac{1}{Y_{11}}\right)}{2\pi \times freq} \quad (2)$$

$$Q = -\frac{imag(Y_{11})}{real(Y_{11})} \quad (3)$$

where ***freq*** is the working frequency and Y_{11} is the input admittance.

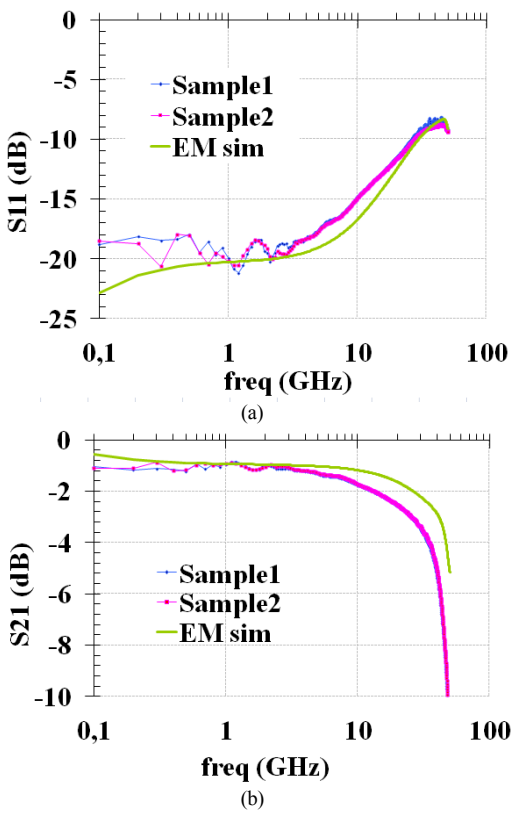


Figure 7. Comparison between Measured and simulated data on both (a) Reflection and (b) transmission S-parameter (1-turn solenoid)

From the available test-cases, a pretty good agreement is found for the self-inductance as well as the quality factor variations versus frequency.

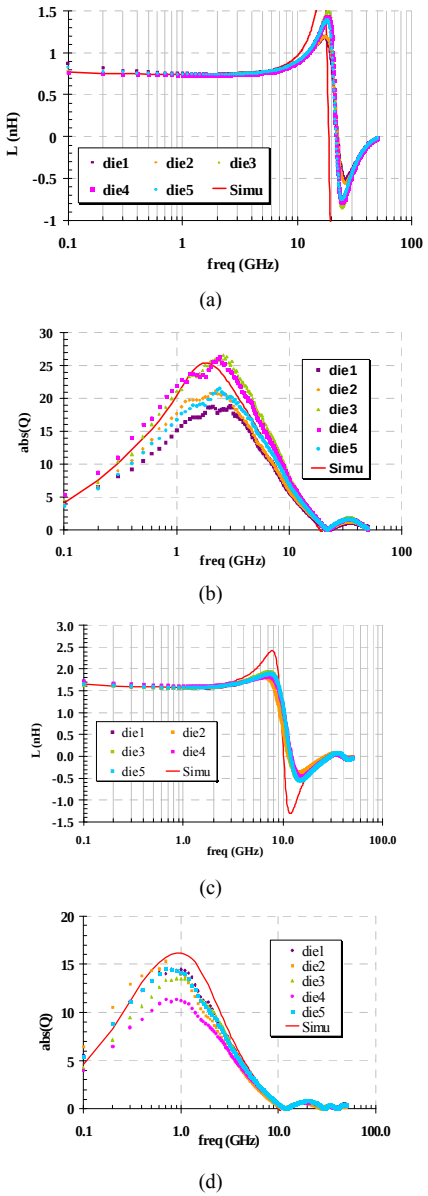


Figure 8. Comparison between measured and simulated data for 1-turn solenoid (a): self inductance value (b) quality factor and 2-turns solenoid (c): self-inductance value (d) quality factor

The SRF (Self-Resonant-Frequency) is also well predicted suggesting that the parallel capacitances are also well evaluated with the proposed approach. Typically, a difference of 3 % is observed on the self-inductance value and 10 % on the overall variations of the quality factor. This validates our approach that will be used to design a 3D solenoid based passive filter. Nonetheless, these measurements and simulations have been performed on-wafer without any coating on top of the substrate. In the following part of this paper, we propose to study a single test-case combining a chip, a package and a line on a board to validate our EM tool for packaging applications as well.

IV. PACKAGE MEASUREMENT AND MODELING

The following section will describe an original approach that has been considered to perform S-parameter measurements on a commercial package (QFN type).

A. Test-case description and measurement

Indeed, the emerging applications of wireless communications require effective low-cost approaches to microwave and RF packaging in order to meet the demand of the commercial marketplace. In that sense, surface mountable packages and especially plastic packages are a cost effective solution for low-cost assembly and packaging. However, plastic packages, whatever their types (standard QFN or flip chip based solutions such as BGA) contain unavoidable parasitic elements. As a consequence, development of characterization techniques for surface mounted packages is motivated by the need to predict the parasitic behavior of packages at microwave frequencies. In fact, the capability of accurately and easily characterizing packages provides a means to study and correctly model their high frequency behavior. Work in the literature relies mainly on EM simulations [29] [30]. In this paper, we will present an "on wafer" method of measuring the microwave performances of a chain containing a chip, a package and a 50 Ω line on Rogers substrate. Final goal of this part is to calibrate the EM simulator (in our case EMPro from Agilent) based on this single test-case.

B. Package modeling

One of the main problems of package characterization is that the terminals of the lead-frame are not accessible without significant modification to the investigated structure. To overcome the need for this modification, we have divided the test-case into three main parts. A photograph of the test case is provided on Figure 9.

So the first part of the test-case is a BiCMOS (NXP in house process) silicon die containing a coplanar line. The line is designed in such a way that it allows GSG probing with conventional micro-probes from Cascade Micro-Tech. This line is then connected with the help of 4 bond wires (2 for the signal and 2 for each ground path) to the pins of the package. Classical 20 µm diameter gold bond-wires have been considered for this study. Then, to be able to measure the electrical characteristics of the package, it is mounted onto a RO4003C substrate from Rogers Corporation (thickness = 406 µm, ε_r = 3.38, tan(δ) = 2.7e^{-3}). A specific coplanar access is also designed on the substrate allowing also GSG probing (bottom side of the photograph in Figure 9).

In order to perform 2-ports S-parameter measurements, the package is then opened to access the GSG pads on the chip. Prior to measurements, a Short-Open-Load-Thru (SOLT) calibration is performed. Four test-cases have been

measured up to 50 GHz to ensure a good reproducibility of the measurements. Results are presented in Figure 10.

The first results clearly show a good reproducibility between the measurements. Insertion and Return loss of the total chain are respectively equal to -1.3 and -10 dB at 4 GHz, which makes such a package suitable for multi-GHz applications. Of course, many improvements can be considered to enhance these performances (ground connection, wire loop profile, down bonds implementation). But, these techniques will not be addressed in this paper.

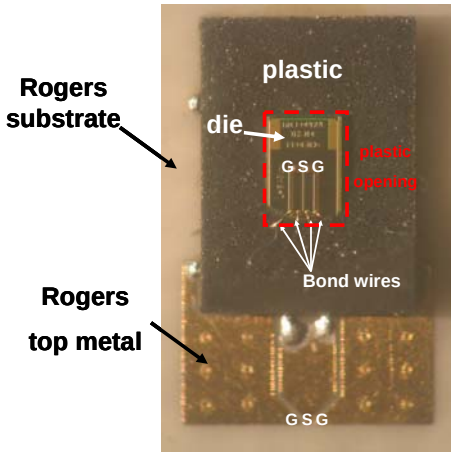
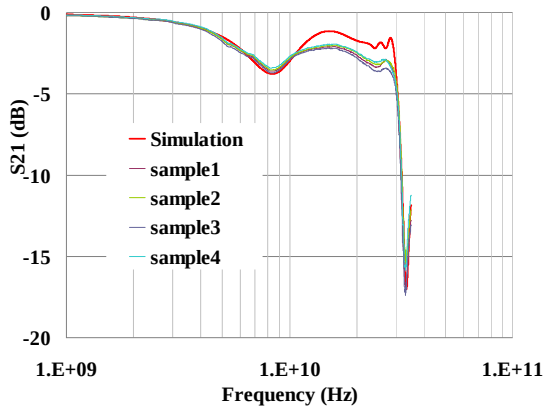


Figure 9. Photograph of the designed test-case suitable for microwave package characterization and modeling. Configuration allows 2 ports micro-probing: one on the inner die and the second one on the Rogers top metal (bottom of the picture)

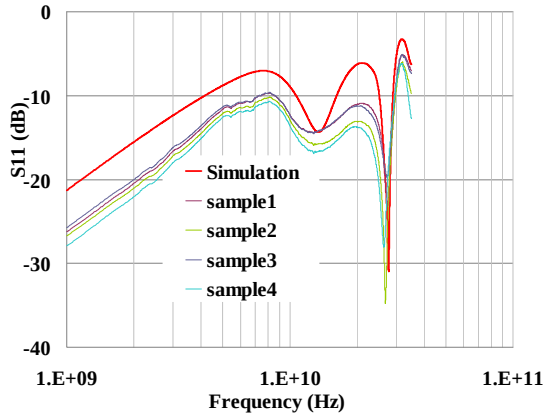
Aim of this section is to calibrate the 3D FEM solver EMPro from Agilent to correctly handle the S-parameter variations of the previously measured test-case. The 3D EM model should estimate the electrical performances of the package as accurately as possible, but on the other hand, should not be too complex for the EM simulations of more complex blocks. The following methodology has been applied:

- Bond wires cross-section have been first described with a square shape. Generally speaking, all round shapes should be avoided as much as possible as they are really time consuming for the simulations and the 3D mesh generation.
- Bond wire profiles were estimated based on a circle shape assumption as proposed by Alimenti et al. [31].
- Package terminals are defined into two equal steps (each is 100 µm thick) to have accurate modeling of the thick metal. One should try also to approximate their geometries with few corner points as possible but the modifications should not affect the electrical response of the simulator.
- Coplanar ports have been used on both the chip and substrate lines.
- All dielectrics are defined with finite bricks taking into account their relative permittivity and the loss tangent or the conductivity. Plastic brick is open with an "Air" brick in order to stick as much as possible to the measurement configuration.
- The common ground reference was set to the bottom metal of the Rogers substrate.

Both reflection and transmission S-parameter obtained from EM simulations are plotted in Figure 10 together with measured data. The simulated results corroborate the measured data with a good accuracy up to several tenths of gigahertz.



(a)



(b)

Figure 10. Comparison between measurements and simulated data vs. frequency on the package test-case – (a) transmission parameter, (b) reflection parameter

To conclude this part, the EM simulation tool enables relatively accurate and complex package analysis. So based on these two previously studied test-cases (solenoid and package) the FEM solver is calibrated and ready for embedded filter design with solenoid based TSV.

V. 4 GHz Band-pass Filter Modeling and Design

Based on the previous building blocks that have been studied in previous sections (i.e., package and solenoid measurements together with EM modeling), this part will focus on the design feasibility of a 4 GHz band-pass filter.

The objective is to design a band pass filter with a maximum of 4dB insertion loss.

A. Schematic design

First, a third order Chebyshev architecture has been considered to design a filter prototype. Nonetheless, taking into account coefficient in [32] and applying the well known transform from low-pass to band-pass filter, lead to an inductor value in the serial electrical path that is equal to 9.13 nH. Such an inductor will have a high serial electrical resistance that will seriously affect the insertion loss of the overall filter and will also have a Self-Resonant Frequency too close to operating frequency clearly limiting its usage. So, a choice has been made to split the filter into two different parts as shown on Figure 11 and already proposed in [16]. The first part is a 5th order low-pass filter while the second one is a 3rd order band-stop filter. Both are Chebyshev filters. By doing this, only MOM capacitors and small inductances values (i.e., 451 pH for L6 and L10) will be present in the serial path of the filters. This approach allows reaching the specified level of insertion loss.

All inductors will be designed using TSV with the same architecture as the ones presented in the first part of this document. The quality factors of inductors L6/L10 have been simulated prior to implementation and are equal to 10, which is sufficient for the targeted application. For inductors placed on the parallel paths (i.e., L1, L3, L5 and L9) their impact is really low regarding the insertion loss.

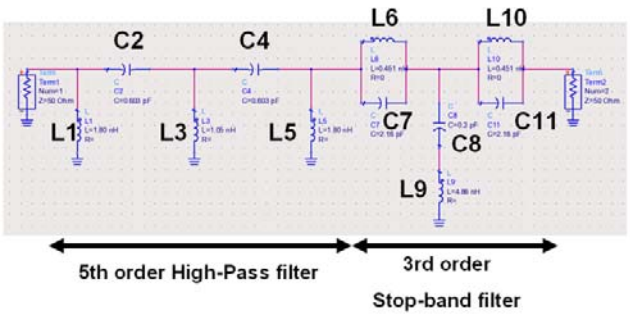


Figure 11. Schematic view of the 4 GHz band-pass filter considered for this study

For the capacitors, a choice has been made to use the "free" MOM capacitor offered by the process. In fact two metallization are present and can be patterned as well on the top-side of the wafer. They are separated by a classical oxide with a density of 0.1 nF/mm^2. A very low serial resistance value induced by the capacitor is expected to result from the use of two thick copper layers as device electrodes. Furthermore, very precise values of capacitance can be obtained since its relative precision is driven by the oxide thickness, which is really low (+/- 5%).

All these components will of course interact one with another leading to a change in the frequency response of the filter. That's why, a top level EM simulation is required to adjust and optimize the topology of the overall filter taking into account the interconnections as well as the ground return path.

B. Layout Implementation

Special care has been taken to optimize the electrical resistance on the serial path. Wherever possible, the RF path was designed by stacking both levels of metallization connected together using vias. Orientation and aspect ratio of capacitors have been chosen in such a way to minimize the resistive losses. A view of the simulated filter is shown on Figure 12.

First order dimensions of the solenoids (Dy, N) have been deduced from the analytical model provided in [22]. The value of the ground path inductance (metal tracks + bumps) is then taken into account as they participate to the self-inductance value from the RF path to the ground (inductors L1, L3, L5 and L9). The metal track inductances have been calculated in reference to partial inductance concept proposed by Ruehli and Zhong [33][34]. Electrical parameters of the bumps have been evaluated by calculation and single EM simulations as proposed in [35].

LC tanks (L6, C7 and L10, C11) in the stop-band filter have been realized with one-turn solenoids. Then prior to top simulations, each solenoid of the filter is placed with care in order to avoid as much as possible coupling between them. Typically the maximum space is considered, and an orientation of 90° between each inductor is applied to minimize magnetic coupling. Dimensions of the whole filter are 3.6x2.4 mm^2 and clearly outperform conventional microwave structures such as hairpin filter for similar application [30]. The full structure is then simulated within the package with the bump connection to the Rogers substrate. Results are presented on Figure 13.

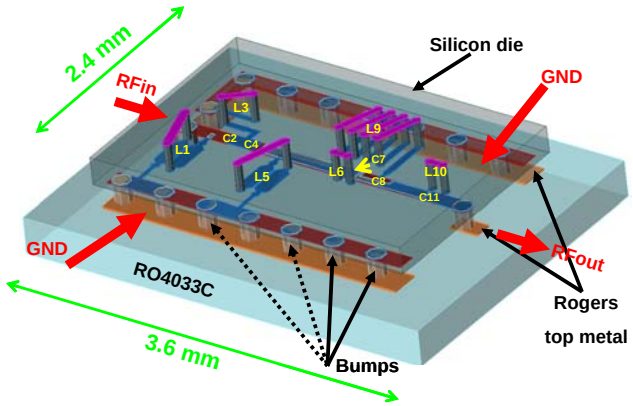


Figure 12. Top view of the simulated 4 GHz band-pass filter. Plastic of the package is not represented on the picture for clarity reason.

From the available results, the filter exhibits insertion and return loss of 2.6 and 16 dB respectively. Insertion losses are clearly within the specifications even if they are higher than classical micro-strip filters. The main contributors to the insertion losses are both inductors L6 and

L10 for whom electrical resistance increases very fast with the frequency.

C. Discussion

The approach described here gives indeed good results in case of moderate, loaded quality-factors (i.e., few units). Furthermore, it corroborates with the performances level already simulated by Georgia Tech on High Resistive Silicon (HRS) substrate [19]. On the other hand, it seems that this solenoid architecture is not appropriate in case of narrow fractional bandwidth where higher loaded quality factors are required.

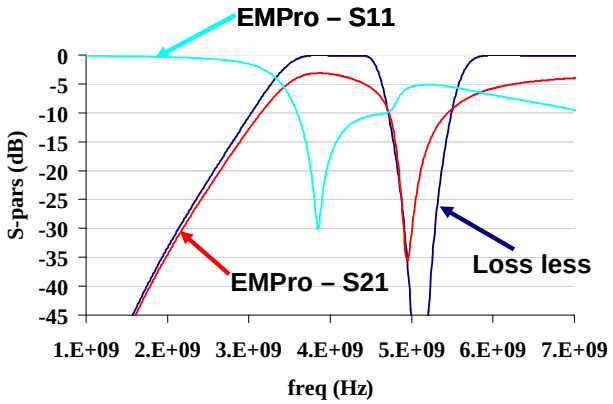


Figure 13. Simulation results of the proposed filter. Dark blue line corresponds to loss-less schematic filter simulated with ADS® schematic.

For these very specific applications, classical micro-strip filters deposited on low-loss substrates such as ceramic should be considered. TSV based solenoids can be used to build compact filtering applications up to several GHz. In fact, as shown by the solenoid characteristics on Figure 8(b) and Figure 8(d), the solenoid suffers from resistive losses at high frequencies on one side and from moderate SRF on the other side. The former effect is impacted by the classical phenomenon occurring at high frequencies within metallic conductors - the skin effect - while the latter one is due to the coupling capacitance between via metallization and the silicon substrate. One way to reduce it consists in using very high aspect-ratio TSV in combination with thinner silicon substrate. In the following part of this contribution, we propose to design a 42 GHz band-pass filter based on high aspect-ratio vias (50/7). In that case, solenoid type of component should be avoided and different filter architecture must be proposed.

VI. V-BAND BAND-PASS FILTER MODELING AND DESIGN

TSV building brick has been identified as a key enabler in view of promoting either C2C (chip to chip), C2W (chip to wafer), W2W (wafer to wafer) 3D IC integration in order to support high performances chips [37]. In a recent work [1], and in the previous study depicted in this document, we have shown some results obtained on 3D based solenoids band-pass filter at 4 GHz. Idea was to use low aspect ratio TSV to make embedded solenoids. Q-factor of the obtained devices was really promising (vs. planar solutions) especially below 5 GHz [22]. However, the devices suffer from the low self-resonant frequency due to the parasitic capacitance between the metal from the via and the silicon substrate, clearly limiting the range of applications of this kind of devices to the L and S bands. In fact, the capacitance between the via and the substrate is given by the following relation:

$$C_{val} = \frac{2\pi . \varepsilon_o \varepsilon_r h}{ln\left(\frac{R_2}{R_1}\right)} \quad (4)$$

In this relation, R_1 is the inner radius of the via while R_2 is the outer one. R_2-R_1 is no more than the thickness of the diffusion barrier between metal and the substrate. Typically, for low aspect ratio via considered in this study, this capacitance is in the order of 11 pF; so its impact is not negligible on the solenoid SRF.

So, one can clearly see the interest of using high aspect ratio vias with reduced substrate thickness down to 50 um. Furthermore, this will have an impact on solenoid density. So, for the filter proposed in the following part of this document, the architecture will be updated to avoid using solenoid that are clearly not suitable for high frequency operations (V-band targeted here). The second interest of TSV at high frequencies is the availability of such interconnect to make a clean and short connection to the ground reference (bipolar emitter, …). Indeed, this is a crucial point for millimeter-Wave applications and TSV will certainly help improving it like it is done in most of AsGa based processes [38][39]. In the following section of this paper, we propose to use intrinsic properties of TSV to make a short inductance value together combined with a clean ground connection in order to make a 3rd order 42 GHz band-pass filter. First, details about the filter architecture are given. Then another paragraph is devoted to the practical layout implementation of each of the sub-blocks of the filter. Prior to filter simulation, EM simulation results of the transmission lines used in the filters are given and compared to measurement data. Finally an analysis related to different process options is given at the end.

A. 42 GHz filter architecture

Our first idea was to reproduce a classical 3rd order Chebyshev filter. Applying the well-known transform from low-pass to band-pass filter and using the ad-hoc coefficient found in [32], it comes out that a 0.76 nH inductor appears to take place in the serial path of the filter (i.e., the serial LC resonator). In addition, the self-inductance values of the parallel resonator are in the order of 50 pH, which is weak and can be achieved with the help of one TSV. A 0.76 nH solenoid is easily achievable but will not support 40 GHz applications. The self-resonant frequency (SRF) is by far below this value. That's why, it has been decided to remove

the serial LC resonator and replace it by one parallel resonator placed between two λ/4 micro-strip lines. Doing that way, only 50 pH to 65 pH inductors are necessary to design the filter. Such inductance will be then TSV based. So the filter will use the well-known property of the quarter-wave lines to invert impedances. The schematic of the filter is provided on the figure below:

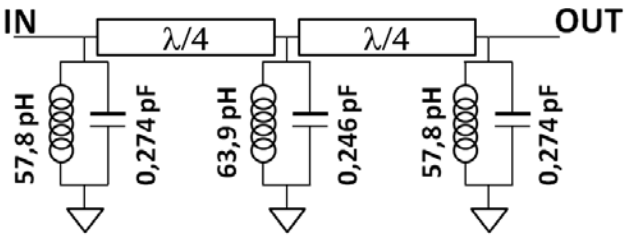


Figure 14. Schematic view of the 3rd order 42 GHz band-pass filter considered

So, basically, the filter will require the implementation of transmission lines, metal-oxide-metal (MOM) capacitors and short connections. The following part of this document will focus on the implementation of each of these sub-blocks.

B. Physical layout implementation

All devices that are used in this study are compliant with classical IC design rules (for this example, we have applied rules from NXP in house BiCMOS process).

1) Transmission Lines EM modeling

A synoptic representation of a transmission line pattern is proposed on the following figure:

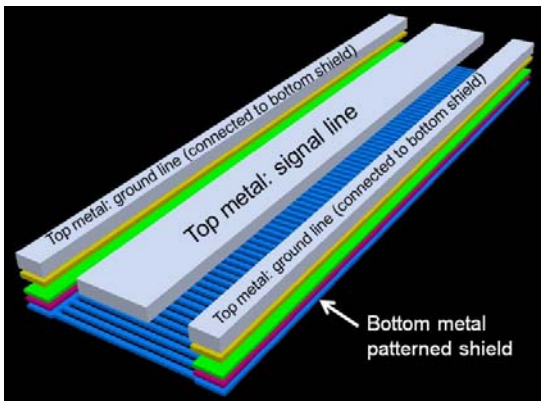


Figure 15. Layout pattern of the considered transmission lines used to calibrate the 3D EM simulator

Transmission lines considered here are mandatory to calibrate the 3D EM solver (i.e., EMPRo) and are based on the slow-wave concept and uses the latest metal level of the BEOL (Back-End Of Line) to propagate the signal. Typically, in this study, it is a 3 µm thick copper layer. All of them have been measured up to 110 GHz with a network analyzer from Agilent Technologies. Prior to parameter extraction, de-embedding was performed using a classical two-steps Open-Short method. A typical view of a transmission line between GSG pads is proposed on Figure 16. The bottom metal layer of the process is used for two main purposes:

- To shield the line and thus reduce and prevent the losses within the substrate. In fact, the metal shield is implemented in order to block the electric field penetration inside the lossy substrate. On the other side, a patterned design is adopted to be compliant with design rules and also to break current loops in it. In fact, these loops can have a significant impact on line attenuation.
- To connect the bottom face of the chip using TSV. TSV are used to connect the ground plane for the micro-strip line to the back side of the chip, which is indeed the real ground reference.

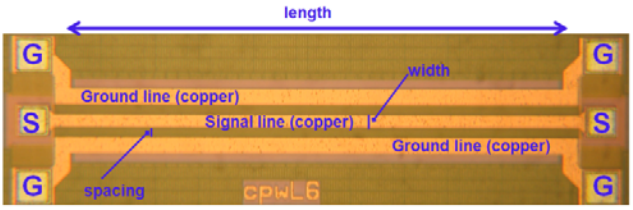


Figure 16. Photograph of a transmission line within GSG pads for two-ports S-parameter measurements, used to calibrate the 3D EM simulator

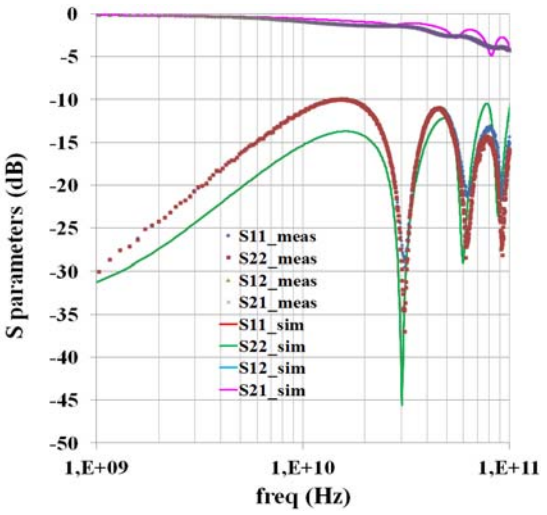


Figure 17. Comparison between simulated (EM) and measured S-parameter obtained on a transmission line (length = 2000 µm, width = 15 µm , spacing = 8.3 µm)

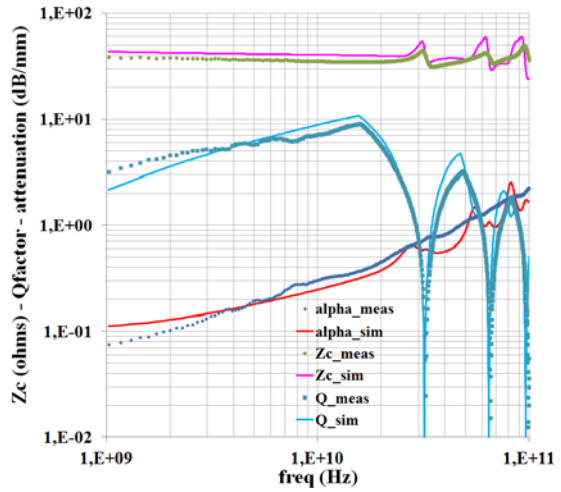


Figure 18. Comparison between measured and simulated data vs. frequency for transmission line characteristic impedance Zc, attenuation alpha and quality factor Q (length = 2000 µm, width = 15 µm, spacing = 8.3 µm)

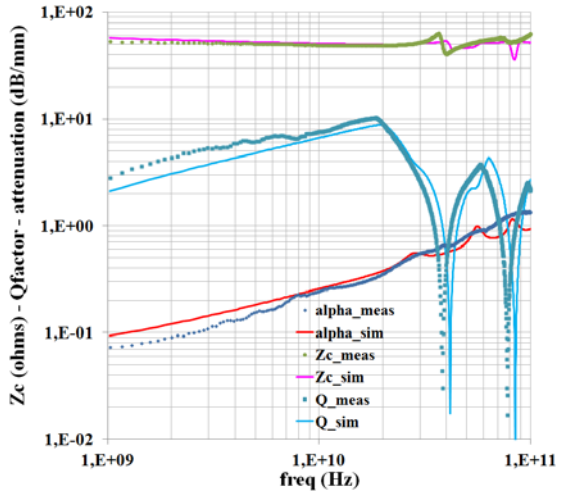


Figure 19. Comparison between measured and simulated data vs. frequency for transmission line characteristic impedance Zc, attenuation alpha and quality factor Q (length = 2000 µm, width = 15 µm, spacing = 8.3 µm, 4 bends)

A physical wide-band electrical modeling has been already proposed to deal with the electric behavior of such devices [44]. The accuracy is really excellent but like for solenoid this model can of course not take into account the global environment of the line. That's why, again an EM model is mandatory to correctly simulate the filter response.

EM simulator has been calibrated based on measurements performed up to 110 GHz on various geometric variants of the previously described transmission lines. Calibration has been performed based on S-parameter variations and extracted parameters. These electrical parameters are:

- The characteristic impedance Zc (ohms)
- The attenuation α (dB/mm)
- The quality factor Q

Based on the available data and results, the correlation between measurements and EM simulations is really satisfying up to 110 GHz. From a performance point of view, the attenuation constant is equal to 0.66 dB/mm, which is in good agreement with results already published in the literature [40]. The patterned shield plays a significant role in reducing the attenuation of the lines (i.e., in the order of 1.3 dB/mm without shield [41]). This is the last building brick necessary to achieve the design of the 42 GHz band-pass filter.

2) Filter implementation

The proposed transmission lines have a width of 15 µm and the ratio width/height (W/H) is equal to 1.75 to ensure a 50 ohms configuration. The simulated attenuation is equal to 0.53 dB/mm and the total length of each line is equal to 1.134 mm leading to an overall attenuation of the lines equal to 1.21 dB. Based on simulations, characteristic impedance of the transmission lines, Z_c, has been found equal to 50.5 ohms at 42 GHz. Taking into account this value, the new parallel inductance and capacitance values (see Figure 14) are calculated using the initial values deduced from the ad-hoc coefficients of the Chebyshev filter synthesis:

$$C_{new} = \frac{Y_c^2}{C\omega_0^2} \quad (5)$$

$$L_{new} = \frac{Z_c^2}{L\omega_0^2} \quad (6)$$

where Z_c is the characteristic impedance of the line (i.e., 50.5 ohms), $Y_c=1/Z_c$ and $\omega_0=2\pi f_0$ (f_0=42 GHz).

MOM (Metal Oxide Metal) capacitors are designed using two levels of metallization. Bottom level uses the lowest level offered by the process (same as the ground plane for transmission line) while top metal is used for the top electrode. Doing like that, an average density of 4.5 pF/mm^2 is achieved allowing designing capacitors with values up to 0.5 pF. Like for transmission lines, the lowest metal is connected to the ground reference with the help of TSV. It should be noted here that high aspect ratio vias allow decreasing the ground short inductance, which is mandatory at very high frequencies.

A special care has been taken during the implementation of the capacitor in order to reduce as much as possible the parasitic inductance value. In that sense, the form factor of the device must be chosen accordingly with a high ratio width/length.

Regarding the parallel inductances and short connections, the basic idea here consists in using the TSV to make the parallel inductance in the LC resonator and thus the connection to the ground reference. The self-inductance of a single via can, of course, not be changed and exhibits a fixed value of 22 pH (deduced from EM simulations). In order to adjust the parallel self-inductance value, the length/width of the metal track that connects the λ/4 lines to

the vias can vary. At the same time, as explained in the previous part of this paper, each TSV will also present a parasitic capacitance to the substrate due to the presence of the diffusion barrier. In our case, this capacitance is equal to 12.8 fF/via. It is then necessary to adjust the final value of the MOM capacitances taking into account the capacitance inherited from the TSV.

Finally, the layout topology of the filter is proposed in Figure 20.

C. Simulation results

EM simulations have been performed up to 80 GHz on the previous structure taking into account nominal process parameters. Prior to simulations, the bottom metal patterned shield has been simplified to decrease the mesh complexity as well as the simulation time. On the other side, these simplifications must lead to the same level of accuracy. So, the patterned metal shield is made of metal fingers of 5 µm width and 1 µm spacing. The filter has been simulated in its global environment including the bumps to connect it to the active die, and with and underfill material between the stacked dies (not represented on the figures above). Simulation results are proposed in the figure below:

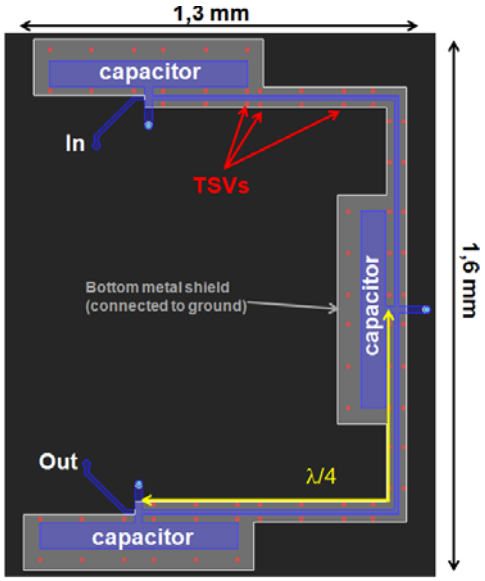


Figure 20. Top view (a) and 3D view – the gray bottom plate is the ground reference of the device (b) of the simulated band-pass filter

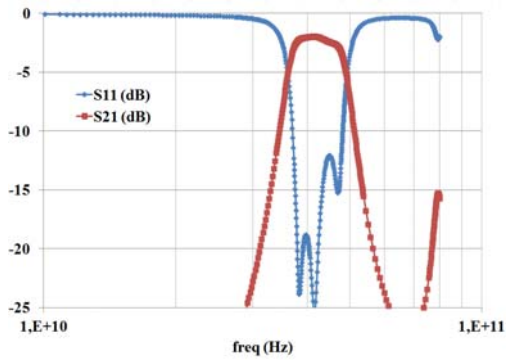


Figure 21. Simulated variations of transmission and reflection S-parameter of the proposed filter (nominal process parameters with copper back-end)

IL (Insertion Loss) and RL (Return Loss) are found to be equal to -2.0 dB and -18.5 dB respectively at 42 GHz. It appears that the losses are mainly dominated by the transmission lines losses. One way to reduce these losses consists in using thicker metal but requires process updates that are not always compliant with cost efficiency. The bandwidth of the filter at -3 dB is equal to 12.3 GHz, which was predicted by the theory. The filter exhibits a reduced footprint of about 2 mm^2 compared to classical interposer done with LTCC substrate [42] [43]. A summary of simulated filters intrinsic properties is proposed in the table below:

TABLE I. OVERVIEW OF FILTERS CHARACTERISTICS

	C-band filter	**V-band filter**
	Low-density TSV	***High density TSV***
f_0	4 GHz	42 GHz
IL[a] at f_0	-2,6 dB	-2,0 dB
RL[b] at f_0	-16,0 dB	-18,5 dB
Frac. Bandwidth[c]	16 %	29 %
footprint	8,6 mm^2	2 mm^2

a. Insertion loss
b. Return loss
c. Bandwidth is calculated at -3dB

However, the level of performance might be improved by looking into the best process options. Simulations have been performed in that sense and are presented in the last part of this work.

D. Process options

Several process options have been considered for investigation purpose:

- Thick copper: 8 µm instead of 3 µm
- Substrate resistivity: 20 ohms.cm instead of 200 ohms.cm
- BEOL: Al back-end instead of Cu back-end

Simulation results are on the following graph:

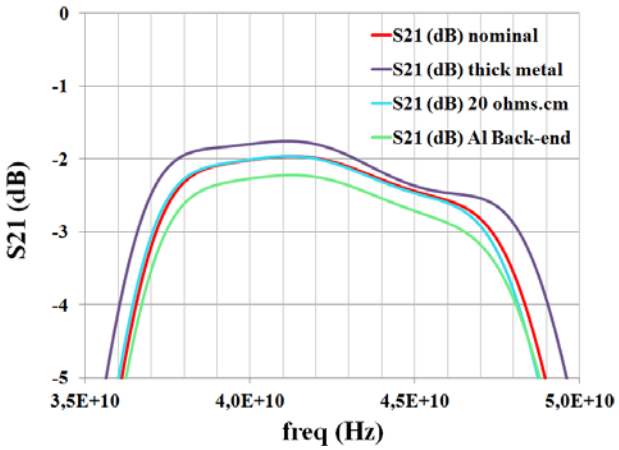


Figure 22. Variations of the Insertion Loss vs. frequency for different process options

Based on available results, one can clearly see that if a shield metal is used to block the penetration of electrical filed, the silicon conductivity has a minor impact on the insertion loss of the filter (provided that the substrate resistivity is between 10 and 1000 ohms.cm). Indeed, as already mentioned earlier, the losses are dominated by resistive losses within the transmission lines.

On the other side, one can remark that moving from Cu BEOL to Al BEOL only degrades the IL by 0.3 dB. Then this is a trade-off between process cost – compatibility between Al metal and Cu vias – process reliability. In the same way increasing the Cu thickness from 3 to 8 µm, only improves the IL by 0.2 dB. This point can be clearly understood if we take into account the skin depth of these materials at 42 GHz (i.e., 0.3 µm for Cu and 0.43 µm for Al). In fact it is relatively small compared to metal thickness. Conclusions would have been of course completely different for applications at lower frequencies (<5 GHz). But in that case such as design with λ/4 on silicon lines does not make sense.

- Changing the substrate resistivity also have a minor impact on the results for two reasons essentially: the presence of a bottom metal shield is the key point to reduce the transmission line losses within the substrate as suggested by [44]
- The use of high aspect-ratio within a "thin" substrate reduces drastically the losses induced by the TSV together with parasitic capacitive coupling with the substrate.

VII. CONCLUSION AND PERSPECTIVES

In this paper, two band pass filters for 3D-IC integration are proposed. The former one centered at 4 GHz is based on low aspect-ratio TSV and uses 3D integrated solenoid to design inductive elements. The latter is made of high aspect-ratio TSV combined with thin substrate. It uses λ/4 transmission lines to make impedance inverters and thus inductive elements are designed using single vias. Capacitive elements are classically made with MOM devices for both types of filter. The electrical characteristics of each single element on silicon (transmission lines, integrated solenoid, single via) have been measured up to 110 GHz and results have been cross-checked with 3D FEM data in order to make the 3D EM solver calibration. Modeling of the passive interposer's environment (i.e., the package and the under fill material) is also proposed and correlated to EM simulations. An original package characterization technique is also reported. It allows package modeling up to 50 GHz with high accuracy together with conventional measurements setup.

For both filters, good performances have been achieved. A bandwidth of 16% and 29% are reached with insertion loss of -2.6 dB and -2.0 dB combined with return loss of -16 dB and -18.5 dB respectively at the center frequencies for the S-band and V-band filters. It appears from these results that TSV based filtering applications are suitable for moderate loaded quality factor devices – typically few units. Classical micro-strip filters on LTCC should be preferred for very high loaded quality factors [45][46]. Investigation based on different process options is also proposed on the V-band filter. From available results on filter performances, they clearly highlight the interest of an efficient shielding technique rather than process updates. The presented technologies here show significant potential for millimeter-wave applications and are expected to allow 3D IC integration of high performances circuits. In fact, in order to reduce the footprint and enhance the performances of the products, a displacement from wire-bonding technology to flip-chip technology with TSV based passive interposers will take place. This new approach will help reducing the products size, weight and cost.

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