Defining the Optimal Architecture for Multi-Standard Radio Receivers Embedding Analog Signal Conditioning

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***Abstract*—This paper focuses on finding the optimal architecture for a multi-standard radio receiver embedding analog signal conditioning compatible with the major commercial wireless standards. By developing a standard independent methodology, the paper addresses systematically the large amount of information comprised in the envisaged standards. Based on the systematic approach, the multi-standard receiver main electrical requirements are defined and their values determined. The presented results constitute the starting point in building a multi-standard wireless receiver.**

Keywords-software defined radio; receiver electrical specifications.

I. INTRODUCTION

At the beginning of the mobile Internet age, it becomes clear there is a strong need of mobile equipment able to maximize its wireless connectivity.

There are several reasons that make extremely attractive the usage of multi-standard radio transceivers to enable the wireless interoperation of such mobile equipment, [1,2].

Firstly, a multi-standard solution is efficient as only one design is required to handle the mobile device wireless communication. Thus, the number of different dedicated ICs or IP blocks inside a large SoC is reduced. This simplifies the overall communication platform integration.

Secondly, since only one design is required to cover for all the targeted wireless standards all cost related to the IP development and testing are minimized.

The ideal multi-standard receiver was proposed by Mitola in [3]. The Software Defined Radio Receiver (SDRR) shown in Fig. 1.a is the optimal choice from system level perspective, as it comprises only an ADC.

In reality, due to practical implementation constrains, a multi-standard receiver requires a signal conditioning block in between the antenna and the ADC. The SDRR concept shown in Fig. 1.b relaxes the ADC specifications by ensuring additional selectivity and amplification for the wanted signal.

First, the paper focuses on finding the optimal architecture for the SDRR signal conditioning block that enables its monolithic integration.

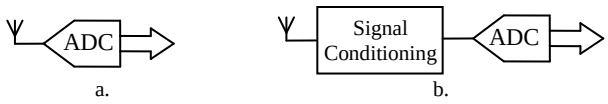

Figure 1. a. Mitola SDRR Concept, b. SDRR embeding signal conditioning.

Based on a detailed overview of the key receiver architectures, Section II introduces the optimal architecture for a SDRR that targets compatibility to the major commercial wireless standards listed in Table I.

Second, the paper pursues the identification of the SDRR key electrical requirements and their values. Based on a systematic approach, the paper introduces a standard independent methodology for evaluating the SDRR performance.

Section III defines the SDRR receiver sensitivity, NF and gain requirements, while Section IV analyses the blocker and interferers impact on the SDRR linearity requirements. Section V concludes the paper.

II. INTRODUCING THE OPTIMAL ARCHITECUTRE OF THE SIGNAL CONDITIONING BLOCK

This Section covers one of the paper's goals that is to find the optimal architecture for the SDRR signal conditioning block enabling its monolithic integration. In Section II.A, the key receiver architectures are analyzed, while Section II.B determines the quadrature direct conversion topology suits best the envisaged purpose.

Section II.C overviews the architectural changes that make the homodyne receivers ready for monolithical integration. The presented solutions are realized without introducing particular analog tricks to satisfy the needs of only one of the standards, as the SDRR must represent "universal receivers", and not be turned into a "multi-standard ASICs".

A. Overview of Key Receiver Architectures

First of all, one of the most popular receiver architectures is the heterodyne architecture. It was developed in 1918 by Edwin Armstrong as a viable alternative to the regenerative receiver with respect to the technical issues of vacuum tubes implementation, [4].

TABLE I. TARGETED MAJOR COMMERCIAL WIRELESS STANDARDS KEY SPECIFICATIONS

Wireless Standard		Frequency Plan [MHz]		Modulation Type	SNR_0 [dB]	RF Signal BW / Channel Spacing [MHz]	Specified Sensitivity [dBm]	Sensitivity @ NF_{RX} = 3 dB [dBm]
		Downlink	*Uplink*					
GSM, [5]	GSM 850	869 ÷ 894.8	824 … 849.8	GMSK	9	0.2	–102	–109
	GSM 900	935 ÷ 960	890 … 915					
	DCS 1800	1805 ÷ 1880	1710 … 1785					
	PCS 1900	1930 ÷ 1990	1850 … 1910					
UMTS, [6]	I	2110 ÷ 2170	1920 ÷ 1980	QPSK	−18 (@ 12.2kbps)	3.84 / 5	–117	–123
	II	1930 ÷ 1990	1850 ÷ 1910					
	III	1805 ÷ 1880	1710 ÷ 1785					
Bluetooth, [7]		2402 ÷ 2480		GFSK	16	1	–70	–94
DECT, [8]		1880 ÷ 1980, 2010 ÷ 2035		GFSK	13	1.2 / 1.736	–83	–97
WLAN IEEE 802.11b (DSSS), [9]	1 / 2 Mbit/s	2400 ÷ 2485		DBPSK / DQPSK	−4 / −2	14 / 5	–80	–104 / –102
	5.5 / 11Mbit/s			CCK	9 / 11		–76	–91 / –89
WLAN IEEE 802.11a,g (OFDM), [9]	6 / 9 Mbit/s	5150 ÷ 5350 & 5725 ÷ 5825 (a) 2400 ÷ 2485 (g)		BPSK	4 / 5	16.6 / 20	–82 / –81	–95 / –94
	12 / 18 Mbit/s			QPSK	7 / 9		–79 / –77	–92 / –90
	24 / 36 Mbit/s			16QAM	12 / 16		–74 / –70	–87 / –83
	48 / 54 Mbit/s			64QAM	20 / 21		–66 / –65	–79 / –78

The basic block schematic of this concept is depicted in Fig. 2. The original superheterodyne uses only one downconverter mixer (i. e., single conversion superheterodyne), and mixes the Radio Frequency, RF, input signal with the Local Oscillator, LO, signal.

The resulting signal frequency is mixed down by the mixer (i. e., MIX in Fig. 2), to an Intermediate Frequency, IF, equal to the difference between the RF carrier and LO signal frequencies.

Intrinsically the mixing process will render at the mixer output also the sum frequency component. For most applications this component represents an unwanted signal and is filtered by the band pass filter (i. e., BPF in Fig. 2) following the mixer and/or in the mixer output stage.

The major issue of the heterodyne topology is the image frequency rejection.

The issue is two symmetrical signals with frequencies spaced apart by twice the IF frequency are downconverted by LO mixing to the same IF frequency, as shown in Fig. 3.

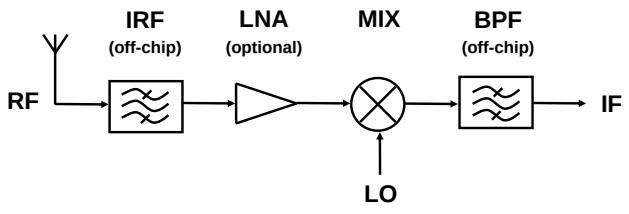

Figure 2. Single Conversion Superheterodyne Receiver Block Schematic.

Generally, only one of the two sideband signals conveys useful information, while the other represents an unwanted image signal.

Thus, for superheterodyne receivers image signal rejection is critical for a proper signal demodulation.

The superheterodyne architecture solves the issue by filtering the image signal before it enters the mixer, or more precisely, immediately after the antenna in the external image reject filter (i. e., IRF in Fig. 2).

The image rejection filter specifications depend on the IF value and they are more relaxed as the image frequency is larger, respectively as the distance between the RF carrier and its image is larger.

Signal conditioning constraints, set by the channel selection filter located after the down conversion mixer (i. e., the second band pass filter of Fig. 2), prevent the choice of a very large IF. This toughens image filtering requirements. In practice, ceramic filters satisfy the constraints, but they possess two major drawbacks: they are quite expensive and by far not compatible with monolithic integration.

Channel selection is also demanding, as for many applications channel bandwidth is fairly small compared with IF. In such context, bandpass Surface Acoustic Wave (SAW) filters are used for analog channel selection. But, these types of filters are unattractive to SoC ICs for the same two reasons as the ceramic antenna filters: incompatibility with monolithic integration and high cost.

Basically, single conversion superheterodyne receiver design is driven by the trade-off between antenna and channel filtering, which imposes the optimum IF frequency.

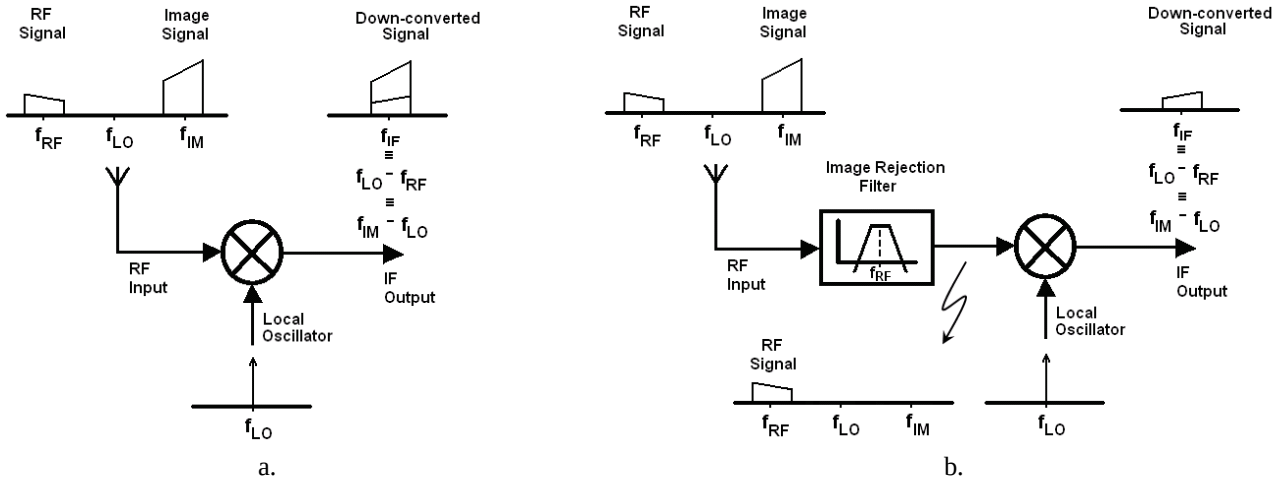

Figure 3. Down-conversion: a. without Image Rejection and b. with Image Rejection.

Second of all, so far, the design of superheterodyne receivers has been optimized to alleviate image rejection rather than optimizing RF performance. Thus, using an image rejection receiver that implements a complex mixer to cancel out the unwanted image signal, removes the lock on architecture enabling the RF performance optimization. The principle schematic of such a receiver is depicted in Fig. 4.a.

The complex mixer is made out of two mixers which share the same RF input, while the LO port is controlled by two quadrature signals. By adding a 90 degrees delay line in one signal path, the down converted image signals will be in-phase, while the useful signals will be 180 degrees delayed. Hence, by considering the difference between the two paths the image signal is cancelled, while the useful signal is added. The major advantage of this approach is the antenna filtering becomes less critical. Thus, the use of expensive and bulky, external (off-chip), ceramic filters are no longer required. On the other hand, the image rejection now depends on the quadrature accuracy of both gain and phase of the LO and IF paths. If the two LO signals exhibit exactly 90 degrees phase delay and have the same amplitude, while the gain of the two paths are perfectly matched, the unwanted image signal is completely rejected.

Hence, image rejection receivers cancel out the image signals by subtracting two – potentially very large – signals, resulting in a difference that is theoretically equal to zero.

However, any gain error or phase error between the two signal paths will determine an incomplete annihilation of the image signal. Thus the image rejection, *IR*, is given by, [10]:

$$IR = -20\log\left\{\frac{1}{2}\left[\frac{Gain_{I-Q\,err}}{Gain} + tg\left(Phase_{I-Q\,err}\right)\right]\right\} \quad (1)$$

where *Gain* represents the receiver's gain, $Gain_{I\text{-}Qerr}$ is the I-Q gain mismatch and $Phase_{I\text{-}Qerr}$ is the I-Q phase mismatch.

Since accurate wide-band quadrature phase shifters are difficult to design, Weaver receivers of Fig. 4.b are preferred.

To cancel the need for the 90 degrees phase shift on the signal path an extra pair of mixers and quadrature LO signals are required. Still, the LO signals quadrature accuracy, of both gain and phase, and the gain matching of the quadrature downconverted channels set the image rejection performance as described by (1).

Third of all, all receiver architectures presented so far have to fight image rejection. In direct conversion receivers also known as homodyne receivers, the IF frequency is zero, hence, the useful signal is its own image.

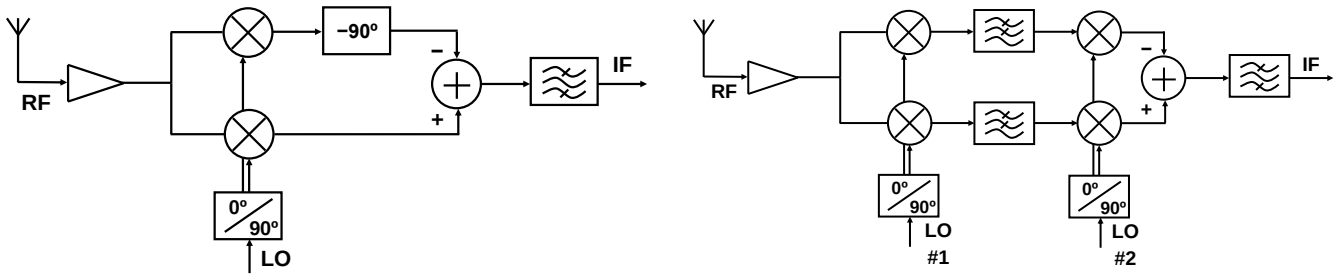

Figure 4. a. Image Rejection Receiver and b. Weaver Receiver.

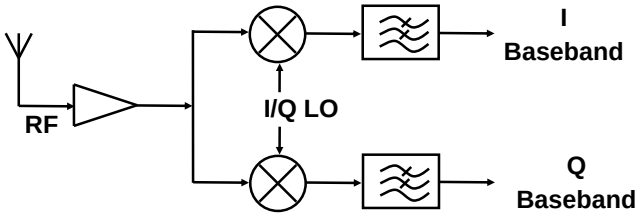

Figure 5. Quadrature Direct Conversion Receiver Block Schematic.

Therefore, in a homodyne receiver (see Fig. 5) the image signal has an amplitude comparable to the useful signal, and hence, image rejection requirements are relaxed. Furthermore, all baseband processing, like analogue filtering, analog-to-digital conversion and the digital demodulation, take place at the lowest possible frequency.

These features make the homodyne receiver an ideal candidate for monolithic integration and open the possibility of creating an "*universal*" receiver, compatible with all wireless standards, [4].

However, although direct conversion receivers monolithic integration seems straight forward there are several drawbacks to this approach.

The second major issue of direct conversion architecture is that even order distortions generate a signal dependent DC offset.

Another issue of such architecture is self-mixing. Basically, the LO signal, which in most cases is orders of magnitude larger than the RF signal, leaks to the RF port of the mixer and it will be mixed down to baseband. If the LO leaking signal is phase shifted with respect to the real LO, this almost always being the case in practice, the DC offset caused by self-mixing may dominate the mixer output.

Finally, although direct conversion architecture has relaxed image rejection specifications, it has to fight with DC offset, 1/f noise and self-mixing.

Hence, the low-IF architectures (see Fig. 6) become attractive. Essentially, the RF signal will now be downconverted to a low IF frequency (i. e., up to a few hundred kHz) and thus, the issues of direct conversion receivers are alleviated.

But, the image rejection requirements are again tight. This stresses the implementation of the active poly-phase filter that follows the mixer and is used for image rejection and channel selection.

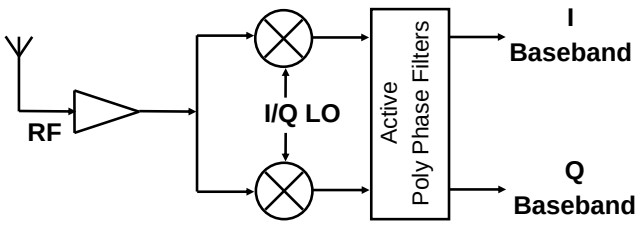

Figure 6. Low-IF Conversion Receiver Block Schematic.

B. SDRR Architecture Choice: Heterodyne vs. Homodyne

The main features of a SDRR must be a versatile architecture and the ability to be reconfigured on-the-fly as the communication burst requires.

From the perspective of SoCs, the optimization of the chip power dissipation and die area is mandatory. As the SDRR will be a part of a SoC, this trade-off must be the main guideline in sizing the SDRR design, as well as in choosing its architecture, as a first and, very important, starting point.

From area perspective the cumbersome image rejection filters of superheterodyne topology are not so attractive for monolithic integration.

On the other hand, for direct conversion architecture the image rejection requirements are much smaller than for any other receiver architecture.

Furthermore, the IF selection for superheterodyne architectures is fairly cumbersome and cannot be extrapolated in a systematic way to all standards, as it would be required for a true SDRR, [11].

The IF should be chosen to avoid the in-band down-conversion of strong interferers. In most applications the nearest strong interferers is located three channels apart from the RF carrier, [12]. As the channel bandwidth differs even within the same wireless standard, it is not possible to select intermediate frequencies which will lead to reuse of same image filters for a multi-standard environment compatible receiver.

Similarly, it is difficult to design an accurate wide-band 90° phase shift block for the image rejection receiver of Fig. 4.a, as imposed by a multi-standard application. Also, the fact the Weaver receiver from Fig. 4.b requires a cascade of two complex mixers increases the overall receiver area and power consumption, while it is also constraining its image rejection capabilities.

From power consumption perspective the homodyne topology has even more advantages. First of all, the baseband signal processing takes place at the lowest possible frequency. Secondly, this topology is not tributary to the 3 dB noise penalty of superheterodyne architectures, [11].

Hence, the SDRR architectures of choice are superheterodyne, homodyne or low-IF.

Table II summarizes the advantages and disadvantages of the three architectures with respect to monolithic integration in a SDR SoC.

Given the overview presented in Table II, it becomes clear the direct conversion receivers represent the optimal choice for satisfying the requirements of a true SDRR.

This has been validated through several circuit implementations in CMOS processes, [1, 13-15].

As noted, zero-IF receivers are susceptible to multiple issues (e. g., DC offset, 1/f noise, the self-mixing process), which make their monolithic integration quite a challenging task. All these aspects will be discussed in the following sub-section.

TABLE II. SUPERHETERODYNE, HOMODYNE AND LOW-IF RECEIVERS FOR SOC INTEGRATION – PROS AND CONS

Superheterodyne		Homodyne		Low-IF	
PROs	CONs	PROs	CONs	PROs	CONs
☺ Well known	☹ Requires off-chip components Ceramic antenna filter SAW Filter	☺ Less external components No ceramic antenna filter No SAW Filter	☹ DC Offset	☺ no DC Offset	☹ High image rejection requirement
			☹ 1/f noise	☺ reduced 1/f noise	
	☹ IF selection Difficult to mitigate the multi-standard environment	☺ Image is wanted signal mirror Mirror signal is not a strong interferer	☹ self-mixing	☺ reduced self-mixing	
	☹ Power consumption BB signal conditioning is done at IF	☺ Power consumption BB signal conditioning is done at lowest frequency			
	☹ 3 dB noise penalty, [10] Image frequency band degrades receiver SNR by 3 dB	☺ No 3 dB noise penalty Quadrature receiver			

C. *Making the Homodyne Architecture Ready for Monolithical Integration*

As detailed in the previous sub-section and in-depth analyzed in [16], due to intrinsic operation of homodyne systems, they exhibit a large sensitivity to DC offset, either static or dynamic, and 1/*f* noise. Also, self-mixing issues can dramatically reduce performance of receivers implemented with direct conversion architectures.

First of all, homodyne architecture is extremely sensitive to static DC offsets and 1/*f* noise. As for some wireless standards a large part of the signal energy is found at low frequencies (e. g., GSM), the down-converter mixer output is DC coupled to the anti-alias LPF. Thus, the receiver output risks of being overloaded even for small values of the DC offset, in the order of a few hundreds μV given the large VGA gain, usually larger than 60 dB, [17]. Regular AC coupling will not solve the issue, as receiver settling will be severely affected by a low cut−off frequency in the order of a few hundred Hz.

Hence, the receiver must embed an offset calibration loop.

One possibility is to use the correlated double sampling offset compensation technique, [18]. This is preferred to chopper stabilization, [19], as there is no risk of spurs overwhelming the receiver output spectrum. The receiver block schematic embedding offset calibration is shown in Fig. 7, redrawn from [16].

In the first phase (i. e., *Offset_meas* control signal is "High" – switches closed) the baseband chain DC offset is sampled on a capacitor, via the additional transimpedance amplifier, while the antenna input is shorted to ground, [10].

During normal operation, the second phase (i. e., *Offset_meas* is "Low" – switches open), the RF input is connected back to the antenna and the signal flows through the receiver, while the DC offset is inherently cancelled out.

The static DC offset compensation loop will also reduce the 1/f noise level.

The Fig. 7 receiver embeds multiple LNAs to mitigate the multi-standard frequency plan requirements from Table I.

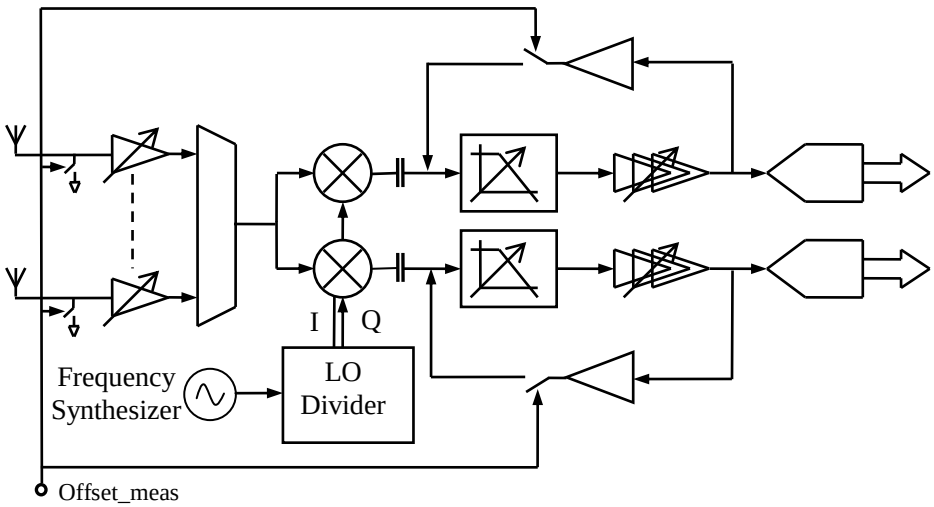

Figure 7. Low-IF Conversion Receiver Block Schematic.

The second major issue of the homodyne receiver architecture is the signal dependent DC offset generation due to even order distortions. the received input power can change dynamically, since other transmitters may start to communicate, a dynamic offset component is generated due to the receiver second order non-linearity. Therefore, dynamic offset compensation, to the extent required by almost all commercial wireless standards, implies the usage of a differential architecture for the whole receiver chain, starting with its LNA.

Thirdly, the self mixing process, determined by the LO mixing with the LO signal leaking the VCO to the receiver input, can generate a large DC offset overloading the receiver output. Hence, the VCO must not oscillate at the same frequency with the RF carrier frequency. Hence, the quadrature LO signals driving the downconverter mixer must be obtained by dividing down the VCO frequency in the LO divider block from Fig. 7 (e. g., [20]). Moreover, very good isolation between RF and LO mixer ports is required for good receiver performance.

III. Defining the SDR Sensitivity, Noise Figure and Gain Requirements

A. Introducing the Minimum Signal-to-Noise Ratio Required for Proper Signal Demodulation, SNR_0

The front-end must be able to downconvert the useful signal without hampering its electrical properties, such as the baseband processor is able to demodulate the information within a specified Bit Error Rate (*BER*). Basically there is a minimum SNR at the receiver output, SNR_{out}, required for the digital demodulator to properly demodulate the useful signal. This minimum SNR_{out} value is further on denoted as SNR_0.

As expected, higher SNRs are required to demodulate the signal within the same BER as the modulation number of bits per symbol increases.

Increasing the SNR requirements is achieved at the cost of higher power consumption, by increasing the signal power, or at the cost of lowering the bandwidth. In any case, there is a trade-off between power consumption and BitRate (*BR*). This can be mathematically expressed as follows:

$$\begin{cases} S = BR \cdot E_b \\ N = BW \cdot N_0 \end{cases}, \quad (2)$$

where *S*, respectively *N*, is the receiver input signal, respectively noise, power, E_b is the energy per bit, N_0 is the noise power density at the receiver input; in practice, $N_0 = k_B T \cdot F$ – where F is the receiver noise factor.

Given (2), the maximum bit-rate from can be written as, [2]:

$$BR \le BW \log_2\left(1+\frac{S}{N}\right) = BW \log_2\left(1+\frac{BR \cdot E_b}{BW \cdot N_0}\right) \quad (3)$$

From (3) results there is a minimum amount of signal energy required to transmit a bit:

$$E_b \ge N_0 \frac{2^{BR/BW}-1}{BR/BW} \quad (4)$$

As (4) shows, the minimum E_b only depends on N_0 and on the coding scheme, through the *BR*/*BW* ratio.

There are two extreme cases depending on the *BR*/*BW* ratio value.

Firstly, if *BR*/*BW* is very low (i. e., a large *BW* is used for a small *BR*) the limit from (4) is:

$$E_b \ge N_0 \ln 2 \quad (5)$$

This case is exploited by spread spectrum systems. Basically, the SNR_0 has a negative value for UMTS and WLAN 802-11 standards, as it accounts the processing gain, [21].

Secondly, for large *BR*/*BW* (e. g., for 64QAM), the limit from (4) becomes:

$$E_b \ge N_0 \frac{2^{BR/BW}}{BR/BW} \quad (6)$$

Hence, the SNR_0 in this case is:

$$SNR_0 = \frac{BR \cdot E_b}{BW \cdot N_0} \ge 2^{BR/BW} \quad (7)$$

As an example the SNR from (7) translates to 18 dB SNR_0 for 64QAM. Of course, this theoretical limit translates to a few dB higher value in practical implementation.

Based on the analysis presented in [22], the SNR_0 as a function of the *BER* has been determined for the basic modulation schemes. Table I notes the targeted standards signal modulation and the corresponding SNR_0 values.

The usage of the concept "SNR_0" facilitates the finding of the multi-standard receiver key electrical parameters by enabling a standard independent approach.

B. Sensitivity and Noise Figure

One of the most important parameters of a wireless receiver is its sensitivity, S_{RX}. The sensitivity is defined as the minimum input signal the receiver must be able to demodulate within the specified *BER*.

Thus, the Signal-to-Noise Ratio at the RX output, SNR_{out}, has to be above SNR_0. As each standard specifies a sensitivity level, given the useful signal RF bandwidth, BW_{RF}, the receiver NF, NF_{RX}, is calculated as:

$$NF_{RX} \le S_{RX} - 10\log BW_{RF} - SNR_0 - N_0, \quad (8)$$

where $N_0 = k_B T = -174$ dBm/Hz represents the noise power spectral density at the antenna output for T = 290 °K.

In practice, an overhead to SNR_0 should be considered in (8), since the overall receiver SNR is degraded by multiple factors, not only by noise (e. g., imperfect impedance matching, multipath channel).

The receiver NF specifications for all the wireless standards can be calculated with (8) by accounting the specified sensitivity levels from Table I.

A NF as the one derived by (8) can be obtained at the expense of larger power consumption of thy receiver.

In order to maximize the link budget, most commercially available dedicated receivers push their sensitivity level towards smaller and smaller values by decreasing NF_{RX}.

Hence, a true re-configurable multi-standard solution must embed a receiver with a small NF (typically < 3 dB) in order to be able to achieve a low enough sensitivity for all the targeted standards. Table I also comprises the required sensitivity levels, assuming NF_{RX} = 3 dB, for all the envisaged wireless standards.

C. Maximum gain requirements

In general, the receiver signal conditioning path gain is constraint by the received signal strength.

Any wireless receiver with an analog signal conditioning path embeds at least one variable gain block.

Thus, for each communication burst an Automated Gain Control loop (AGC) measures the Receiver Signal Strength Indicator (RSSI) and changes the receiver gain accordingly, in order to avoid the ADC overloading and to optimally load it.

The receiver maximum gain requirements are constraint by the ADC full scale level, FS_{ADC}, and the specified receiver sensitivity.

In order to optimally load the ADC, the receiver signal conditioning path maximum gain, G_{RX}, is given by:

$$G_{RX} = \frac{k \cdot FS_{ADC}}{S_{RX}}, \quad (9)$$

where $k < 1$ accounts the head room taken to avoid the ADC overloading.

TABLE III. THE MULTI-STANDARD RECEIVER MAXIMUM GAIN REQUIREMENTS

Wireless Standard		G_{RX} [dB]
GSM		115
UMTS		129
Bluetooth		100
DECT		103
WLAN IEEE 802.11 b,g (DSSS)	1 / 2 / 5.5 / 11 Mbit/s	110 / 108 / 97 / 95
WLAN IEEE 802.11 a,g (OFDM)	6 / 9 / 12 /18 24 /36 /48 /54 Mbit/s	101 / 100 / 98 / 96 93 / 89 / 85 / 84

For a multi-standard receiver embedding analog signal conditioning (see Fig. 1.c), k is set by the Variable Gain Amplifier (VGA) gain step (e. g., 6 dB, [14]). Equation (9) assumes all interferes and blockers have been totally filtered out before the ADC. This corresponds to the case of complete analog channel selection.

Table III presents the receiver signal conditioning path maximum gain requirement for all the envisaged standards calculated based on equation (9) for a 1 V FS ADC and for a receiver matched to 100 Ω with k = 0.9; the NF_{RX} of the receiver was assumed to be 3 dB. For direct sequence spread spectrum systems (e. g., WLAN 802.11b) the gain requirement is smaller, as in practice other signals will be present as well inside the received bandwidth.

Nonetheless, we can conclude, based on Table II data, that the low sensitivity levels of the targeted wireless standards require a large maximum gain for the multi-standard receiver.

IV. BLOCKERS AND INTERFERERS IMPACT ON THE MULTI-STANDARD RECEIVER CHARACTERISTICS

Besides the useful signal, other interferers and blockers can be present at the antenna input. The list comprising all interferes and blockers under which influence the receiver must still be able to properly demodulate the wanted signal represents the receiver blocker diagram. For each wireless standard such a receiver blocker diagram is specified.

Based on the envisaged wireless standards blocker diagram analysis, in [12] a receiver generic blockers diagram has been constructed. This newly introduced tool enables the designer to handle efficiently the large amount of information comprised in the targeted radio standards.

Thus, based on the receiver generic blockers diagram analysis it results immediately there are two major issues due to blockers and interferes:

- the receiver output clipping, due to the large receiver gain requirements and to the large difference between the useful signal and the blocker levels (i. e., typically > +40 dBc);
- intermodulation distortions that fall in-band, due to the receiver not perfectly linear transfer characteristic.

The receiver output clipping can be handled (i) by making the LNA and VGA blocks gain variable and (ii) by allowing the receiver high frequency part noise and linearity performance to adjust with the RF front-end gain. This has analysed in-depth in [23].

On the other hand intermodulation distortions are un-wanted products that potentially fall in-band and cannot be disseminated from the useful signal. Thus the wanted signal demodulation is affected due to the SNR degradation. Further on the analysis presented in this Section focuses on finding the values for the Figures of Merit (FOMs) used in evaluating the radio receiver linearity performance: the *IIP*2 and *IIP*3.

A. Finding the SDR IIP2

While receiving the RF input power may change significantly because of the reception of unwanted blockers/interferers. Due to the receiver even order

distortions, the received signal DC offset component will change. This *dynamic offset* effect upsets the received signal demodulation, especially if the envisaged modulation concentrates a large part of the symbol spectral power at low frequencies. This is the case for older standards like GSM, as the latest wireless standards use modulation schemes that do not carry information at low frequencies.

The figure of merit quantizing the analog front-end second order distortions is the second order intercept point, *IP*2. The SDRR input referred IP2, $IIP2_{\mathrm{RX}}$, is given by, [10]:

$$iIP2_{\mathrm{RX}} = 2 \times P_{blocker} - P_{in} + SNR_0 , \qquad (10)$$

where $P_{blocker}$ is the blocker level and P_{in} is the wanted signal level.

Based on the targeted standards analysis, it results the worst case scenario is met for the GSM standard that requires $IIP2_{\mathrm{RX}}$ = +46 dBm, [2].

B. Finding the SDR IIP3

For most wireless receivers, given the fully differential circuit implementation, the dominant non-linear contribution comes from the third order coefficient of power series expansion of their transfer characteristic. The maximum in-band level of the third-order intermodulation product, P_{IM3}, must be smaller than the useful RF signal level with SNR_0:

$$P_{IM3} \le P_{in} - SNR_0 \qquad (11)$$

In practice, a supplementary head room to SNR_0 should be considered, since the overall receiver SNR is degraded by multiple factors, not only by the down-converted spurs.

TABLE IV. MULTI-STANDARD RECEIVER IIP3 REQUIREMENTS

Standard	Intermodulation conditions	RX IIP3[dBm]	
		Eq.	*Value*
GSM	$P_{interferer}$ @ −49 dBm, P_{in} @ −99 dBm	(12)	−19
UMTS	$P_{interferer}$ @ −46 dBm, P_{in} @ −114 dBm	(12)	−21
Bluetooth	$P_{interferer}$ @ −39 dBm, P_{in} @ −64 dBm	(12)	−18.5
DECT	$P_{interferer}$ @ −47 dBm, P_{in} @ −80 dBm	(12)	−24
WLAN IEEE 802.11b,g (DSSS)	$P_{interferer}$ @ −35 dBm, P_{in} @ −70 dBm CCK – 11 Mbit/s	(12)	−12
W-LAN IEEE 802.11g (OFDM @ 2.4 GHz)	Interferer intermodulation: $P_{interferer}$ @ Sensitivity, P_{in} @ +32…+15 dBc (6…54 Mbit/s)	(12)	−32
	Blocker intermodulation: $P_{blocker}$ @ −10 dBm, P_{in} @ −42 dBm, BPSK – 6 Mbit/s	(12)	+8.5
	Sub-carrier intermodulation: P_{in} @ −20 dBm, N = 52 carriers, 64QAM – 54 Mbit/s	(15)	+10
W-LAN IEEE 802.11a (OFDM @ 5 GHz)	Sub-carrier intermodulation: P_{in} @ −30 dBm, N = 52 carriers, 64QAM – 54 Mbit/s	(15)	+5

Given (11), the receiver IIP3, $IIP3_{\mathrm{RX}}$, must meet the condition specified by the equation:

$$IIP3_{\mathrm{RX}} \ge P_{\mathrm{interferer}} + \frac{P_{\mathrm{interferer}} - P_{IM3}}{2} \qquad (12)$$

where $P_{\mathrm{interferer}}$ is the power per interferer of two interferers that cause the in-band third order distortion.

A special case is represented by OFDM Signals. An OFDM signal comprises frequency orthogonal sub-carriers, [19]. Receiver non-linearity leads to formation of bogus signals in-band due to sub-carrier intermodulation. The figure of merit in evaluating the third order intermodulation products thus formed is the Composite Triple Beat (CTB).

As is pointed out in [24] the worst case for the CTB products level is found in the centre band of the OFDM signal spectrum:

$$CTB[\mathrm{dB}] \le -2\left(IIP3_{\mathrm{RX}} - P_{in}\right) + 1.74 , \qquad (13)$$

where P_{in} is the OFDM signal power in all the carriers.

Hence, in order for the digital back-end to be able to still demodulate properly the wanted signal, the CTB level must be smaller than the useful RF signal level per carrier with SNR_0:

$$CTB \le P_{in} - 10\log N - SNR_0 , \qquad (14)$$

where N represents the number of OFDM sub-carriers.

In (14) SNR_0 represents the corresponding SNR headroom of the OFDM sub-carrier modulation.

Given (13) and (14), it results that in order to avoid destructive inter-carrier intermodulation, the $IIP3_{\mathrm{RX}}$ must meet the following condition:

$$IIP3_{\mathrm{RX}} \ge \frac{1}{2}\left(P_{in} + 10\log N + SNR_0 + 1.74\right) \qquad (15)$$

Each wireless standard specifies a set of particular intermodulation conditions. Table IV summarises the power per interferer of two interferers that cause the in-band distortion and the input signal power. By analysing all the targeted standards, the receiver *IIP*3 specifications were derived using (12) or (15) and noted in Table IV. The large variations in the *IIP*3 requirements are a reflection of the extreme reception conditions specific to the wireless environment. In [23] it is shown a versatile receiver is able to mitigate all presented scenarios, by adjusted dynamically its linearity and noise performance with the received power.

V. CONCLUSIONS AND FUTURE WORK

This paper conducted an analysis for finding the optimal architecture for a SDRR embedding analog signal conditioning and targeting compatibility with the major commercial wireless standards (see Table I).

Based on the analysis of the key receiver architectures, the homodyne receiver is found to suit best a monolithic implementation of a SDRR. By enhancing the classical homodyne architecture through the inclusion of an offset cancelation loop and quadrature LO generators the SDRR monolithic integration is made possible. The presented solutions are realized without introducing particular analog tricks to satisfy the needs of only one of the standards, as the SDRR must represent "universal receivers", and not be turned into "multi-standard ASICs".

Further on, the minimum SNR at the receiver output, SNR_0, required for a proper signal demodulation was calculated for all the envisaged standards. The usage of the concept "SNR_0" facilitates the finding of the multi-standard receiver key electrical parameters by enabling a standard independent approach.

Thanks to the standard independent systematic approach the presented analysis found the values for the key SDRR electrical specifications (i. e., NF_{RX}, $IIP2_{RX}$ and $IIP3_{RX}$) that ensure its compatibility with the envisaged standards.

Of course, a true SDRR has to be versatile and robust, such as it can adjust dynamically its performance (e. g., NF_{RX}, $IIP3_{RX}$) depending on the communication burst particularities. Nonetheless if a SDRR targets compatibility with the standards from Table I, it must meet the electrical specifications determined in this analysis.

So, the presented analysis constitutes the starting point in building the SDRR. Further on, the SDRR electrical specifications must be partitioned over its building blocks. The optimal specification partitioning must account the limitations due to the physical implementation (i. e., CMOS process) for each of the SDRR building blocks.

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REFERENCES

[1] S. Spiridon et. al., "Deriving the Key Electrical Specifications for a Multi-standard Radio Receiver," Proc. Of the First Intl. Conf. on Advances in Cognitive Radio COCORA 2011, April 2011, pp. 60-63.

[2] S. Spiridon, *Analysis and Design of Monolithic CMOS Sofware Defined Radio Receivers*, PhD Thesis, Ed. Tehnica, 2011.

[3] J Mitola, "Software radios – survey, critical evaluation and future directions," IEEE Nat. Telesystems Conf., 1992, pp. 13/15 – 13/23.

[4] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 2nd Ed., 2004, pp. 710-713.

[5] "ETS 300 577, GSM: Digital Cellular Telcommunications System (Phase 2); Radio Transmission and Reception," European Telecommunication Standard Institute (ETSI), 1997.

[6] "3GPP, Technical Specification 25.101, v.6.10.0," Third Generation Partnership Project, Dec. 2005.

[7] "IEEE Std 802.15.1™–2005," IEEE Computer Society, 2005

[8] "ETS 300 175, DECT: Digital Enhanced Cordless Telecommunications," European Telecommunication Standard Institute (ETSI), 1995.

[9] "IEEE Std 802.11g−2003," IEEE Computer Society, 2003.

[10] F. Op't Eynde, "Direct-Conversion Radio Transceivers," RF IC Design Course Slides, EPFL, Switzerland, October 2005.

[11] F. Op't Eynde, "Front-end circuit design for RF Transceivers, "Cellular and WLAN Transceivers: From Systems to Circuit Design," Short Course Slides, ISSCC 2011, February 2011.

[12] S. Spiridon, C. Dan, M. Bodea, "Filter partitioning optimum strategy in homodyne multi-standard radio receivers," Proc. of the 7th Conf. on Ph.D. Research in Microelectronics and Electronics, PRIME 2011, July 2011, pp.9-13.

[13] J. Craninckx et. al, "A Fully Reconfigurable Software-Defined Radio Transceiver in 0.13µm CMOS," *Digest of Technical Papers of the International Solid State Circuit Conference*, ISSCC 2007, pp. 346-347 and 607.

[14] V. Giannini et. al, "A 2mm^2 0.1-to-5GHz SDR Receiver in 45nm Digital CMOS," *Digest of Technical Papers of the International Solid State Circuit Conference*, ISSCC 2009, pp. 408-409.

[15] M. Ingels et. al, A 5mm^2 40nm LP CMOS 0.1-to-3GHz multistandard transceiver, *Digest of Technical Papers of the International Solid State Circuit Conference*, ISSCC 2010, pp. 458-459.

[16] S. Spiridon et. al., "Making Homodyne Receivers Ready for Monolithic Integration in Multi-Standard Wireless Transceivers," Annals of Academy of Romanian Scientist, Series on Science and Technology of Information, Vol. 3, No. 2, pp. 73-80, 2010.

[17] S. Spiridon and F. Op't Eynde, "Low power CMOS fully differential variable-gain amplifier," in Proc. of the Annual Intl. Semiconductor Conf. CAS 2005, October 2005, vol. 2, pp 383-386.

[18] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2000.

[19] A. Danchiv, M. Bodea, C. Dan, "Amplifiers Chopper Technique Effects on Noise Performances," Proc. 10th Intl. Conf. on Optimization Of Electrical And Electronic Equipment OPTIM 2006, May 2006, pp. 16-20.

[20] S. Spiridon, F. Agavriloaie, M. Serban, "High Frequency Programmable Wide-Band Frequency Divider Design for CMOS Software Defined Radio Transceivers," Proc. of the 30th Annual Intl. Semiconductor Conf., CAS 2007, October 2007, Vol. 2, pp. 451-454.

[21] A. J. Viterbi, *CDMA: Principles of Spread Spectrum Communication*, Addison-Wesley, 1995.

[22] A. Tarniceriu, B. Iordache, and S. Spiridon, "An Analysis on Digital Modulation Techniques for Software Defined Radio Applications," Proc. of the 30th Annual Intl. Semiconductor Conf. CAS 2007, October 2007, vol. 2, pp. 571-574.

[23] S. Spiridon et. al, "Smart gain partitioning for noise – linearity trade-off optimization in multi-standard radio receivers," *Proceedings of the 18th International Conference Mixed Design of Integrated Circuits and Systems*, MIXDES 2011, June 2011, pp. 466-469.

[24] The Relationship Of Intercept Points Composite Distortions And Noise Power Ratios, http://www.matrixtest.com/literat/mtn109.pdf, Matrix Technical Notes, October 2005