DS-CDMA receiver in Software Defined Radio technology

Admission to the implementation of a RAKE receiver

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Abstract — Programmable radio is one of the latest trends in the construction of multi-standard receivers. The technology, called Software Defined Radio (SDR), is also an ideal test platform that allows to try out different algorithms of signal receiving. This particular feature led to choose this platform to implement a DS-CDMA receiver (Direct Sequence Code Division Multiple Access). The use of SDR allows for a gradual upgrade of data processing algorithms in terms of correctness of the received signal and, what is equally important, its processing time. This paper mainly focuses on these two aspects. Subsequently, the plans are submitted for further development of the software receiver.

Keywords - Software Defined Radio; SDR; RAKE; DS-CDMA; phase correction

I. INTRODUCTION

The variety of standards for radio systems make it necessary to construct a mobile terminal that has the technical possibilities of cooperation with different radio standards. This simple concept created an idea of a programmable radio called Software Defined Radio, based on a universal hardware layer, with only a layer of software determining its functionality [1-5].

Based on these assumptions a programmable receiver has been developed for DS-CDMA signals. It consists of a wideband receiver and a personal computer (PC) equipped with a acquisition card. PC with appropriate software is used to control both the receiver and the acquisition card; also it serves for signal processing.

In this article, a basic concept of SDR will be presented; also basics of the RAKE receiver and the purpose of the WMSA filter will be introduced. Next, the physical implementation of DS-CDMA signal receiver and its structure will be shown. Selected parameters of received signal and encountered problems with data processing (initial phase correction, frequency jitter, processing time) will be presented as well.

Finally, the direction of expansion of the programming layer multipath signal reception (RAKE receiver) will be presented.

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II. SOFTWARE DEFINED RADIO

As was mentioned, the concept behind Software Defined Radio is to implement – to the greatest possible extent – signal processing blocks of a radio transceiver in software rather than in dedicated hardware. The differences between the classic "analogue" version of a receiver and the programmable one are illustrated, respectively, in Figures 1 and 2 [1], [2].

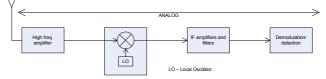


Figure 1. Block diagram of analogue receiver

Receiver shown in Figure 2 can be divided into two different parts of a system:

• hardware (analogue radio) in the form of a set of classic radio components,

• software (digital), whose main element is fast signal processor DSP (Digital Signal Processor).

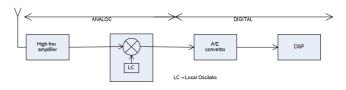


Figure 2. Block diagram of Software Defined Radio

Conceptually speaking, a SDR should have the following properties [4]:

- reconfigurable RX/TX architecture, controlled by software,
- most part of the radio functionality performed by software,

 system specification (bandwidth, bit rate, demodulation) can be updated whenever needed to do so.

The task of the analogue radio part is to strengthen appropriately and convert the received radio signal from the high-band radio frequency to lower frequency band. Then, in this band with a fast A/D converter (Analogue to Digital Converter) a received analogue signal is converted into its digital form. Processing is performed in a properly programmed digital signal processor.

In short, we will find that having a broadband receiver and analogue-to-digital high-frequency sampling with high dynamics, we can get a very comprehensive platform of the receiver, which can perform demodulation/detection of any signal only through the change of software.

III. THEORY OF A RAKE RECEIVER

The mobile radio communication systems, radio wave radiating from the transmitter to the receiver, encounter many obstacles on its way, which means that the signal reaches the receiver in many routes and many random time delays. DS-CDMA receiver is called in the literature as a RAKE receiver. It gives the opportunity of receiving signals in a multi-way propagation environment. In the presented method, due to the use of a spreading sequences and their good correlation properties, the receiver can extract the signal transmitted in several propagation multipath. Therefore the phenomenon of multipath can be used to improve the quality of the received signal.

Technique of direct spread spectrum DS-CDMA creates new opportunities for receiving such signals. If the maximum delay difference between different paths is larger than the duration of one chip, then the temporary reception will allow almost independent reception of each signal. Thanks to this property, the phenomenon of multipath can be used to improve the quality of the received signal.

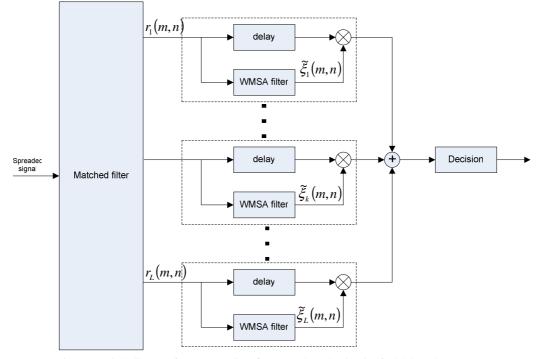


Figure 3. Block diagram of a RAKE receiver ($\xi_L(m,n)$ – channel estimation for l-th branch)

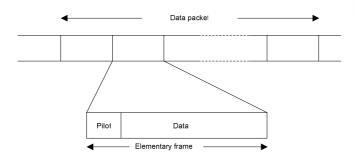
A. Receiver

Analysing the block diagram shown in Figure 3 we can conclude that the RAKE receiver is a set of correlation receivers, acting in parallel. In each branch signal is correlated with the spreading sequence delayed by the same time as the delay introduced by the different signal propagation paths. The signal after phase correction is sent to the decision-making system. Next, the results of decision are gathered in the system of accumulating the results of decisions in order to give them logical values: zero or one. The RAKE receiver is so named because it reminds the function of a garden rake: each branch collects symbol energy like tines of a rake collect leaves.

As known, multipath fading depends on the speed of a terminal [7]. With the increasing speed phase shift estimation is more difficult to estimate [6], [7]. Therefore a chosen method should estimate the phase shift for both slow and rapid fading of the signal. Popular technique filters are operating on linear interpolation, the Gaussian interpolation [8], [9] or Wiener filters [10], [11]. However, Wiener filters require information about the statistical properties of the

existing fading, which in practice is almost impossible. WMSA filter (*Weighted Multi-Slot Averaging*), presented in this paper, is based on the weight variables whose values are linearly interpolated basing on data derived from sequentially received elementary frames.

A simulation model was developed prior to the implementation of a receiver. This method was selected due to its potential low computational complexity which translates to speed of the program. A structure of transferred data, illustrated in Figure 4, was applied for the purpose of simulation. Frame containing the data begins with a known sequence of N_P pilot bits, followed by N_D data bits.

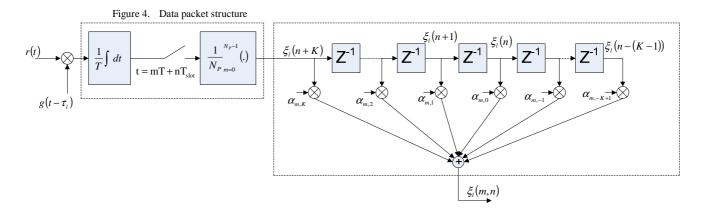


B. WMSA filter

WMSA filter is based on the weight coefficients of the variables. Block diagram of WMSA filter is shown in Figure 5 [6], [7]. In comparison with linear interpolation filters, *the Gaussian* interpolation filters or Wiener filters, the WMSA filter allows better tracking of fading.

Due to the elimination of fading, the weight factors are changed from frame to frame. This eliminates the problem of proper tracking of the channel fading.

Sets of coefficients have been designated, basing on the simulation results presented in [7]. These factors have been optimized to measure frames and are independent of the position of the symbol. Based on these results, two sets of factors have been appointed. These sets are presented in [6]. The first set of designated factors is referred to as Type I and the second one as Type II. They differ only in the number of branches (respectively six and four).



 $\begin{array}{l} \mbox{Figure 5.} & \mbox{Block diagram of WMSA filter (m-received symbol, n-no of frame, T-time of a symbol, T_{slot}-time of elementary frame T_{slot}=(N_{P}+N_{D})T, N_{P}-number of pilot bits, N_{D}-number of data bits, $r(t)$-received signal, $g(t)$-spreading sequence, τ_{l}-l chips delay, $\xi_{l}(n)$-channel estimation, n-th frame, $l-th path, Z^{-1}-l frame delay block, $\alpha_{m,K}$-changing weighting factors, $\xi_{l}(m,n)$-channel estimation for l-th branch) } \end{array}$

C. Simulation results

As a master thesis both of WMSA filters were tested in a simulation environment [12]. The presented results refer to the following signal parameters:

- transmission speed 8kb/s,
- terminal speed 3km/h,
- propagation model Outdoor to Indoor & Pedestrian (according to ITU-R M 1034 recommendation),
- channel model with Rayleigh's fading
- Sample results are shown in Figure 6.

Based on the simulations, several important conclusions can be extended [12]. Due to use of WMSA filters, lower ratio of of E_b/N_o is required to keep the same rate of errors. Estimator used in the receiver phase (WMSA) will improve from 1 to 3 dB (the ratio is less than the required E_b/N_o at the same error rate). WMSA filters Type I and Type II differ only in the number of branches. After comparing filter Type I (six branches) with filter Type II (four branches), an improvement of 0,1-0,4 dB is obtained. This is a small difference, and from a practical point of view it can be assumed that the filter Type II is computationally more efficient due to the smaller number of arms and thus a smaller number of operations to be performed.

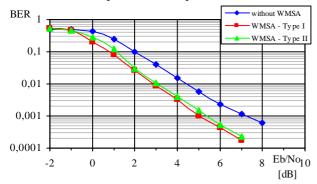


Figure 6. Results of simulation (speed of a receiver 3km/h, transmission speed 8kb/s)

IV. HARDWARE IMPLEMENTATION

Figure 7 shows the diagram of the receiver made in software defined radio technology.

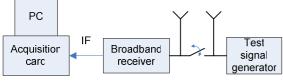


Figure 7. Block diagram of programmable receiver

It consists of a broadband receiver and a PC fitted with a data acquisition card (Figure 8), whereby the analogue radio signal is converted into a sequence of discrete data samples. Computer task is to control the operation of the receiver (the

choice of frequency, width filters, etc.) and to process data received from data acquisition card.

- Actual received signal parameters are as follows:
- The signal carrier frequency: 450MHz,
- Data rate: 1kHz,
- Bandwidth after spreading: 1MHz,
- Modulation: QPSK,
- In accordance with the structure of the frame (Figure 5): $N_P = 13$, $N_D = 26$,

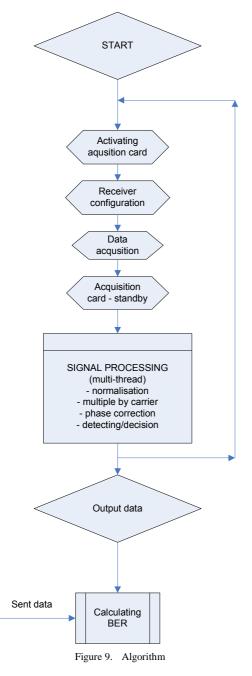
- Inphase and quadrature components carry independent data



Figure 8. Acquisition card

A. Algorithm

The basic algorithm of operation is shown on Figure 9. The program begins with launching and configuring the data acquisition card and setting the parameters of the receiver. Then, the process of acquisition (writing to a binary file data samples) begins. After a certain time, acquisition is completed and acquisition card goes into standby mode. The next step is to process the collected samples. The values of the samples are in the range from 0 to 65536 (16 bit resolution) and they are changed into the range from - 32768 to 32768. Then, the data are divided by the maximum value of level in order to normalize the data (after this, samples are in the range from -1 to +1). Next, samples are multiplied by carrier (both the cosine and sine) and by the spreading sequences. The correlation function, obtained in this way, allows to determine the actual value of the Realis component (Re) and Imaginary component (Im). A correction phase is being fixed on their basis. When receiving a bit, sequence is compared with the sent sequence, and on this basis bit error rate (BER) is calculated.



B. Frequency jitter

During the processing of data, we should consider errors resulting from inaccuracies in the internal clocks of the receiver and data acquisition card. Correction is being determined after receiving a few bits; next, it is added in the following stage of detection. This frequency drift and phase error can be illustrated as the constellation of the received signal. Due to the independent component in inphase and quadrature, received signal can be detected as two BPSK modulation. Bearing in mind the above, received signal constellation may take the form shown in Figure 10. Bellow the following sequence of bits has been given for illustration:

bit no.	1	2	3	4	5	6	7
sequence	1	1	1	1	1	0	0
bit no.	8	9	10	11	12	13	14
sequence	1	1	0				
bit no.	15	16	17	18	19		
sequence		0	1	1	0		

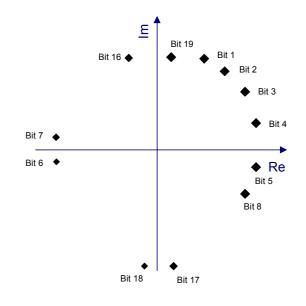


Figure 10. BPSK constellation of a received signal

Analyzing the presented sequence with constellation shown in Figure 10 it can be seen that bits 18 and 19 without phase correction have opposite values. After applying the correction phase (Figure 11), both points are on the side of their actual representation.

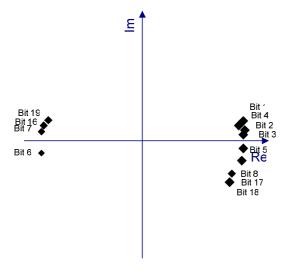


Figure 11. BPSK constellation after phase correction

In the first approach of implementation the phase is calculated on the basis of receiving the first few bits of a known pilot. Currently, tests are conducted on receipt of a number of generators at the same time (using different spreading sequences).

C. Processing time

Time of signal processing is one of the most important parameters of a programmable radio. It is recommended to obtain the strongest possible CPU for a PC. If possible, convert each calculating subprogram to the application, using several processor cores. Only the development of multithreaded applications can effectively cope with the complexity of computing with which we meet in implementing a programmable radio. Not only the hardware layer affects the processing speed, it is equally important to optimize the code.

The first attempts to receive transmitted signal took over an hour of processing time (for the acquisition of 40 seconds). At the moment, the software was significantly enhanced (algorithm were optimized, multithread environment was implemented). These treatments resulted in reducing the processing time to approximately 40-60 seconds.

V. CONCLUSION AND FUTURE WORK

Application of the DS-CDMA signal receiver in programmable radio technology allows a flexible approach to updating and verification of the implemented software receiver. It also allows to implement several methods of reception in order to compare their efficiency, correctness and processing time. Preliminary studies conducted in the lab confirms the versatility of the platform.

The next step will be implementation of RAKE receiver algorithms (multipath reception). In this case, properties of WMSA filters may be required for proper signal detection. The results are going to be compared with simulations presented in this article.

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