Performance Characterization of TAS-MRAM Architectures in Presence of Capacitive Defects

João Azevedo, Arnaud Virazel, Yuenqing Cheng,
Alberto Bosio, Lugi Dilillo, Patrick Girard, Aida Todri
LIRMM – University of Montpellier 2 / CNRS
Montpellier, France
e-mail: {azevedo, Virazel, cheng, bosio, dilillo, girard, todri}@lirmm.fr

Jérémy Alvarez-Hérault
CROCUS Technology
Grenoble, France
e-mail: jherault@crocus-technology.com

Abstract—**Magnetic Random Access Memory (MRAM) is an emerging memory technology. Among existing MRAM technologies, Thermally Assisted Switching (TAS) MRAM technology offers several advantages such as selectivity, single magnetic field and high integration density. In this paper, we analyze the impact of capacitive defects on the TAS-MRAM performance. Electrical simulations were performed on a 16-words TAS-MRAM architecture enabling any sequences of read/write operations. Results show that writing operations may be affected by these defects. Especially, we demonstrate that some capacitive defects may have a local (single cell) impact on the functionality of TAS-MRAM while others, even if there is an effective coupling, do not change the functional operation. These results will be further used to develop effective test algorithms targeting faults related to actual defects that may affect TAS-MRAM architecture.**

Keywords–non-volatile memories; spintronics; TAS-MRAM; capacitive defects; fault modeling; test.

I. INTRODUCTION

Nowadays, Non-Volatile Memories (NVMs) are more and more integrated in consumer applications. Though widely used, Flash memories still have several drawbacks such as high supply voltage requirement, low speed and susceptibility to reliability issues due to high electric field for programming operations. On the other hand, Magnetic Random Access Memory (MRAM) is an emerging technology with high data processing speed, low power consumption and high integration density compared with Flash memories. Moreover, this memory technology is non-volatile with fair processing speed and reasonable power consumption when compared to Static RAMs (SRAMs). MRAM probably is the closest to an ideal "universal memory" and thus may be used as NVM as well as SRAM and DRAM according to the 2011 International Technology Roadmap for Semiconductors (ITRS) [1].

MRAMs have the potential to mitigate almost all Flash related issues but they are prone to defects as any other kind of memory. Only few papers on MRAM testing can be found in the literature, and target mainly Field Induced Magnetic Switching (FIMS) MRAM technologies. Su et al. [2] present the Write Disturbance Fault (WDF) model, a fault that affects data stored in Toggle MRAM cells due to the amount of magnetic field applied during write operations on neighboring cells. Su et al. [3] identified two new faults related to the magnetic junction behavior and called Multi-Victim Fault (MVF), in which a cluster of cells can easily change their magnetization state due to process variations, and Kink Fault

(KF), in which the hysteresis loop shrinks because of its relation with cell shape, thus changing MTJ resistivity.

A thorough investigation and deep analysis must be done for testing MRAMs memories. In [4] and [5], resistive-open and resistive-bridge defect analyses are presented for TAS-MRAM architectures. These studies have revealed the importance of electrical analyses of defects that may impact the performance of TAS-MRAMs.

In this paper, we complete these studies by considering parasitic coupling, i.e., capacitive defects. Parasitic coupling between adjacent interconnect lines is a major limiting factor in deep-submicron ICs due to the injection of noise from switching lines to neighboring lines [6]. The trend of increasing the integration level of ICs has a negative impact on interconnect performance. The cross section is smaller in the scaling-down process increasing the line's resistance. In order to reduce resistance while maintaining high horizontal interconnect density, the aspect ratio is larger than "1" increasing the coupling capacitance. In addition, the effective capacitance increases as the spacing between lines decreases, which causes an increase in the delay related to the RC constant. Moreover, crosstalk between lines due to mutual capacitance and inductance becomes worse.

In this context, we fully characterize the impact of capacitive defects on the TAS-MRAM performance. Considered defects were selected based on the layout structure of the TAS-MRAM array. Simulations were performed in a TAS-MRAM architecture supporting any read/write sequences. Results show that capacitive defects have almost no impact on read operations. Conversely, write operations are affected by capacitive defects depending on the size and location. Such results will be helpful to define an efficient test algorithm to fully test TAS-MRAMs.

The rest of the paper is organized as follows. Section II provides the fundamentals and background on MRAM technologies. The proposed TAS-MRAM architecture is described in Section III. The capacitive defect analysis is provided in Section IV. Section V concludes the paper.

II. MRAM TECHNOLOGIES

MRAMs are Spintronic devices that store data in Magnetic Tunnel Junctions (MTJs). A basic MTJ device is usually composed of two FerroMagnetic (FM) layers separated by an insulating layer, as shown in Figure 1. One of the FM layers is pinned and acts as a reference layer. The other one is free and can be switched between, at least, two stable states. These

states are parallel or anti-parallel with respect to the reference layer. When the MTJ is in the parallel state, it offers the minimum resistance (*Rmin*) while the maximum resistance (*Rmax*) is obtained when anti-parallel. The difference between *Rmin* and *Rmax*, quantified by the Tunnel Magneto Resistance (TMR), is high enough to be sensed during the read operation.
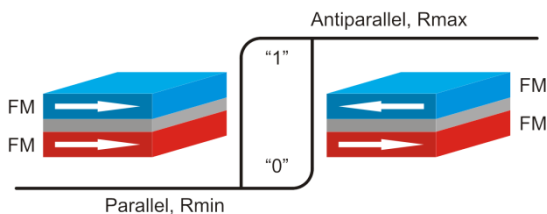

Figure 1. MTJ in parallel and antiparallel states

A read operation consists in determining the MTJ's magnetization state and can be performed by voltage or current sensing across the MTJ stack. A CMOS sense amplifier is used to retrieve the stored bit information. High TMR allows simple and stable sense amplifiers, improving reading accuracy [7].

Magnetization dynamics describes how the magnetization goes from one point of equilibrium to another one. This evolution of the magnetization in terms of time and space under a local effective field can be described by the Landau-Lifshitz-Gilbert equation (1):

$$\frac{\partial \vec{m}}{\partial t} = -\frac{\gamma}{1+\alpha^2}\vec{m}\times\overrightarrow{H_{eff}} - \frac{\gamma\alpha}{1+\alpha^2}\vec{m}\times\left(\vec{m}\times\overrightarrow{H_{eff}}\right) \qquad (1)$$

where $\vec{m}$ is the unit vector along the magnetization of the free layer, γ is the gyromagnetic ratio, α is the Gilbert damping constant and H_{eff} is the effective magnetic field.

A write operation can be performed using magnetic fields or spin polarized current and depends on MRAM technologies: FIMS (Field Induced Magnetic Switching), Toggle Switching, TAS (Thermally Assisted Switching) and CIMS (Current Induced Magnetic Switching).

Thermally Assisted Switching^{TM} is an alternative switching method for MRAMs. In the scheme proposed by Spintec [8] and industrialized by Crocus Technology, the MTJ is modified by inserting an Anti-FerroMagnetic (AFM) layer that pins the storage layer while below its blocking temperature (T_B) that can be calculated by (2).

$$T_B = \frac{KV}{k_B \ln\left(\tau_0 e^{\left(\frac{KV}{k_B T}\right)}\right)} \qquad (2)$$

where K is the effective anisotropy constant, V is the device volume, k_B is the Boltzmann constant and τ_0 is the attempt time.

In AFM materials, the magnetic moments of atoms are aligned in a regular pattern, neighboring spins pointing in opposite directions. This organization vanishes above T_B and the material becomes paramagnetic. When MTJ's temperature rises above T_B, the storage layer is freed and can be reversed

under the application of a small magnetic field provided by a single field-line. The magnetic field is maintained beyond the heating voltage pulse to ensure the correct pinning of the storage layer.

TAS approach offers several advantages compared to predecessors MRAM technologies. The selectivity problem is reduced since only heated MTJs are able to switch and all other MTJs hold their stable state as they remain below their blocking temperature. Although TAS-MRAM needs an additional heating current, this current is much smaller than the current used to generate the second magnetic field in FIMS-MRAM technology. The integration density is improved due to thermal stability and the need of only one field-line. Finally, as the free layer can be pinned to any stable state, multi level logic can be achieved [9]. TAS-MRAM is for the moment the most promising MRAM solution as it mitigates most drawbacks from its predecessors.

III. TAS-MRAM ARCHITECTURE

Figure 2 shows the TAS-MRAM architecture we have developed for our study. The organization is done in a square matrix that has 2^{MR} rows and 2^{NC} columns, for a total storage capacity of 2^{MR+NC} bits per page, where MR and NC are the numbers of bits used to specify the row and column address, respectively. In our case study, MR and NC are equal to 2 and the number of pages is 4; hence, the storage capacity is 64 bits (16 words of 4 bits). Each cell in the array is connected to one of the row-lines, called word-lines, and connected to one of the column-lines, called bit-lines. A particular set of MTJs can be accessed for a read or write operation by selecting its word-line and bit-line. There is only one field-line that connects all MTJs serially row by row passing through all pages in this architecture.

During a read operation, the read driver applies a small voltage that generates negligible heat to both the selected MTJ and a reference MTJ. The reference MTJ is halfway between the high and low resistance values. The resistance difference is then sensed to determine the stored data in the selected MTJ.

A write operation is performed as follows:

- Initially, the write driver applies a voltage to heat the selected MTJ above its T_B (about 150 °C).

- Next, the field-line driver applies a current to generate the data zero magnetic field. While the MTJ is cooled down below T_B, the magnetic field is maintained.

- Then, the field-line driver inverses the current direction and the MTJ is heated again to perform the write 1 operation, if needed. When the MTJ reaches room temperature, the writing procedure is accomplished.

This approach allows writing "logic 0" and "logic 1" in one cycle to different MTJs sharing the same field-line. Note that, a Write 1 operation (denoted W1) consists of applying both field-line current polarities (magnetic field for "data 0" and then magnetic field for "data 1"), while a Write 0 operation (denoted W0) consists of applying only one field-line current polarity (magnetic field for "data 0" only). These writing procedures are inspired by Flash programming procedures

where a write operation (write 1) is always preceded by an erase operation (write 0).
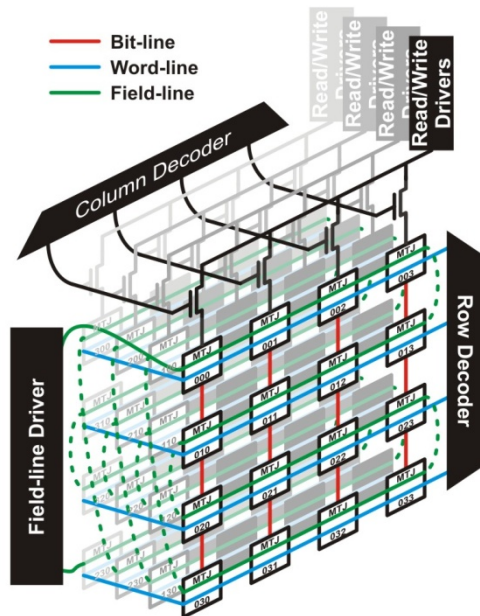

Figure 2.   TAS-MRAM architecture

Electrical simulations were performed using the TAS-MTJ model developed by Spintec [9]. This model is based on the physical equations of the MTJ and is calibrated with respect to the targeted TAS-MRAM technology. Moreover, this model is compiled in C language and is compatible with the Spectre simulator of the standard Cadence design suite [10].

Table I summarizes simulated fault-free characteristics of $MTJ_{1,1,1}$ ($MTJ_{i,j,k}$ with i ⇒ page number, j ⇒ row number and k ⇒ column number) in the second page, second column and second line of the TAS-MRAM architecture shown in Figure 2. The first column gives the four possible operations R0, R1, W0 and W1. The next five columns provide all the MTJ's parameters:

- **V** – Voltage level at the MTJ interface.
- **I** – Current passing through the MTJ during read or write operations.
- **R** – Resistance of the MTJ.
- **T** – Temperature of the MTJ during operations.
- **M** – Magnetization state that is related to the angle between the two ferromagnetic layers. The parallel magnetization state is represented ideally by "1 ⇒ logic 0" and the anti-parallel magnetization state by "-1 ⇒ logic 1". The magnetization state is correlated to the resistivity of the MTJ.

Finally, the last column gives the sensing voltage (S) during read operation only. The two resistive states of the MTJ are 1.48kΩ for *Rmin* and 2.80kΩ for *Rmax* during read operation. In normal operation the sensing voltage (S) is around 165mV for *Rmin* and 254mV for *Rmax*. During write operations, the current that passes through the MTJ is high enough to heat its temperature above the blocking temperature, i.e., 193°C for

W0 and 193/183°C for W1. The MTJ's resistivity is different during read and write operations even if the magnetization state is the same. This is due to the voltage applied to the MTJ as well as its operating temperature.

TABLE I. $MTJ_{1,1,1}$ CHARACTERISTICS UNDER READ/WRITE OPERATIONS

Operation	MTJ$_{1,1,1}$ parameters					S (mV)
	V (mV)	I (uA)	R (kΩ)	T (°C)	M	
R0	111.49	74.89	1.48	31.16	1	165.67
R1	202.35	72.11	2.80	34.26	-1	254.49
W0	745.32	606.59	1.22	193.18	1	n.a.
W1	745.32 863.09	606.59 542.63	1.22 1.59	193.18 183.75	-1	n.a.

Figures 3 and 4 show temperature profiles for W0 and W1 operations performed on a 16-bit fault-free TAS-MRAM memory page, respectively. Note that, MTJs are written row by row from $MTJ_{x,0,0}$ to $MTJ_{x,3,3}$. We observe that temperature rises twice during each write cycle in W1 operations and rises only once per cycle in W0 operations. This behavior is expected according to the writing scheme previously described.
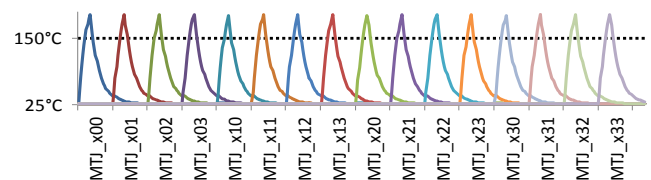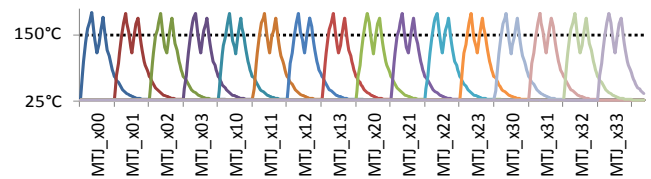

Figure 3.   16-bit W0 fault-free temperature profiles

Figure 4.   16 bits W1 fault-free temperature profiles

IV.   CAPACITIVE DEFECT INJECTION

The capacitive defect injection in TAS-MRAM architecture is depicted in Figure 5. Capacitive defects are inserted between interconnect lines based on the TAS-MRAM array layout as follows:

- **C1:** MTJ's bottom metal – Field-line
- **C2:** Field-line – Word-line
- **C3:** Word-line – Word-line
- **C4:** Word-line – MTJ's bottom metal

Note that all resistive parameters are not represented in Figure 5 but are all taken into account in models (lines, transistors, drivers) used for electrical simulations.

TAS-MRAM performance is affected by these capacitive defects in several ways. In the following sub-sections, we show a complete analysis of how these four capacitive defects impact the TAS-MRAM performance. Simulations were performed using the following write sequences:

- 0W0: W0 operation performed on a MTJ that initially contains "logic 0". There is no transition in this sequence.
- 1W0: W0 operation performed on a MTJ that initially contains "logic 1". This sequence corresponds to a falling transition.
- 0W1: W1 operation performed on a MTJ that initially contains "logic 0". This sequence corresponds to a rising transition.
- 1W1: W1 operation performed on a MTJ that initially contains "logic 1". This sequence allows verifying the W1 operation since it applies both field-line current polarities.
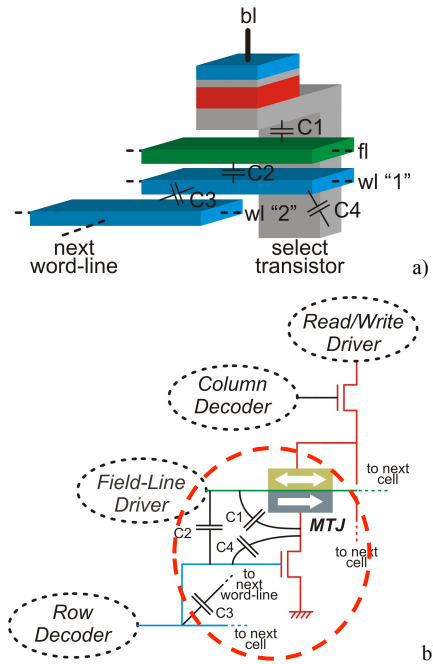

Figure 5. Capacitive defects injection
a) layout extraction and b) electrical modeling

For each capacitive defect, the capacitance range varies from the typical value to 10x the typical value. Larger capacitance sizes are unrealistic from process variations point of view. In those cases, other defect types, such as bridging defects, may appear.

A. MTJ bottom – Field-line (C1)

The current that passes through the MTJ is responsible for heating the device above its blocking temperature during write operations. This current is also important to retrieve the MTJ's logic state during read operations.

Tables II and III summarize the simulated characteristics of $MTJ_{1,1,1}$ and $MTJ_{1,1,x}$ in the presence of a capacitive defect located between bottom metal of $MTJ_{1,1,1}$ and field-line labeled as C1. Gray lines represent typical C1 capacitance size. From these data, we observe that only MTJs sharing the same bit-line are barely affected by this defect when the defect size is up to 1fF. Consequently, there is no observed faulty behaviors for the considered defect range, i.e., from typical value to 10x the typical value.

TABLE II. $MTJ_{1,1,1}$ CHARACTERISTICS UNDER WRITE OPERATIONS

Operation	C1 (fF)	V (mV)	I (uA)	R (kΩ)	T (°C)	M
0W0	0.10	746.38	605.99	1.23	191.52	1
	1.00	746.36	605.91	1.23	191.58	1
1W0	0.10	744.68	606.92	1.22	194.09	1
	1.00	744.63	606.85	1.22	194.18	1
0W1	0.10	746.37 / 863.96	606.00 / 542.15	1.23 / 1.59	191.52 / 182.55	-1
	1.00	746.35 / 863.87	605.92 / 542.12	1.23 / 1.59	191.58 / 182.54	-1
1W1	0.10	744.64 / 862.99	606.93 / 542.66	1.23 / 1.59	194.11 / 183.93	-1
	1.00	744.66 / 862.99	606.85 / 542.54	1.23 / 1.59	194.18 / 183.99	-1

TABLE III. $MTJ_{1,1,x}$ CHARACTERISTICS UNDER WRITE OPERATIONS

Operation	C1 (fF)	V (mV)	I (uA)	R (kΩ)	T (°C)	M
0W0	0.10	746.45	606.00	1.23	191.45	1
	1.00	747.09	605.96	1.23	190.83	1
1W0	0.10	744.70	606.94	1.22	194.07	1
	1.00	745.24	606.96	1.22	193.68	1
0W1	0.10	746.44 / 864.01	606.00 / 542.10	1.23 / 1.59	191.45 / 182.33	-1
	1.00	747.12 / 864.43	605.95 / 540.93	1.23 / 1.59	190.79 / 179.95	-1
1W1	0.10	744.68 / 863.22	606.96 / 542.57	1.23 / 1.59	194.06 / 183.67	-1
	1.00	745.35 / 864.94	607.04 / 541.95	1.23 / 1.59	193.64 / 181.54	-1

In Figure 6, we show temperature profiles for W1 operations performed in one memory page under C1=1fF barely affecting the MTJs sharing the same bit-line ($MTJ_{1,0,1}$, $MTJ_{1,2,1}$ and $MTJ_{1,3,1}$). Note that MTJs are written row by row from $MTJ_{1,0,0}$ to $MTJ_{1,3,3}$. In addition, a non-catastrophic coupling effect is observed between $MTJ_{1,1,1}$ and $MTJ_{1,0,1}$, $MTJ_{1,2,1}$ and $MTJ_{1,3,1}$.
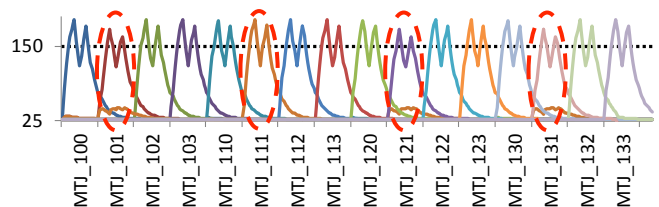

Figure 6. 16 bits W1 under capacitive defect (C1=1fF) temperature profile

B. Field-line – Word-line (C2)

Tables IV and V summarize the simulated characteristics of $MTJ_{x,1,0}$ and $MTJ_{x,2,0}$ under a capacitive defect located between field-line and word-line "1" labeled as C2. Simulations were performed using write sequences previously described.

In Figure 7, we show temperature profiles for W1 operation performed in one memory page under C2=10fF. This defect adds an extra delay when selecting/deselecting the affected word-line. If the defective word-line is half-selected, then operations performed on an MTJ on this word-line may be corrupted. Secondly, if the defective word-line remains partially selected when operations are applied elsewhere in the

TAS-MRAM array, then operations performed on a non-defective word-line may also be corrupted.

TABLE IV. MTJ$_{x,1,0}$ CHARACTERISTICS UNDER WRITE OPERATIONS

Operation	C2 (fF)	V (mV)	I (uA)	R (kΩ)	T (°C)	M
0W0	1.00	748.67	604.77	1.23	188.12	1
	10.00	769.01	572.79	1.23	128.30	1
1W0	1.00	746.68	605.83	1.22	191.28	1
	10.00	880.12	516.44	**1.70**	137.35	**-1**
0W1	1.00	748.67	604.77	1.23	188.12	-1
		864.50	541.85	1.59	181.52	
	10.00	769.01	572.79	1.23	128.30	-1
		767.92	593.69	1.59	163.63	
1W1	1.00	746.64	605.86	1.23	191.29	-1
		863.49	542.41	1.59	183.18	
	10.00	880.12	516.44	1.23	137.35	-1
		872.92	536.88	1.59	168.87	

TABLE V. MTJ$_{x,2,0}$ CHARACTERISTICS UNDER WRITE OPERATIONS

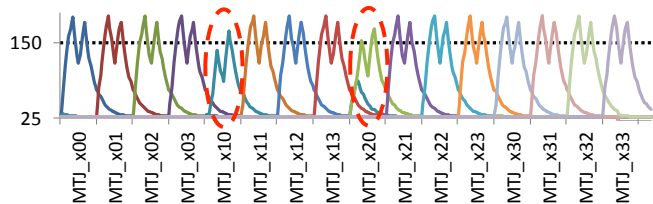| Operation	C2 (fF)	V (mV)	I (uA)	R (kΩ)	T (°C)	M
0W0	1.00	749.26	604.46	1.23	187.23	1
	10.00	773.40	589.91	1.23	147.24	1
1W0	1.00	747.62	605.36	1.22	189.79	1
	10.00	882.29	530.52	**1.70**	152,90	**-1**
0W1	1.00	748.90	604.63	1.23	187.77	-1
		864.58	541.82	1.59	181.42	
	10.00	769.79	591.87	1.23	153.26	-1
		867.45	541.63	1.59	171.08	
1W1	1.00	747.32	605.50	1.23	190.30	-1
		863.68	542.28	1.59	182.89	
	10.00	882.29	530.51	1.23	152.90	-1
		870.03	538.82	1.59	173.52	

Figure 7. 16 bits W1 under capacitive defect (C2=10fF) temperature profile

The selection of word-line "1" is delayed in the presence of C2 as can be seen in the operation performed on MTJ$_{x,1,0}$. Next three operations performed on MTJ$_{x,1,1}$, MTJ$_{x,1,2}$ and MTJ$_{x,1,3}$ that share same word-line work properly as word-line "1" is fully selected. The operation performed on MTJ$_{x,2,0}$ has an undesired behavior as C2 delays the word-line "1" de-selection. Regardless defective word-line selection or de-selection only *1W0* sequence is not correctly performed. Such faulty behavior is modeled by a TF0 (Transition Fault 1 to 0).

C. Word-line – Word-line (C3)

Tables VI and VII summarize the simulated characteristics of MTJ$_{x,1,0}$ and MTJ$_{x,2,0}$, respectively, in presence of a capacitive defect located between word-line "1" and word-line "2" labeled as C3. Simulations were performed using write sequences previously described.

TABLE VI. MTJ$_{x,1,0/x,3,0}$ CHARACTERISTICS UNDER WRITE OPERATIONS

Operation	C3 (fF)	V (mV)	I (uA)	R (kΩ)	T (°C)	M
0W0	1.00	749.16	604.51	1.23	187.38	1
	10.00	755.41	576.71	1.23	147.72	1
1W0	1.00	747.10	605.60	1.22	190.58	1
	10.00	864.84	519.58	**1.70**	155,94	**-1**
0W1	1.00	749.16	604.50	1.23	187.37	-1
		864.77	541.71	1.59	181.30	
	10.00	755.42	576.70	1.23	147.71	-1
		853.37	546.17	1.59	169.08	
1W1	1.00	747.05	605.66	1.23	190,57	-1
		863.63	542.29	1.59	183.02	
	10.00	864.85	519.57	1.23	155.93	-1
		869.09	538.41	1.59	173.94	

TABLE VII. MTJ$_{x,2,0}$ CHARACTERISTICS UNDER WRITE OPERATIONS

Operation	C3 (fF)	V (mV)	I (uA)	R (kΩ)	T (°C)	M
0W0	1.00	758.25	599.58	1.23	173.55	1
	10.00	0	0	-	27.00	1
1W0	1.00	755.70	600.49	1.22	177.40	1
	10.00	0	0	-	27.00	**-1**
0W1	1.00	758.24	599.59	1.23	173.55	-1
		867.51	540.31	1.59	177.15	
	10.00	0	0	-	27.00	1
		744.38	531.97	**1.39**	92.59	
1W1	1.00	755.75	600.51	1.23	177.41	-1
		866.08	540.96	1.59	179.40	
	10.00	0	0	-	27.00	-1
		862.29	477.05	1.80	100.78	

In Figure 8, we show temperature profiles for W1 operations performed in one memory page under C3=10fF. This defect adds an extra delay when selecting/deselecting both defective word-lines.
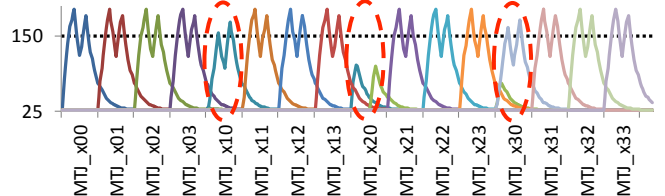

Figure 8. 16 bits W1 under capacitive defect (C3=10fF) temperature profile

As observed for C2, the selection of word-line "1" is delayed in the presence of C3 (operation performed on MTJ$_{x,1,0}$). Next three operations performed on MTJ$_{x,1,1}$, MTJ$_{x,1,2}$ and MTJ$_{x,1,3}$ that share same word-line work properly as their word-line is fully selected. The operation performed on MTJ$_{x,2,0}$ has an undesired behavior as C3 delays both word-line "1" de-selection and word-line "2" selection. Next three operations performed on MTJ$_{x,2,1}$, MTJ$_{x,2,2}$ and MTJ$_{x,2,3}$ work properly. The operation performed on MTJ$_{x,3,0}$ has an undesired behavior as C3 delays the word-line "2" de-selection. In addition to *1W0* operations, *0W1* operations are not correctly performed in presence of C3. Such faulty behavior is modeled by both TF0 and TF1 (Transition Fault 0 to 1).

D. Word-line – MTJ's bottom metal (C4)

Table VIII summarizes MTJ's simulated characteristics in presence of a capacitive defect located between word-line "1" and MTJ's bottom metal labeled as C4.

TABLE VIII.   MTJs CHARACTERISTICS UNDER WRITE OPERATIONS

Operation	C4 (fF)	V (mV)	I (uA)	R (kΩ)	T (°C)	M
0W0	0.10	746.38	605.99	1.23	191.51	1
	1.00	746.34	605.92	1.23	191.60	1
1W0	0.10	744.69	606.90	1.22	194.09	1
	1.00	744.66	606.69	1.22	194.20	1
0W1	0.10	746.37 / 863.95	605.99 / 542.13	1.23 / 1.59	191.52 / 182.55	-1
	1.00	746.33 / 863.79	605.92 / 542.53	1.23 / 1.59	191.61 / 182.71	-1
1W1	0.10	744.67 / 862.94	606.92 / 542.68	1.23 / 1.59	194.10 / 183.95	-1
	1.00	744.63 / 862.97	606.71 / 542.66	1.23 / 1.59	194.20 / 184.00	-1

In Figure 9, we show temperature profiles for W1 operations performed in one memory page under C4=1fF.
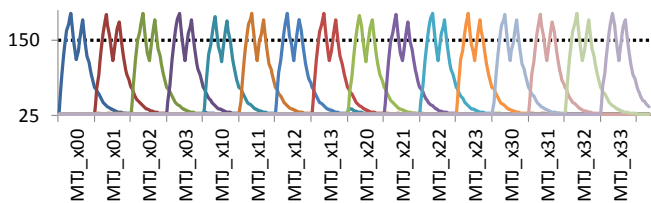

Figure 9.   16 bits W1 under capacitive defect (C4 =1fF) temperature profile

These electrical simulations show that C4 defect does not impact the functional operations of the TAS-MRAM.

V.   CONCLUSION AND FUTURE WORK

In this paper, we have analyzed the impact of capacitive defect on the TAS-MRAM performance. Capacitive defect locations were extracted from the layout of the TAS-MRAM array and are simulated on a 16-words architecture enabling any sequences of read/write operations. Results have shown that writing operations may be affected by these coupling defects. Especially, we have demonstrated that some capacitive defects behave as transition faults while others, even if there is an effective coupling, do not change the functional operation of the TAS-MRAM. As future work, we plan to use these analyses results to guide the test phase by providing effective test algorithms targeting fault related to actual defects that may affect TAS-MRAM architectures.

REFERENCES

[1] Semiconductor Industry Association, "International technology roadmap for semiconductors (ITRS)," 2011.

[2] C.L. Su, C.W. Tsai, C.W. Wu, C.C. Hung, Y.S. Chen, and M.J. Kao, "Testing MRAM for Write Disturbance Fault," in Proc. of IEEE International Test Conference, pp. 277-288, 2006.

[3] C.L. Su, R.F. Huang, and C.W. Wu, "MRAM Defect Analysis and Fault Modeling," in Proc. of IEEE International Test Conference, pp. 124-133, 2004.

[4] J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri, G. Prenat, J. Alvarez-Herault, and K. Mackay, "Impact of Resistive-Open Defects on the Heat Current of TAS-MRAM Architectures," in Proc. of Design Automation and Test in Europe, pp. 532-537, 2012.

[5] J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri, G. Prenat, J. Alvarez-Herault, and K. Mackay, "Impact of Resistive-Bridge Defects in TAS-MRAM Architectures," in Proc. of IEEE Asian Test Symposium, 2012.

[6] X. Aragones, J.L. Gonzalez, F. Moll, and A. Rubio, "Noise Generation and Coupling Mechanisms in Deep-Submicron ICs," IEEE Design & Test of Computers, vol. 19, no. 5, pp. 27-35, Sept.-Oct. 2002.

[7] D.D. Tang and Y.J. Lee, "Magnetic Memory – Fundamentals and Technology," Cambridge University Press, UK, 2010.

[8] M. El Baraji et al., "Dynamic Compact Model of Thermally Assisted Switching Magnetic Tunnel Junctions," Journal of Applied Physics, vol. 106, n° 12, 2009.

[9] W. Guo, "Compact Modeling of Magnetic Tunnel Junctions and Design of Hybrid CMOS/Magnetic Integrated Circuits," Ph.D. Thesis at Institut Polytechnique de Grenoble, 2010.

[10] Cadence Inc., Spectre, User Guide 2008.